Department of Computer Engineering,
University of Peradeniya
January 28, 2025

Group: 09

E/21/148 : GANATHIPAN S.
E/21/152 : GEORGE A. V.
E/21/156: GUNARATNE I.A.T.A.
E/21/157: GUNARATNE R.C

Overview

The objective of this project was to design a traffic light control system for a four-way junction using combinational logic circuits. The system was developed to simulate realistic traffic constraints while ensuring efficient traffic flow and pedestrian safety. The solution aims to achieve simplicity in circuit design, efficient resource utilization, and adherence to real-world traffic management principles.

System Design Constraints

1. **Lane Configuration**:
   Each lane consists of six tracks—three for one direction and three for the opposite direction.
2. **Signal Types**:
   Each lane is equipped with separate signals for the following:
   - **Pedestrian Crossing (P)**
   - **Left Turn (L)**
   - **Right Turn (R)**
   - **Forward Movement (F)**
3. **Pedestrian Safety**:
   - The system strictly enforces pedestrian safety by ensuring:
     i. Only one pedestrian crossing or two opposite-direction crossings are active simultaneously.
     ii. Simultaneous adjacent pedestrian crossings are prohibited to avoid accidents.
4. **Lane Priority**:
   To ensure smooth traffic flow, priority is given to vehicles in the left lane when conflicts arise.

Truth Table

Timer				N				E				S				W			
A	B	C	D	P	L	F	R	P	L	F	R	P	L	F	R	P	L	F	R
0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0
0	0	1	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0
0	1	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0
1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1
1	0	1	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0
1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1
1	1	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0

Boolean Expressions

1. North Lane
    a. Pedestrian

$$F = A \cdot D + \neg A \cdot \neg D \cdot (\neg(B \oplus C))$$

    b. Left Side

$$F = (A \oplus C) \cdot \neg(B \cdot D)$$

    c. Forward

$$F = \neg A \cdot D + A \cdot C \cdot \neg(B \cdot D)$$

    d. Right Side

$$F = B \cdot C \cdot (A \oplus D) + \neg A \cdot D \cdot (B \oplus C)$$

2. East Lane
    a. Pedestrian

$$F = \neg A \cdot D + A \cdot \neg D \cdot (B \oplus C)$$

    b. Left Side

$$F = A \cdot D \cdot (B \oplus C) + B \cdot \neg C \cdot \neg(A \oplus D)$$

    c. Forward

$$F = \neg A \cdot \neg D \cdot (\neg(B \oplus C)) + \neg A \cdot C \cdot \neg(B \cdot D)$$

    d. Right Side

$$F = (A \oplus C) \cdot \neg(B \cdot D)$$

3. South Lane
    a. Pedestrian

$$F = B \cdot C + \neg A \cdot \neg(B \cdot D)$$

    b. Left Side

$$F = A \cdot \neg C \cdot (B \cdot D)$$

    c. Forward

$$F = \neg A \cdot \neg C \cdot (B \cdot D) + A \cdot C \cdot \neg(B \cdot D)$$

    d. Right Side

$$F = B \cdot \neg C \cdot \neg(A \oplus D) + A \cdot D \cdot (B \oplus C)$$

4. West Lane
    a. Pedestrian

$$F = \neg A \cdot \neg C \cdot (B \cdot D) + A \cdot \neg(B \cdot D)$$

    b. Left Side

$$F = \neg A \cdot D \cdot (B \oplus C) + B \cdot C \cdot (A \oplus D)$$

    c. Forward

$$F = \neg A \cdot \neg D \cdot (\neg(B \oplus C)) + B \cdot \neg C \cdot \neg(A \oplus D)$$

    d. Right Side

$$F = A \cdot \neg C \cdot (B \cdot D)$$

Logic Circuit Diagram

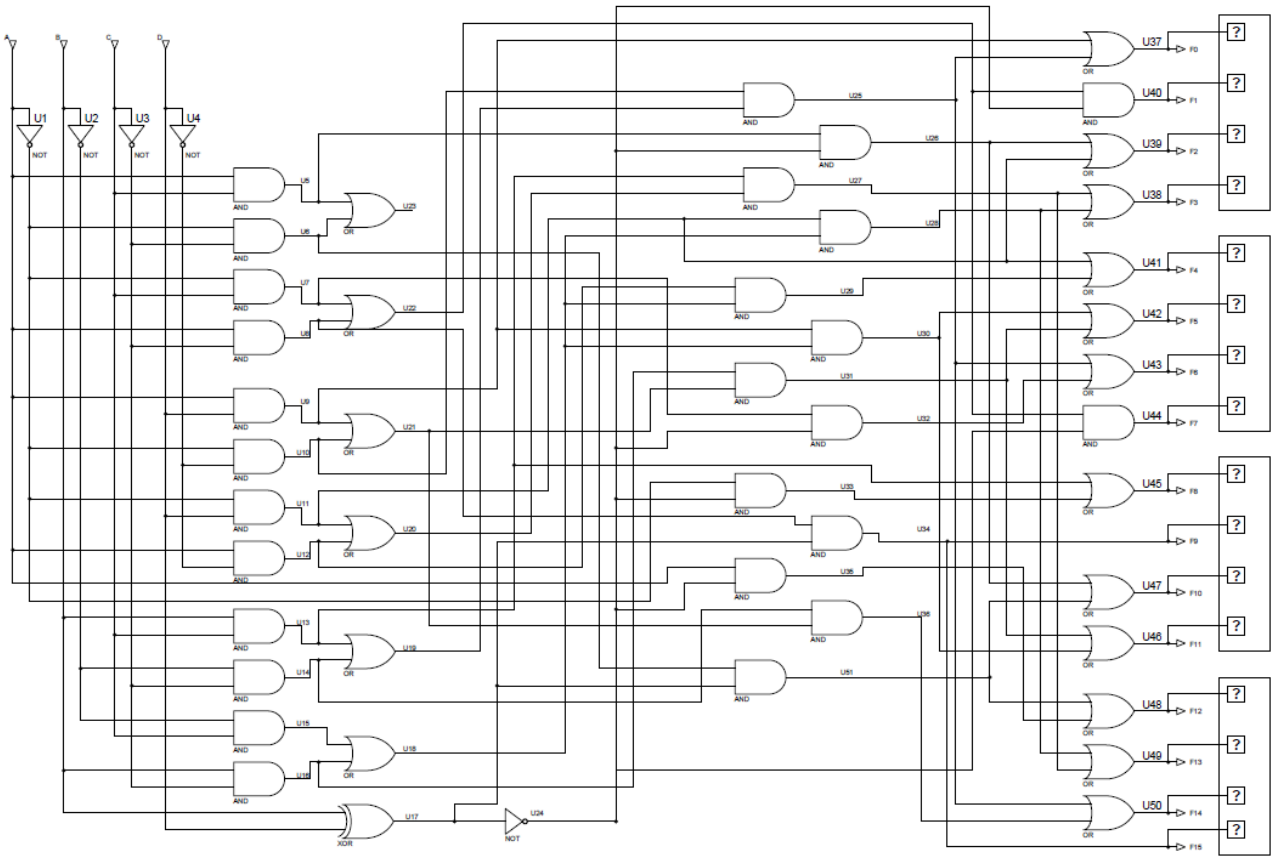

Figure 01: Function Unit for Traffic Determination

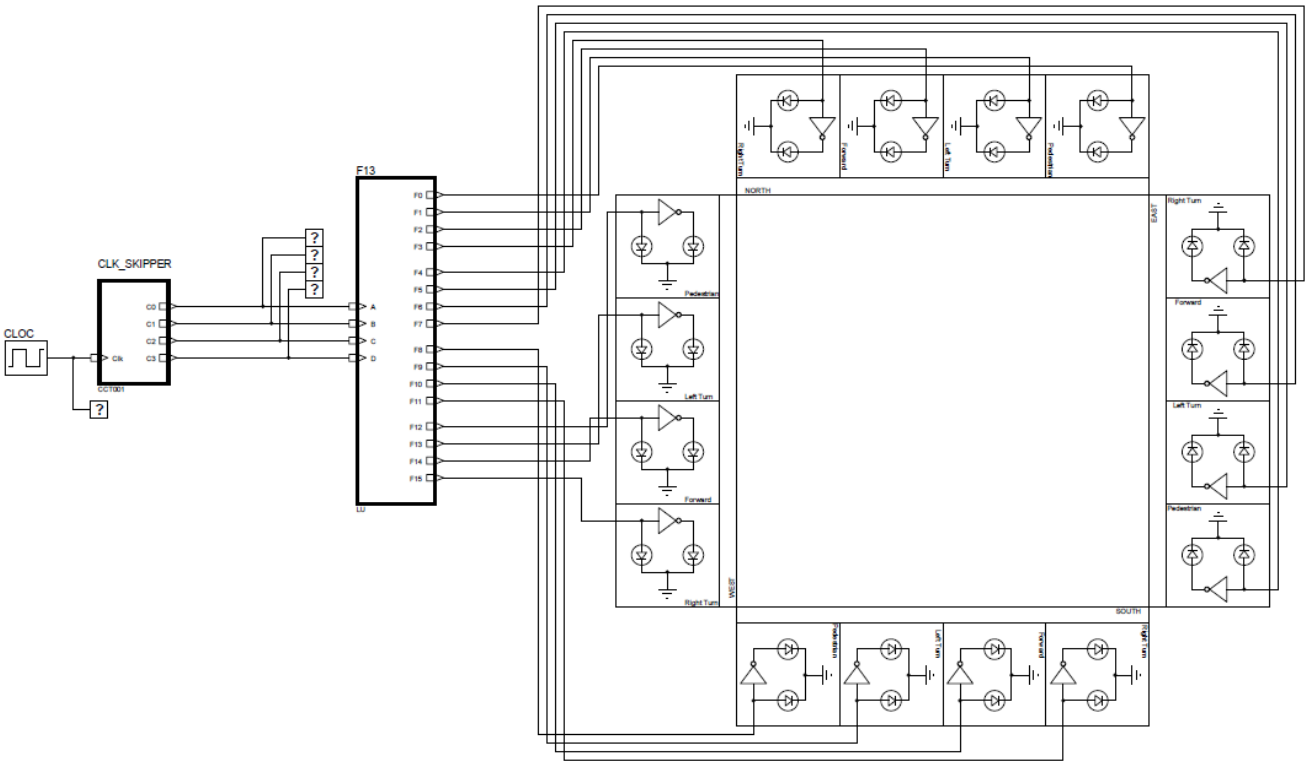

Figure 02: Overall Diagram with Traffic Light and Modules

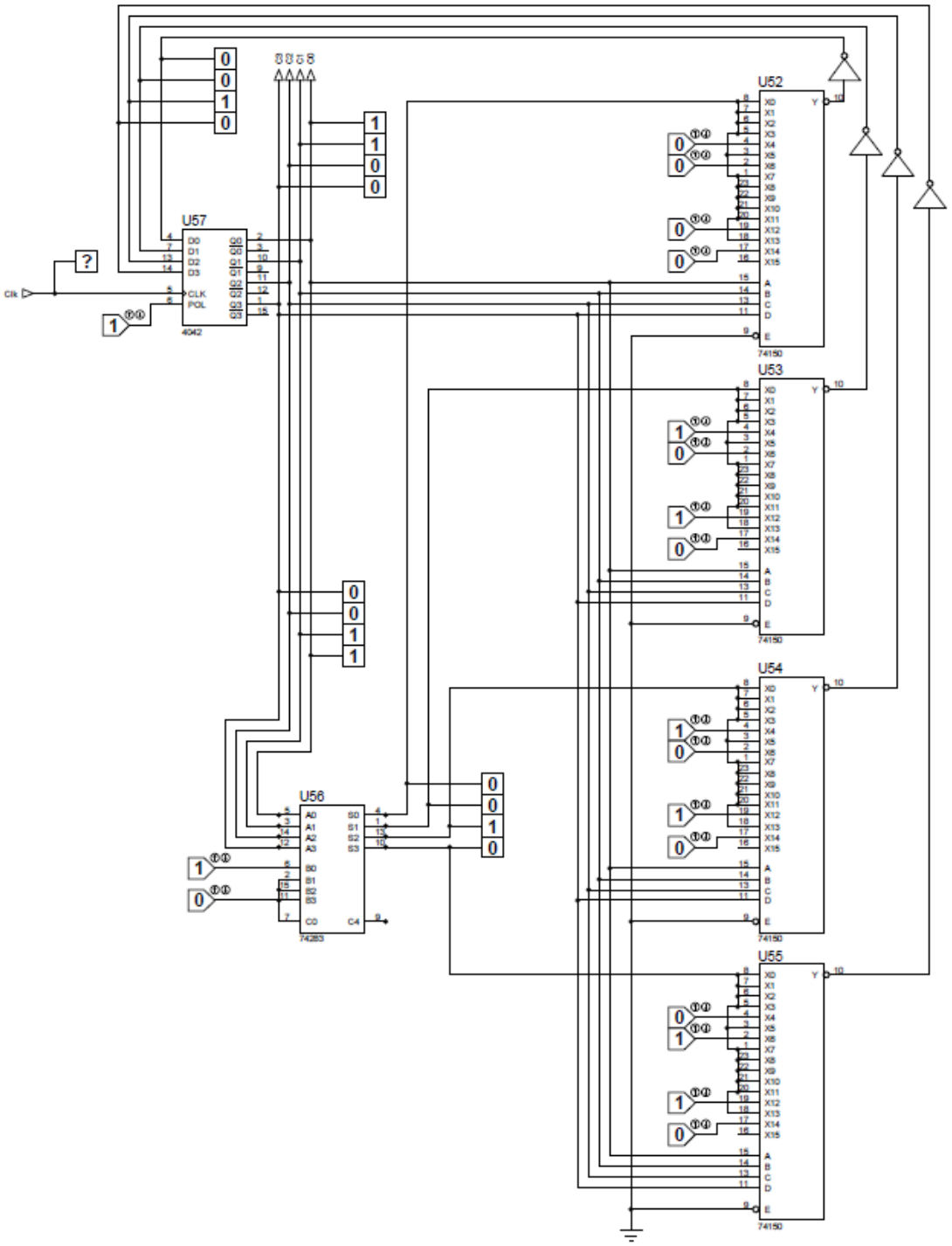

Figure 03: Clock Module to count for 12 periods

Verification

To ensure the accuracy and efficiency of the traffic light control system, a systematic verification process was conducted using both software-based simulation and manual validation methods:

1. Python Program for Permutation Testing

- A Python program was developed to generate and test **permutations of signal combinations** for the four-way junction.
- The program simulated various traffic scenarios to identify a **best-fit set of signal instances** that adhere to the defined constraints (e.g., no conflicting signals, pedestrian safety, and lane priorities).
- Outputs were analyzed to ensure:
    1. Logical correctness of the signal transitions.
    2. Compliance with safety rules (e.g., preventing simultaneous adjacent pedestrian crossings).

2. Manual Logic Verification

- The Boolean expressions derived for each signal (Pedestrian, Left, Forward, Right) were **manually checked against the truth table** for accuracy.
- The logical reductions were re-evaluated to ensure minimal gate usage while preserving functionality.

3. Simulation Logic Verification

- All the modules are developed in Proteus 8 software and tested with all conditions to work smoothly.

Optimized Design

A 4 × 4 Karnaugh Map (K-Map) was utilized to simplify all the logical combinations. The timer operates on a cycle of 16 periods, with 4 periods designated as "don’t care" conditions to simplify calculations further.

To minimize the number of gates required in the circuit:

1. **Reduction of Logic**:
    - The logical expressions were reduced to their simplest forms using the K-Map, ensuring the least number of terms were used.
    - This leads to only 51 gates in the traffic module.
2. **Gate Optimization**:
    - XOR gates were prioritized for their ability to simplify combinations of multiple conditions.
    - XOR gates were implemented using AND and OR gates to reduce the overall gate count.
    - Outputs of AND gates were shared across multiple parts of the circuit, improving resource utilization.
3. **Modular Design:**
    - The circuit was divided into the following modules:
        i. Traffic Logic Module: Manages signal combinations.
        ii. Counter Module: A timer to control the 16-period operation cycle.
        iii. Skipper Module: Handles specific count-based operations.

This method not only simplifies the circuit but also ensures efficient utilization of resources while maintaining the required functionality.