Brunel University London

重庆邮电大学

CHONGQING UNIVERSITY OF POSTS AND TELECOMMUNICATIONS

Lab Report

TERM: **2023-2024**

Module: **EE2627 Electronic Systems**

CLASS: 34092102

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Lab of Design and Simulation of Audio Signal Selector for Radio Stations.

1. Introduction

1.1. Aims

The aim of this experiment is to design and execute a compact electronic system that fulfills the specified requirements. Initially, validation of the correct logic is ensured through simulation. Subsequently, the circuit is constructed to demonstrate its practical functionality.

This experiment aims to foster our proficiency in communication, collaboration, and problem-solving skills through both group and individual projects, thereby enhancing our practical understanding and application of electronic systems.

1.2. Objectives

The objective of this experiment is to create an audio signal selector, essentially a signal gating circuit. This involves evaluating the design's strengths and weaknesses, as well as analyzing any shortcomings in the circuit's functionality. Additionally, this project offers valuable experience in prototype construction methods, utilizing laboratory equipment to assess prototype performance, and gaining insights into PCB layout techniques.

2. Electronic System Design and Simulation

2.1. Design specifications

The design specification requires the creation of an electronic system capable of gating a **1 kHz sinusoidal waveform**. The gating should occur as close as possible to the zero crossings of the sinusoidal waveform. When the gating is off, the output should be at 0 volts. However, upon activation, the output level should be variable up to a **maximum of 5 volts RMS** with **no DC component**. The output resistance should remain low, not exceeding 50 Ohms, and the unit should be powered by standard laboratory supplies. A design hint suggests achieving accurate detection of the sinusoid's zero crossings by using a level oscillator with a substantial output.

2.2. Design concept

2.2.1. The overall design

Based on the topic's requirements, the design primarily comprises two main segments. The initial segment involves generating three distinct waveforms, while the subsequent part involves sequentially connecting these output waveforms through the switch.

2.2.2. The 1st part design

This section primarily addresses the challenge of processing three waveform signals as specified. To generate sine, square, and triangular waves, an approach utilizing the **RC oscillator**

is employed initially to produce the sine wave [1]. Subsequently, the sine wave is transformed into a triangular wave using a Schmidt trigger, and finally shaped into a triangular waveform through an integrator.

Due to inherent phase differences in this conversion process, a phase shifter is employed to ensure all waves are ultimately synchronized in phase.

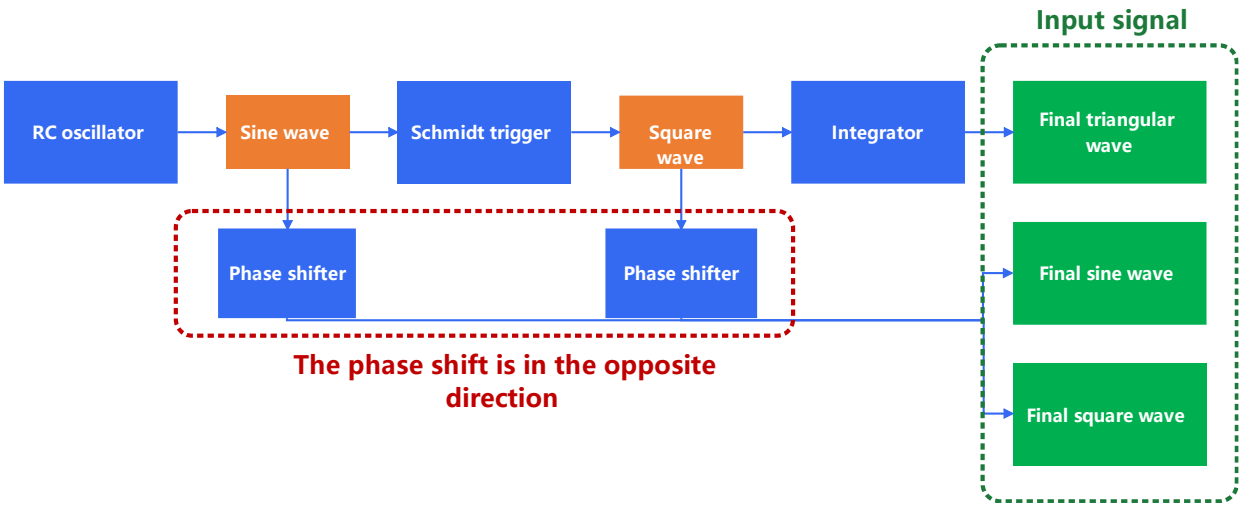

Figure 1: Block diagram of 1st part

As shown in figure 1, through the table diagram, it is very intuitively seeing my thoughts on the design of the 1st part.

2.2.3. The 2nd part design

As per the specifications, each of the three waveforms is required to persist for two cycles before transitioning. The design incorporates a timer to regulate the cycle duration, utilizes a gate circuit for encoding and decoding purposes, and employs an analog switch to manage the input control of the signal.

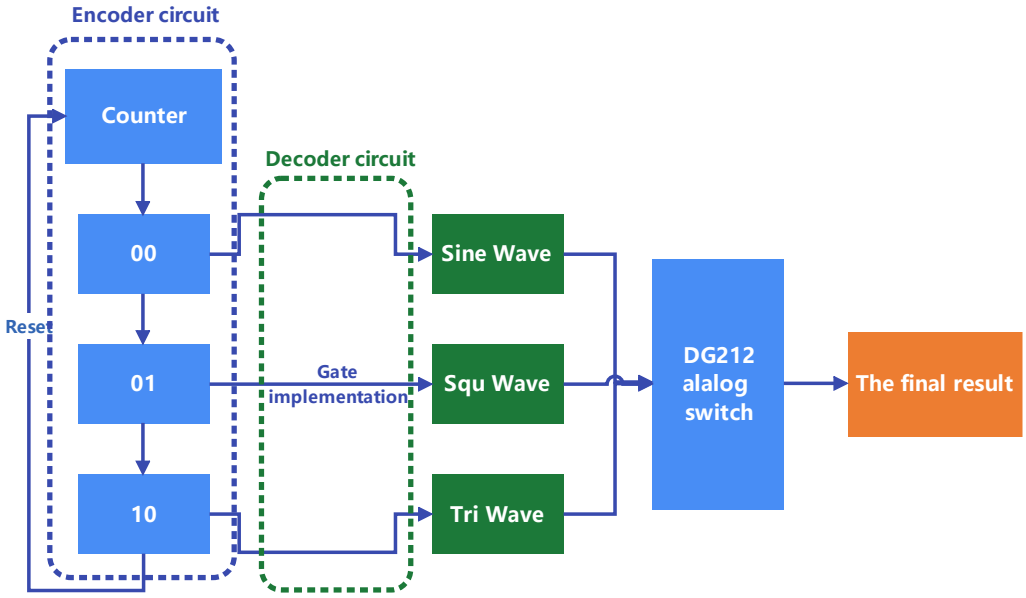

Figure 2: Block diagram of 2nd diagram

Figure 2 shows the 2nd part block diagram, the waveform of the output final result can be measured by an oscilloscope.

2.3. Cell circuit design process and principles description

2.3.1. Sine wave signal generator

(1) Determination of resonant frequency

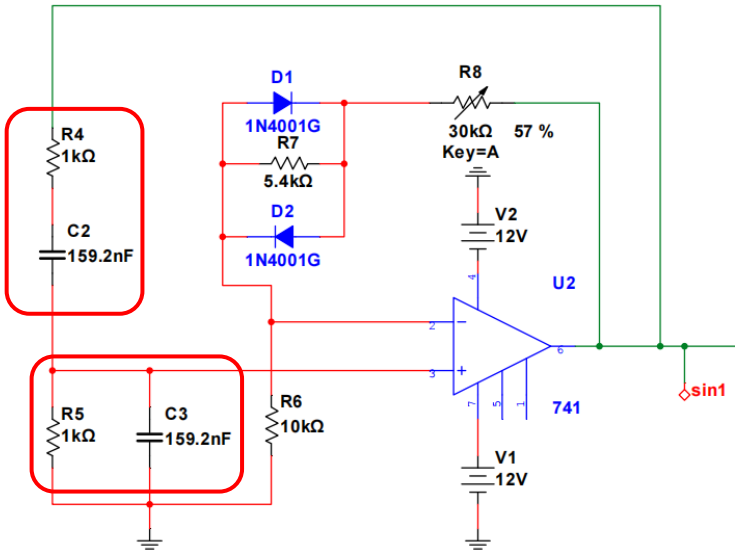

Figure 3: 'RC' sine-wave oscillator

The experimental circuit for the **RC sine wave oscillator** is depicted in Figure 3. It incorporates an RC series-parallel frequency selection network comprising R_4, C_2, R_5, and C_3, which introduces positive feedback. The resonant frequency of this network is $f_0 = \frac{1}{2\pi\sqrt{R_4 R_5 C_2 C_3}}$. At this frequency, the gain of the RC series-parallel network is 1/3. Consequently, to satisfy the amplitude condition for sinusoidal oscillation, the gain of the in-phase proportional amplifier, constructed with an op-amp and resistors R6, R7, and R8, should be set at $1 + \frac{R_7 + R_8}{R_6} \geqslant 3$ (Greater than 3 when starting and equal to 3 when stable).

Given the requirement for a 1 kHz sine wave output, the crucial aspect is to establish the resonant frequency. To streamline the calculation process, I set $R_4 = R_5 = R$, $C_2 = C_3 = C$. Therefore, the resonant frequency is $f_0 = \frac{1}{2\pi \cdot RC}$. Let $R = 1k\Omega$, it can be found that $C = 159.2\ nF$.

(2) Determination of starting vibration resistance value

Additionally, it's crucial to set the gain to ensure a smooth start of oscillation. While a calculation formula has been provided earlier, discrepancies may arise during actual circuit simulations. Hence, the optimal approach is to configure R_8 as a sliding rheostat and iteratively adjust its value until the oscilloscope displays a normal waveform.

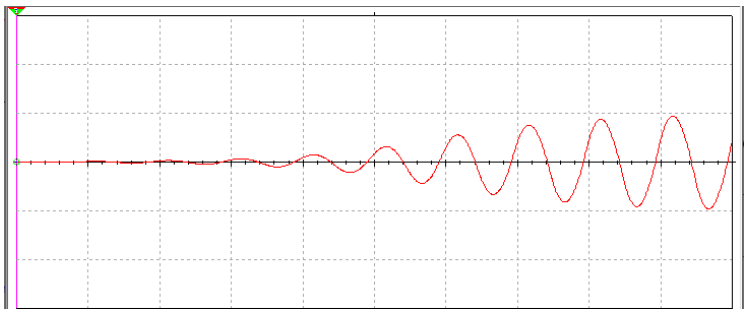

Figure 4: $\boldsymbol{R_8}$ is the onset and steady amplitude oscillation waveform at **57%** of the total value

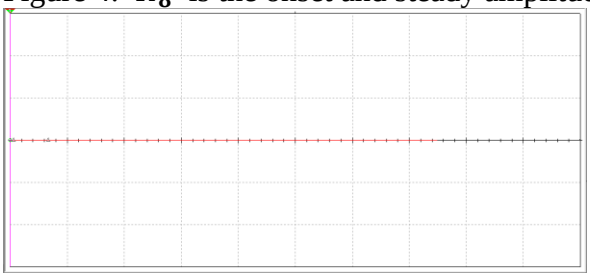

Figure 5: $\boldsymbol{R_8}$ at **30%** of the total value

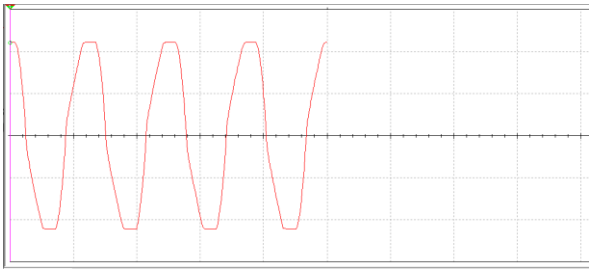

Figure 6: $\boldsymbol{R_8}$ at **90%** of the total value

Figure 4 displays a typical sine wave, whereas Figures 5 and 6 respectively exhibit situations where the waveform presents excessively small and large amplitudes. Consequently, I've determined that setting R_8 to 57% of the total value will result in the oscillating waveform achieving the desired onset and stable amplitude, concurrently set at 5V.

2.3.2. Generation of square and triangular waves

(1) Square wave generator

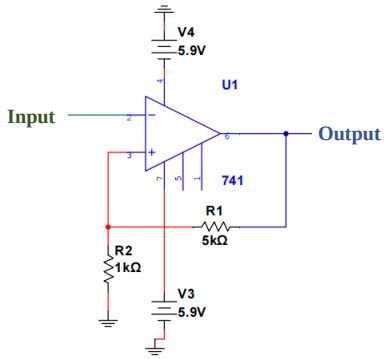

Figure 7: Square wave generator

Figure 7 shows a **Schmitt trigger** to achieve the output of a square wave. In electronics, a Schmitt trigger is a comparator circuit with **hysteresis** implemented by applying **positive feedback** to the noninverting input of a comparator or differential amplifier [2].

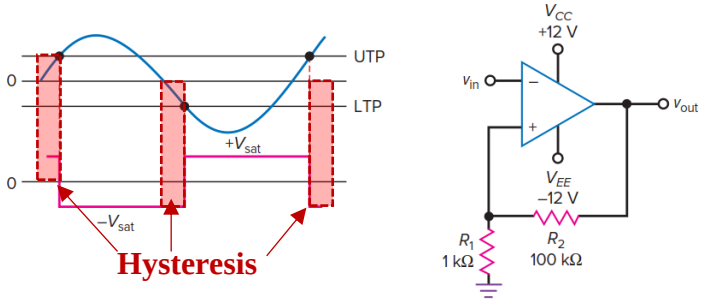

Figure 8: The waveform output of the Schmidt trigger

Figure 8 illustrates the principle of how the Schmidt trigger processes the input sine wave and outputs it as a square wave. Intuitively, it's apparent from the figure that the Schmidt trigger exhibits hysteresis. Owing to the threshold influence, the phase of the output square wave may not align consistently with the input sine wave. Hence, to achieve synchronized phase output for the three waveforms, subsequent adjustments are required. Figure 9 shows the output of the square wave and the phase difference between it and the sine wave.

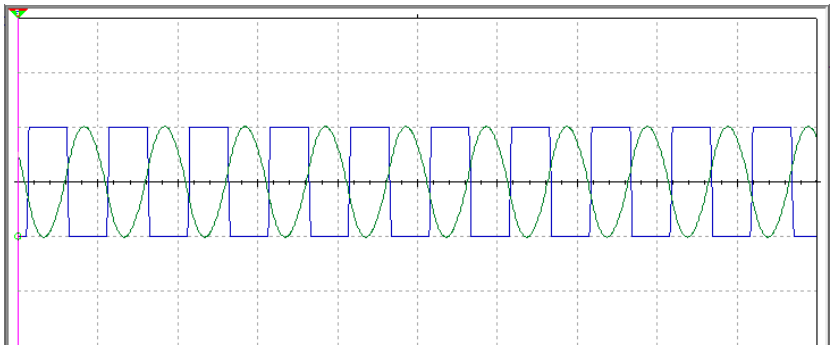

Figure 9: Square wave and sine wave

Finally, to attain a voltage output of 5V for the square wave, I had to adjust the supply voltage. Due to the internal characteristics of the amplifier, the square wave's output voltage reached 5V only after I adjusted the supply voltage to 5.9V.

(2) Triangular wave generator

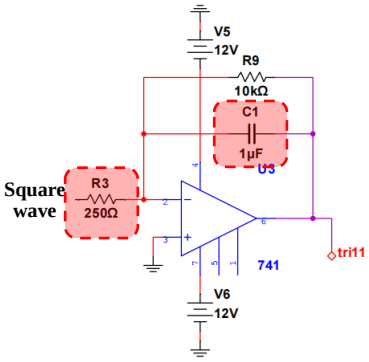

Figure 10: Integrator

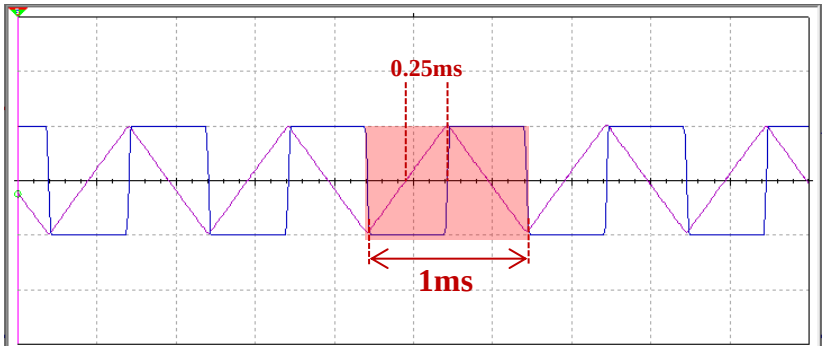

Figure 11: Triangular wave and square wave

Figure 10 depicts the circuit diagram of the triangular wave generator, while Figure 11 illustrates the input and output results. To generate triangular waves, we utilize an **integrator circui**t that takes a square wave as input and produces a triangular wave as output.

$$V_0(t) = -\frac{1}{RC}\int_0^t V_i(t)\ dt \tag{1}$$

Equation (1) shows the formula for calculating the output voltage of the integrator. In this situation, $R = R_3 = 250\Omega$, $C = C_1 = 1\mu F$, $t = 0.25ms$, $V_i(t)$ is the voltage of square wave, $V_i(t) = 5V$. After integrating, it can get the maximum value of triangular wave is $V_0(t) = 5V$. That is my thought process regarding the selection of capacitance and resistance values.

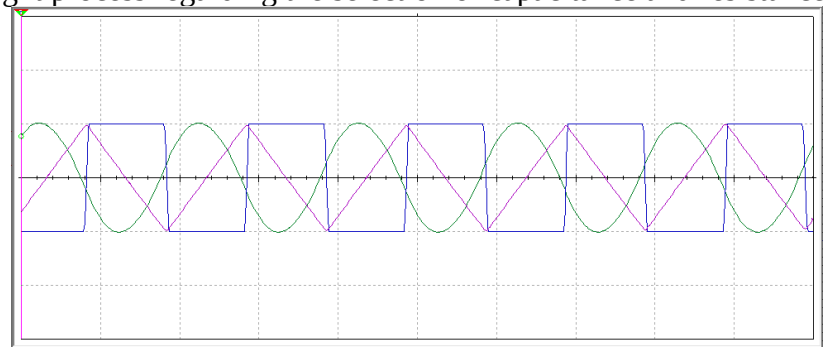

Figure 12: Results of the three waveforms

Figure 12 shows the three waveforms. However, the signal switching cannot occur due to the disparity in phases. Hence, it is imperative to process them in a synchronized phase.

2.3.3. Waveform phase shift

To accomplish waveform phase shifting, consider implementing a **phase shifter circuit**. Use the **triangle wave as a reference** to align the phases of the sine wave and the square wave. It's important to note that the phase shifter is solely compatible with sine waves. Consequently, the phase adjustment for the square wave must be achieved by synchronizing it with the phase shift applied to the sine wave.

(1) The shift term of the sine wave

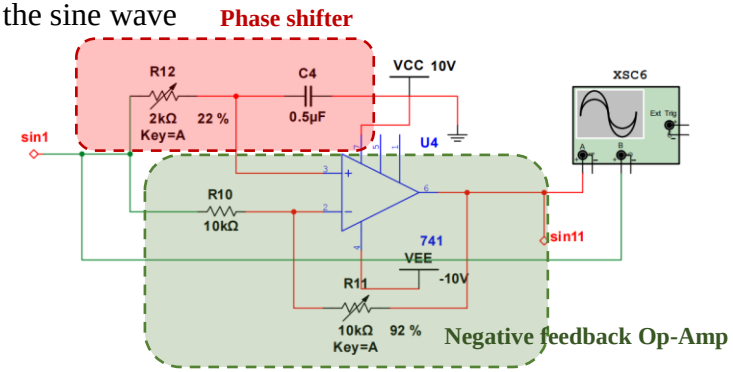

Figure 13: Sine wave phase shift circuit

Based on figure 12, it is evident that shifting the sine wave to the **right** is the optimal direction for achieving phase alignment. Since a phase shift is around $90°$, **a $0 \sim 180°$ phase shift is considered**.

$$H(j\omega) = \frac{1 - j\omega RC}{1 + j\omega RC}$$
$$\Phi(\omega) = -2\arctan(\omega RC) \tag{2}$$

Equation (2) demonstrates the transfer function and the phase shift function. However, in software, it is more convenient to employ a sliding rheostat for continuous adjustment until the two waveforms are perfectly aligned in phase.

(2) The shift term of the square wave

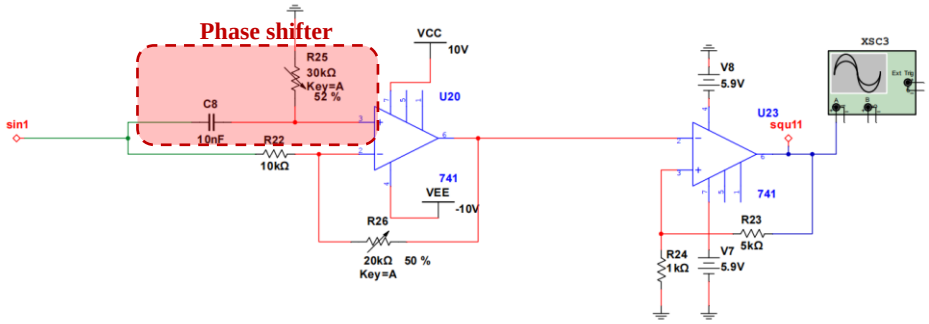

Figure 14: Square wave phase shift circuit

Like the sine wave phase shifter, it is observed that the square wave phase shifts in the **opposite direction** compared to the sine wave. Therefore, the positions of the capacitor and resistance in the phase shifter depicted in figure 13 are exchanged accordingly. Finally, a Schmidt trigger is incorporated to generate a square wave.

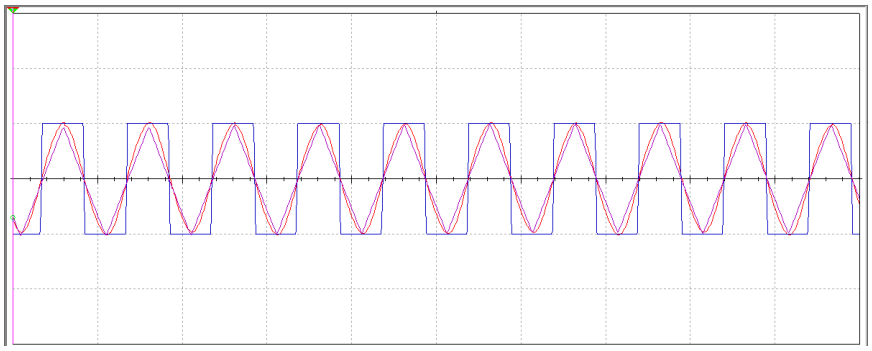

Figure 15: The final output waveform

Figure 15 displays the ultimate output waveform, wherein the three waveforms have been successfully synchronized to the same phase.

2.3.4. Counter setting

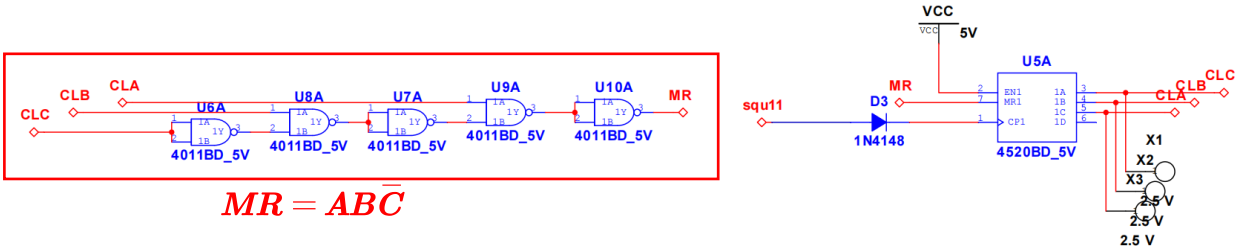

Figure 16: Counter and control circuit

Given that each waveform is intended to persist for 2 cycles, the combination of the three waveforms encompasses a **total of 6 cycles**. Consequently, a 3-bit binary system is employed to count these cycles, using the previously generated square wave as the clock control signal. However, since we only have 6 cycles in total and the 4520BD is a 4-bit counter, it's necessary to **reset the counter to zero after every 6 cycles**. In 4520BD, “CP1” means clock signal, “MR1” means reset, “1A~1D” means counting from low to high. Let $A = CLA$, $B = CLB$, $C = CLC$.

According to the gate circuit on the left of figure 16, $\mathbf{MR} = \mathbf{AB\overline{C}} = (\mathbf{110})_{\mathbf{2}} = (\mathbf{6})_{\mathbf{10}}$. Therefore, when MR=110, counter reset. Figure 17 shows the counter result, it can be verified that my inference is correct.

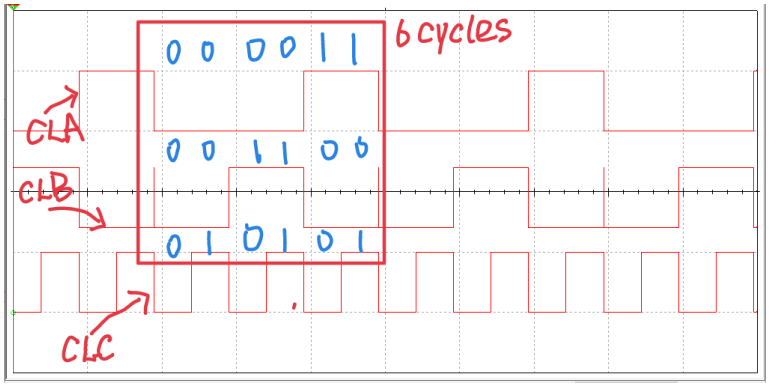

Figure 17: Counter result

2.3.5. Select signal output

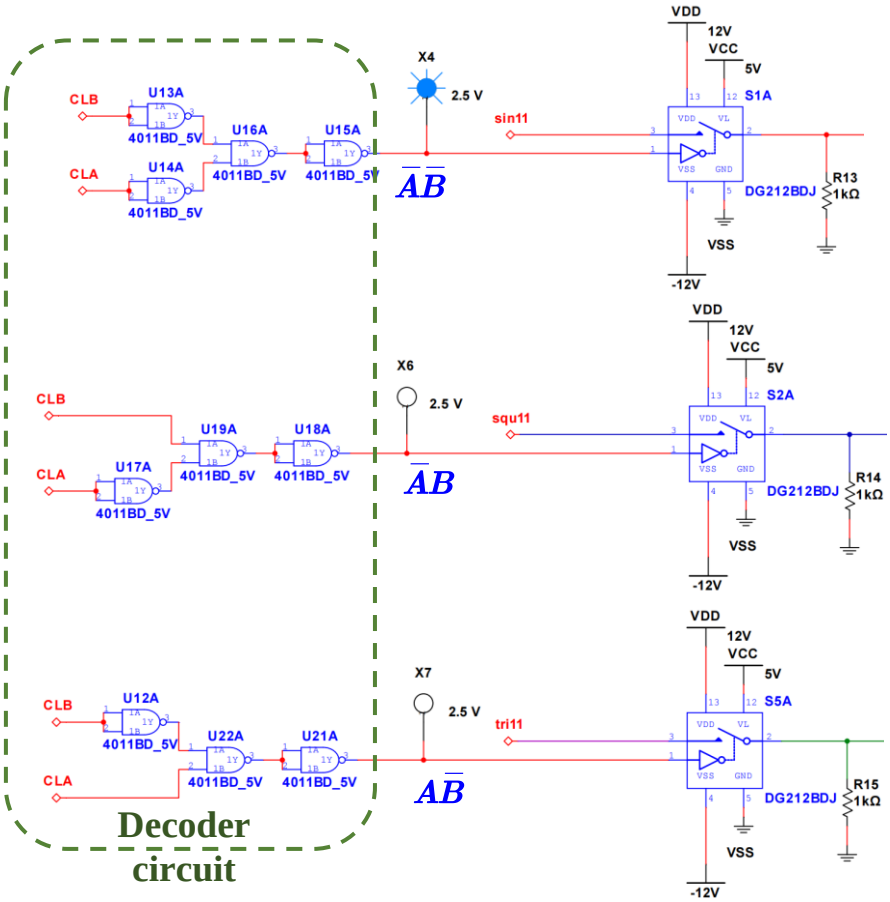

Figure 18: Waveform signal control unit

Figure 18 intuitively illustrates how to control the signal switching using a combination of digital circuits and analog switches. I used multiple 4011BD to make the decoder circuit. When $AB = 00$, the sine wave is input, when $AB = 01$, the square wave is input, when $AB = 11$, the triangular wave is input. The "DG212" represents an analog switch wherein, when the input is set to 1, the switch turns on, enabling the passage of the waveform.

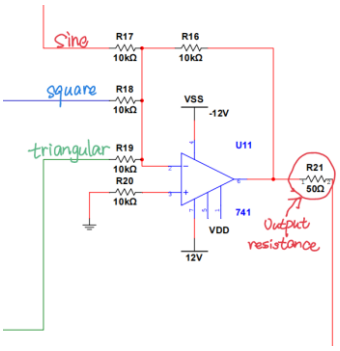

Figure 19: Output signal

As depicted in Figure 19, the ultimate output signal necessitates passing through a differential or reverse Op-amp. This step is crucial because the output result obtained is precisely the opposite of the intended waveform, thus necessitating a phase reversal through the Op-amp.

2.3.6. Optimization of waveform results

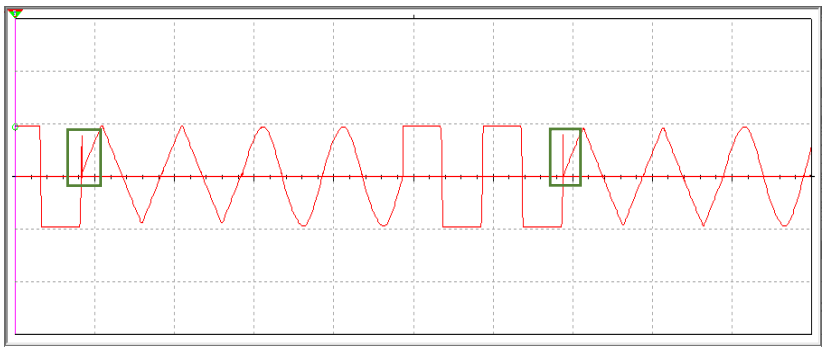

Figure 20: The waveform results before optimized

Referring to Figure 20, prior to optimization, the transition between the square wave and the triangle wave results in a pronounced jagged or "burr" phenomenon. This occurrence is attributed to the waveform's abundance of high-frequency components in the frequency domain, causing notable fluctuations in the time domain. To mitigate these unwanted artifacts, the implementation of a **low-pass filter (LPF)** is under consideration to effectively eliminate the burrs.

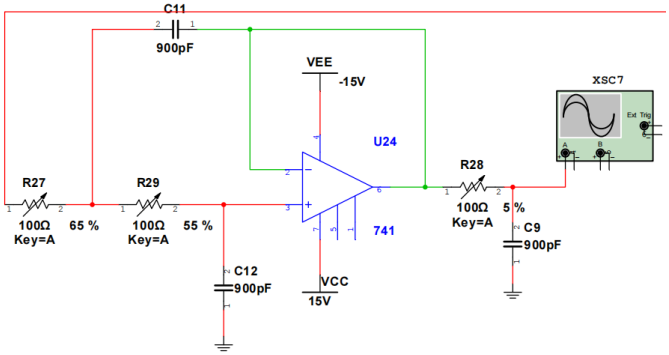

Figure 21: 3rd low-pass filter

Figure 21 shows the 3rd low-pass filter, $R = R_{27} = R_{28} = R_{29}$, $C = C_9 = C_{11} = C_{12}$. Therefore, the cut off frequency is $f = \frac{1}{2\pi \cdot RC}$ $(f \geqslant 1kHz)$. If the cutoff frequency is set too low, it might introduce interference to the original waveform. Conversely, if the cutoff frequency is set too high, it may not effectively filter out the burrs. After continuous adjustments, the optimal values for R and C have been determined.

2.4. Simulation results and analysis

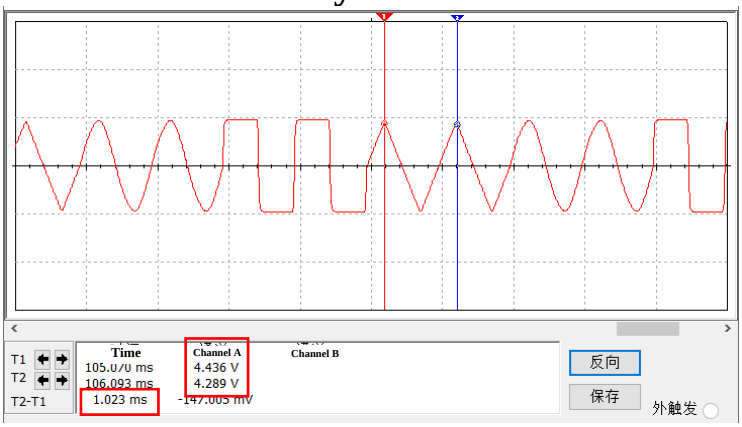

Figure 22: Simulation results

The final simulation result is shown in figure 22. The findings indicate a period of 1ms, equating to a frequency of 1kHz, with an amplitude measuring 4.4V. Waveform transitions occur precisely at the zero-crossing point every two cycles. All these observations align with the specified criteria for the Audio Signal Selector.

The total circuit diagram is shown in Appendix 1. In this circuit setup, no external input is required. The oscillator operates independently, generating sinusoidal signals, subsequently transformed into square and triangular waves through Schmidt triggers and integrators. The amplifiers utilized in the circuit are all "$\mu A741$". A NAND gates circuit and "4520BD" is employed to regulate the clock cycle, using the square wave as the control signal for precise waveform transitions at each zero-crossing point. An analog switch manages the control of waveform output. Finally, a LPF is incorporated to refine the output, ensuring the attainment of an ideal waveform. Through the oscilloscope, we can observe the final simulation results.

3. Hardware implementation

3.1. The initial circuit design

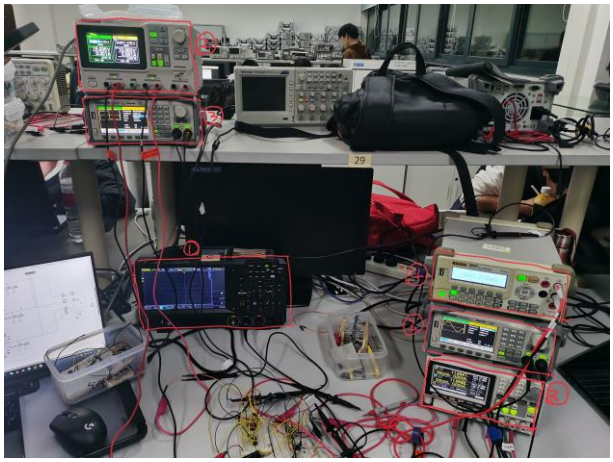

Figure 23: Experimental equipment

Figure 23 shows experimental facilities in our laboratory. During the actual circuit construction process, four types of equipment are required: ① is the oscilloscope, ② is the signal generator, ③ is the programmable DC power supply, and ④ is the multimeter.

Due to potential limitations in the accuracy of the breadboard, there might be difficulty in achieving the oscillator's functionality. As a solution, considering the availability of a signal generator among the provided experimental equipment, the decision is made to directly output the waveform using the signal generator.

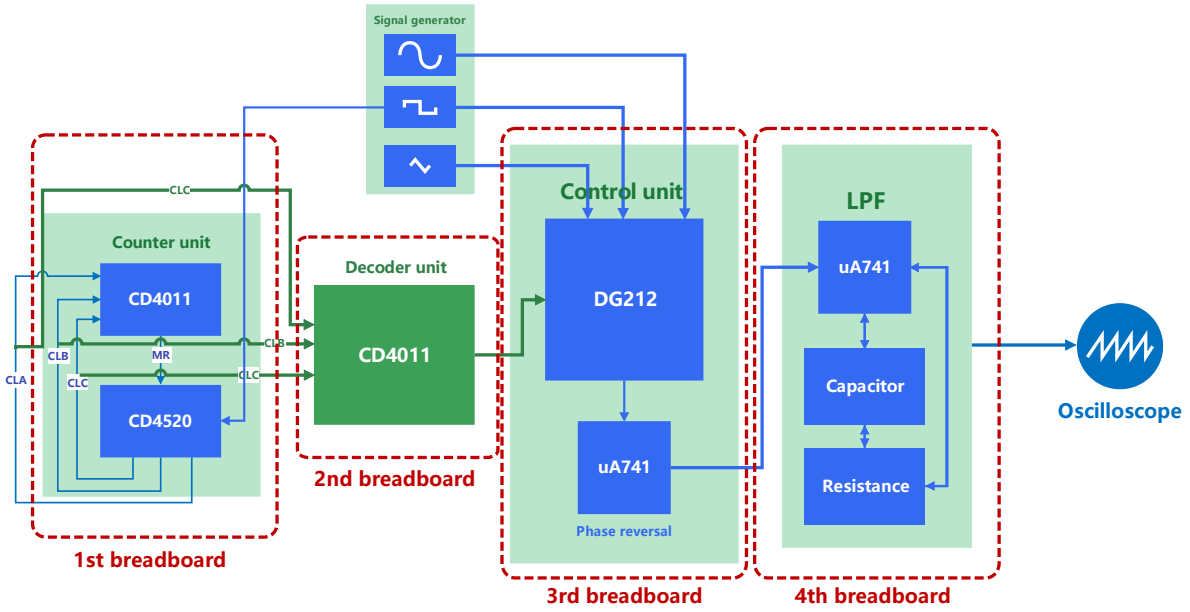

Figure 24: Design scheme block diagram

Figure 24 visually presents my comprehensive design scheme, primarily outlining the input and output configuration of each breadboard. The overall design concept closely mirrors the simulation approach.

3.2. Circuit construction

3.2.1. Counter unit

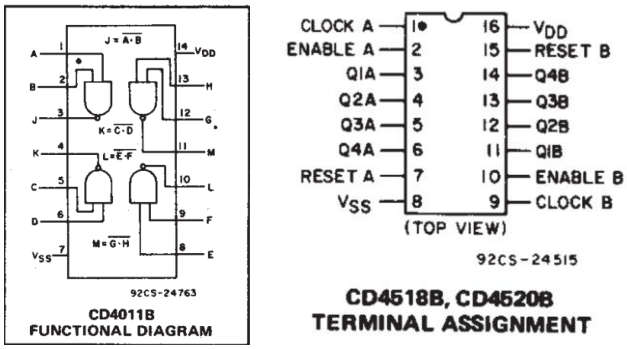

Figure 25: Schematic diagram of CD4011(left) and CD4520(right)

Unlike the simulated circuit, the physical chip CD4011 encompasses 4 NAND gates, while CD4520 integrates 2 counters. To construct the circuit design depicted in Figure 16, this setup requires 2 CD4011 chips and 1 CD4520 chip. Differing from the simulation, the real circuit includes Voltage Drain to Drain (VDD) and Voltage Source to Source (VSS). I connect VSS to ground and furnish a 5V supply voltage to VDD.

3.2.2. Decoder unit

Since in the process of designing the digital circuit, NAND gates are used for the convenience of subsequent hardware implementation in the gate circuit, the splicing of the

decoder is relatively simple. The reference circuit diagram is shown in figure 18. However, due to the large number of inputs, the decoder needs to leave more wires to connect with the previous part.

3.2.3. Control unit

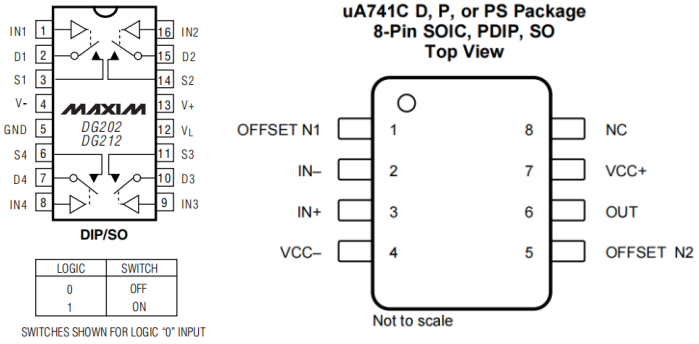

Figure 26: Schematic diagram of DG212(left) and uA741(right)

In this unit, I need use DG212 analog switch and $\mu A741$. The DG212 chip integrates 4 analog switches, thereby requiring only 1 chip to achieve the circuit's functionality. Within the DG212, the "IN" pin is associated with the gating circuit, controlling its connection status. The "S" pin links to the input waveform, while the "D" pin serves as the output signal. Additionally, "V_L" connects to 5V, whereas "V_+" and "$V\_$" connect to +12V and -12V, respectively.

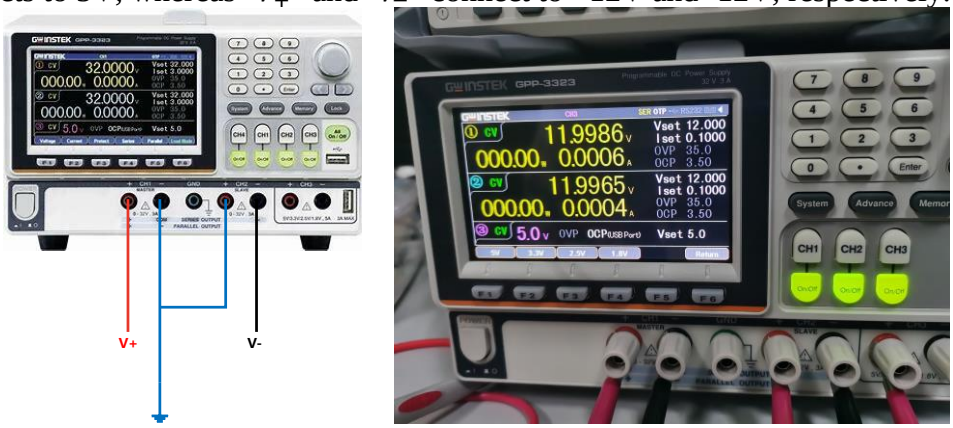

Figure 27: Negative volts from DC power supply

Both the DG212 and uA741 necessitate **negative voltage** for operation. However, the DC power supply can only deliver positive voltage. To address this, I configured the DC power supply in **series mode**, resulting in a short connection between the positive and negative terminals, illustrated in the left image of figure 27. Consequently, the negative terminal of the power supply is linked to the "$V\_$" of the DG212 to generate the required negative voltage.

The schematic for the uA741 is depicted in Figure 26. "IN-" and "IN+" represent the two comparison voltages, while "VCC+" and "VCC-" denote the supply voltages, requiring interconnection. The "OUT" serves as the output voltage. Notably, as the circuit is crafted without a voltage OFFSET, the "offset" terminal remains unconnected to any voltage source. Moreover, "NC" signifies "No internal connection".

3.2.4. LPF unit

In the low-pass filter section, I used a capacitor of 800pF and a resistor of 100Ω.

3.2.5. Breadboard circuit results

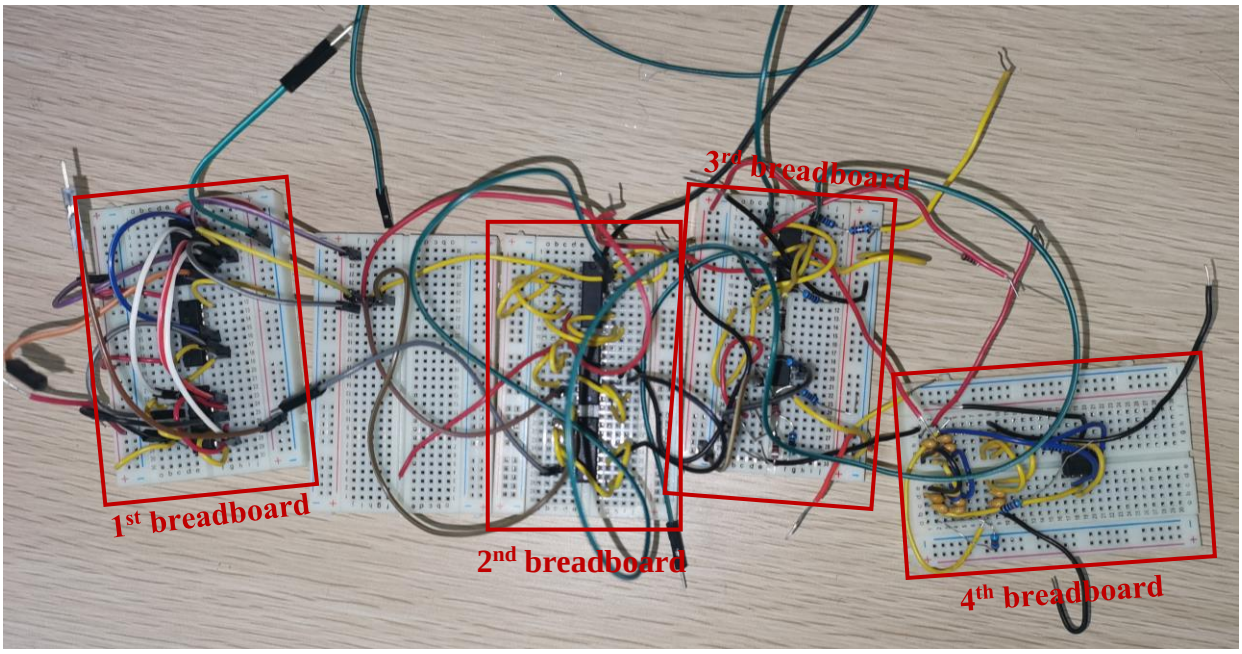

Figure 28: Breadboard circuit results

Figure 28 illustrates the resultant graph of my circuit assembly. Due to the extensive number of components, I utilized multiple breadboards and sequentially linked their inputs and outputs. The circuit's connection pattern aligns with that shown in Figure 24. To accommodate the frequent utilization of clocks CLA, CLB, and CLC, I introduced an additional breadboard to consolidate these three inputs.

3.3. Circuit testing and explanation

3.3.1. Circuit testing

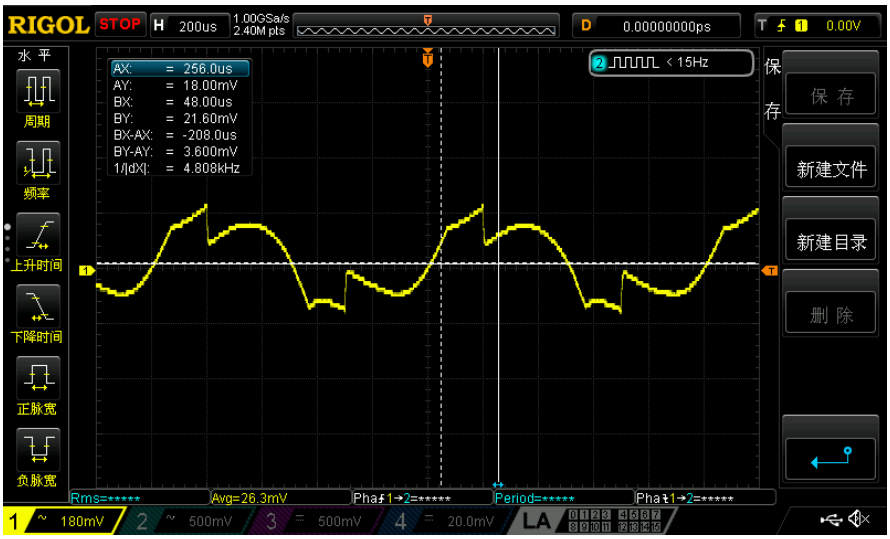

Figure 29: Circuit testing results

Figure 29 represents the conclusive test result diagram of the entire circuit, which, regrettably, exhibits unsatisfactory performance. A noticeable issue arises in the waveform switching process, indicating a problem with the switching method employed. Furthermore, upon repeated toggling of the waveform input, inconsistent final outcomes were observed.

3.3.2. Failure Cause Analysis

As I embarked on troubleshooting the circuit, my initial focus was on examining the first breadboard. Utilizing an oscilloscope to measure the output of CLA, CLB, and CLC, I observed that their cycles were consistent at 1ms and their amplitudes appeared to be identical. However, this observation contradicts the anticipated ideal result shown in Figure 17. Following a thorough inspection of the circuit connections without detecting any issues, it raised the possibility of a problem with the CD4520 chip.

Upon connecting the oscilloscope to the "RESET" pin of the CD4520 chip, a notable observation surfaced: the voltage exhibited a substantial rise followed by a subsequent fall **every 8ms**, resembling an impulse. However, in theory, there **should be an impulse every 6ms**, aligning with the representation in Figure 30.

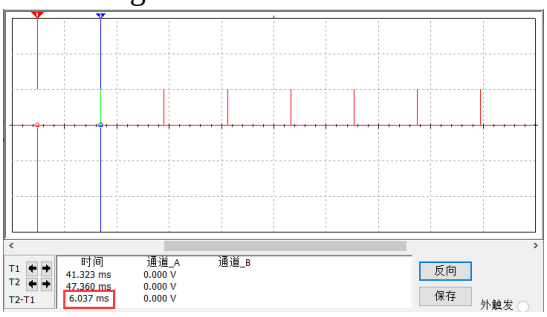

Figure 30: The ideal result for "MR (RESET)"

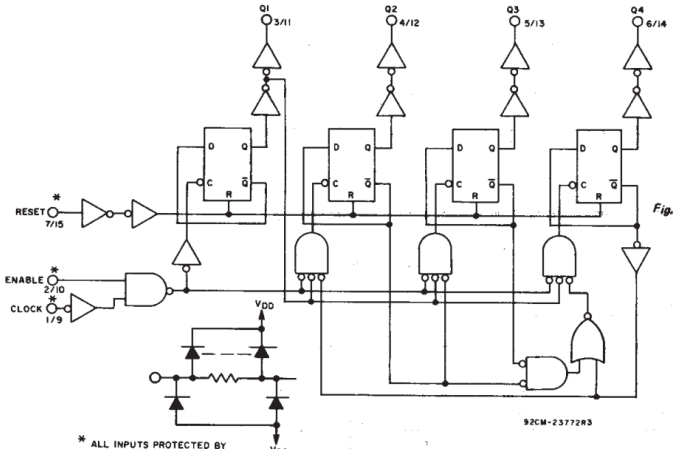

Figure 31: Schematic diagram of CD4520

Upon examining the schematic diagram of the CD4520, as shown in figure 31. It became apparent that the delay in the "RESET" pin is attributed to the complexity of the CD4520 chip itself and the interconnected combinatorial logic circuits in our design. **This complexity leads to operational delays in the circuit's functioning**.

Furthermore, I conducted voltage measurements across the breadboard using a multimeter and observed that each chip pin exhibited the expected voltage, indicating no issues with both the power supply and the chips themselves.

3.4. Evaluation and Modification of circuits

3.4.1. Circuit modification scheme

A simpler **JK flip-flop** is used as the control signal, and three JK flip-flops can be used to control three waveform input signals.

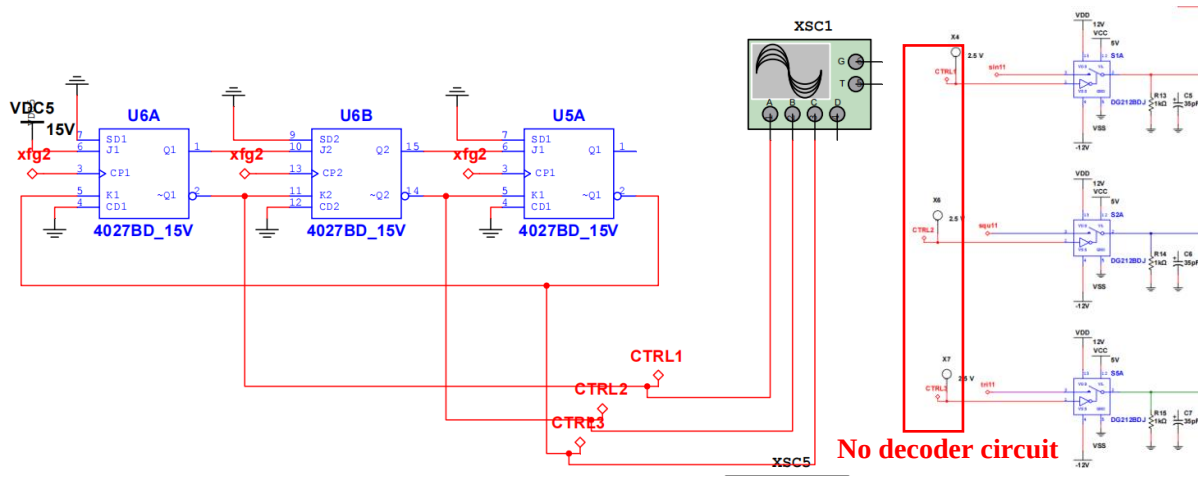

Figure 32: The improved circuit diagram

As shown in figure 32, three JK flip-flops are used in the improved scheme, and they are connected to the **same clock** to **avoid the occurrence of delay**.

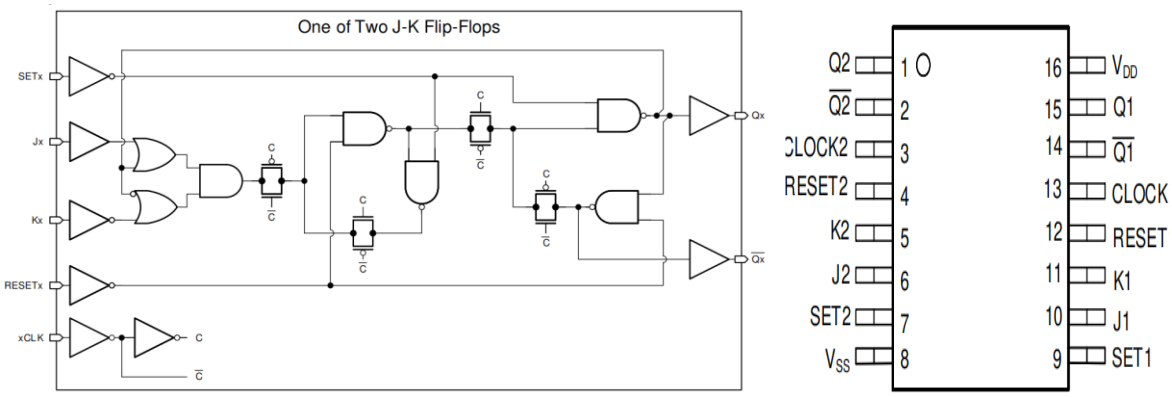

Figure 33: Schematic diagram(left) and pins(right) of CD4027

(1) The basic idea of the design

As depicted in figure 33, in this design, the utilization of "SET" and "RESET" is unnecessary; therefore, I set them to 0. Each waveform is required to persist for two cycles; Hence I configured the clock signal to 500Hz. Utilizing JK flip-flops allows for the direct generation of control signals, eliminating the need for a decoder, as shown in figure 32. This modification significantly simplifies the circuit design and **circumvents any delay generation**.

(2) Control signal generation principle

Table 1: JK-trigger truth table

J	K	Q_t	Q_{t+1}	
0	0	0	0	
0	0	1	1	
0	1	0	0	**Set to 0**
0	1	1	0	
1	0	0	1	**Set to 1**
1	0	1	1	
1	1	0	1	**Change state**
1	1	1	0	

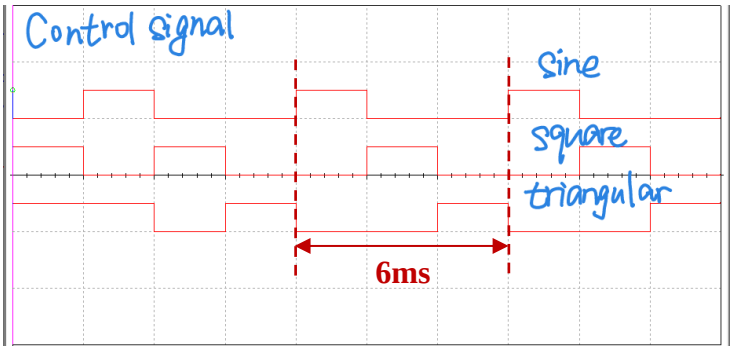

Figure 34: The control signal

Figure 34 illustrates the outcomes for the control signal. To ensure digital switching of the JK flip-flop, the initial flip-flop "J1" needs to be set to 1. Analyzing the truth table of the JK flip-flop, it can be deduced that the first flip-flop "JK=11" will persist for two clock cycles, thus switching twice. The subsequent flip-flops alternate between states "JK=10" and "JK=01".

Consequently, these three flip-flops achieve equilibrium and cleverly combine to produce control signals, each continuously outputting for 2ms.

3.4.2. Optimized circuit construction

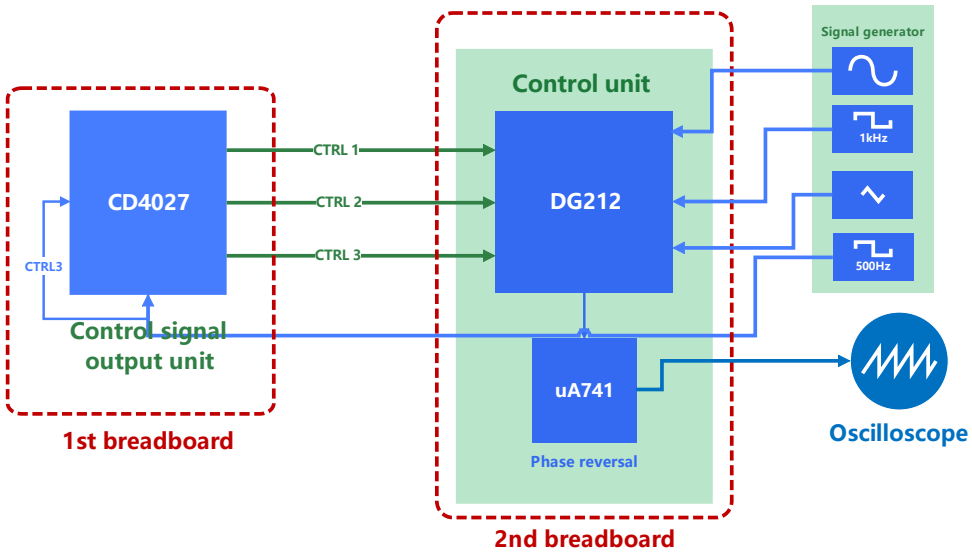

Figure 35: Optimized design scheme block diagram

Figure 35 intuitively presents the optimized circuit splicing scheme. During the circuit splicing process, since each CD4027 chip encompasses 2 JK flip-flops, I require 2 CD4027 chips for constructing the circuit.

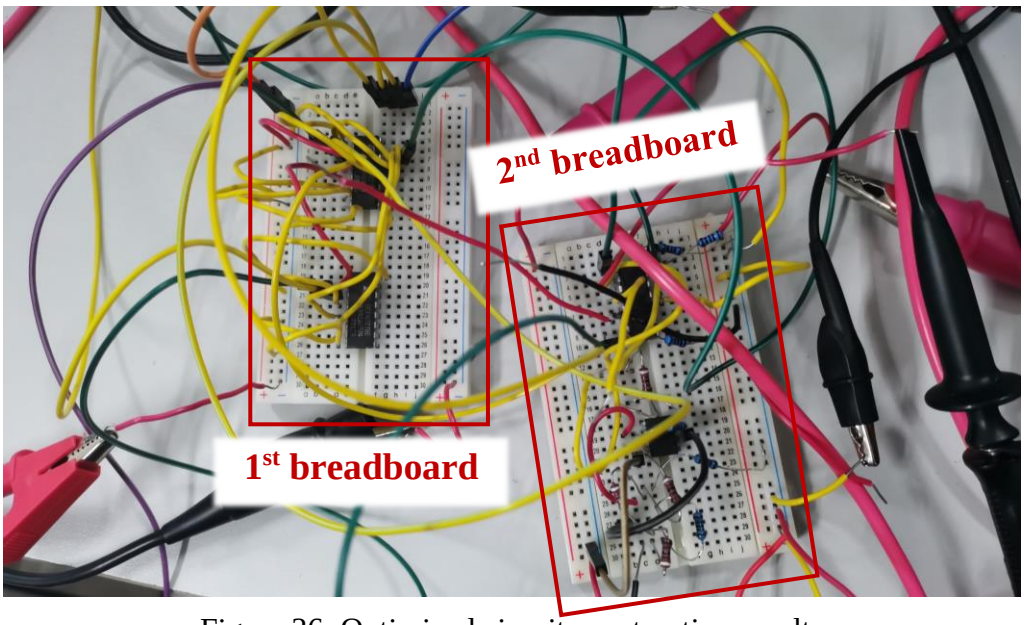

Figure 36: Optimized circuit construction results

Figure 36 displays the constructed outcome of my optimized circuit. It's evident that the circuit has undergone significant reduction.

3.4.3. Evaluation of the optimized scheme

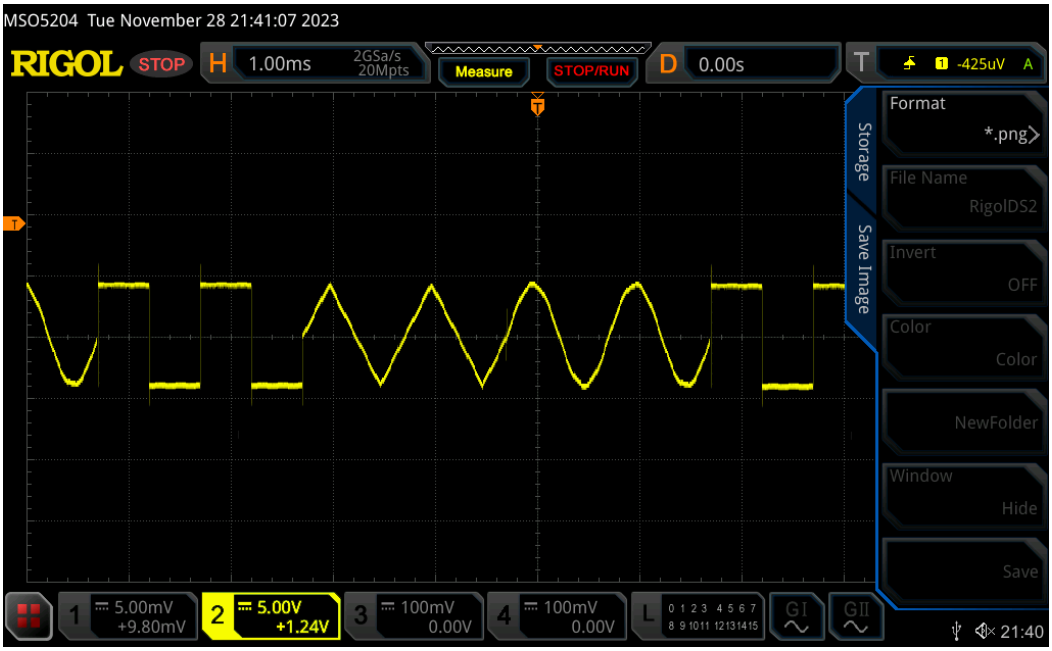

Figure 37: The waveform of the actual circuit

Figure 37 illustrates the waveform results obtained from our optimized circuit, indicating that the waveform switching is functioning correctly. The waveform exhibits an amplitude close to 5V and a period of 1ms, meeting the specified requirements.

4. Conclusion

Throughout this experiment, our team collaborated effectively to complete the circuit simulation design for the "Audio Signal Selector for Radio Stations" project, followed by individual experiments involving circuit construction.

This hands-on experience allowed me to solidify the theoretical knowledge acquired in class and apply it practically to a real project. I gained valuable insights into simulating circuits using software and then translating those simulations into physical breadboard setups. This project significantly enhanced my problem-solving skills and improved my ability to communicate within a team setting. Additionally, it broadened my understanding of electronic systems, identifying areas where further learning and exploration are required.

References

[1] Zhang Xinxian. Multisim 14 Electronic System Simulation and Design [M]. 2nd ed. Beijing: Machinery Industry Press, 2017. ISBN 978-7-111-57662-4.

[2] Wikipedia contributors. (2023, September 21). Schmitt trigger. In Wikipedia, The Free Encyclopedia. Retrieved 02:42, December 2, 2023, from https://en.wikipedia.org/w/index.php?title=Schmitt_trigger&oldid=1176359474.

Appendix 1:

Audio selection signal circuit diagram