Operational Amplifier Circuit

Team	Autumn, 2022
Module	**EE1616 Electronics Workshop**
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Introduction and aims:

To investigate the behavior and performance of **operational amplifiers**. To find the characteristics of Op-Amp through the lab. Further understand the functions of Op-Amp in the integrated circuits.

Task description:

1. Familiar with the operational amplifier we learned before. We need understand the inverting and non-inverting terminal, virtual short circuit, virtual open circuit, saturation, and amplifier region of Op-Amp.
2. Follow the lab tutorial. Connect with the Op-Amp and simulate it.
3. Compare the experimental results with the theory, find the phase shift and peak gap between $V_0, V_i \ and \ V\_$.

Experiment method:

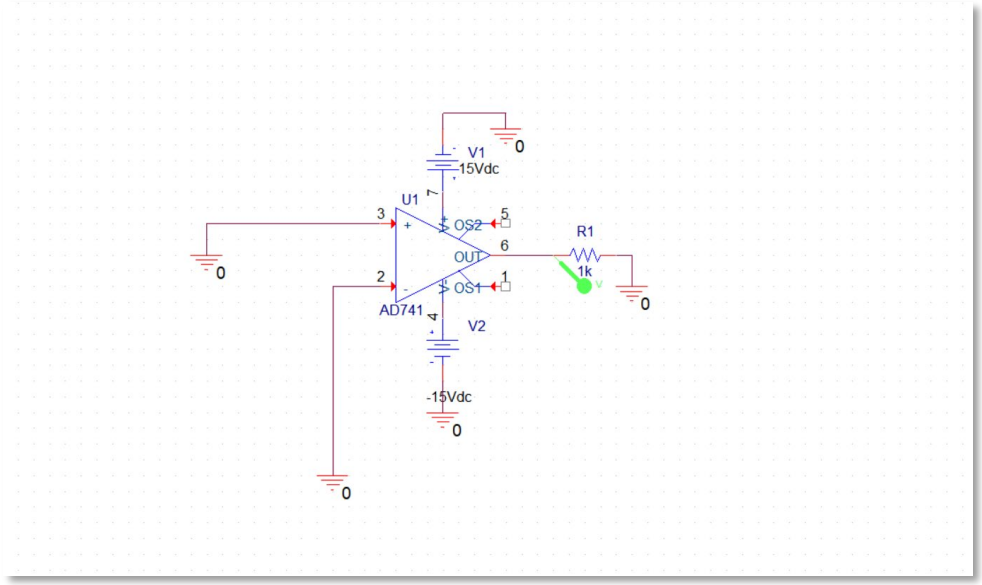
1. Review the characteristics of Op-Amps. **AD741** has 8 terminals, we need to know the functions of each terminal and we need use 5 of these terminals: 2,3,4,6,7.
2. Connect the Op-Amp with resistances or sources correctly. Pay attention we need add a resistance in the output terminal such that we can measure the value of output voltage.
3. Simulate the Op-Amp in the condition of inverting and non-

inverting terminal. Calculate the voltage gain and the phase shift.

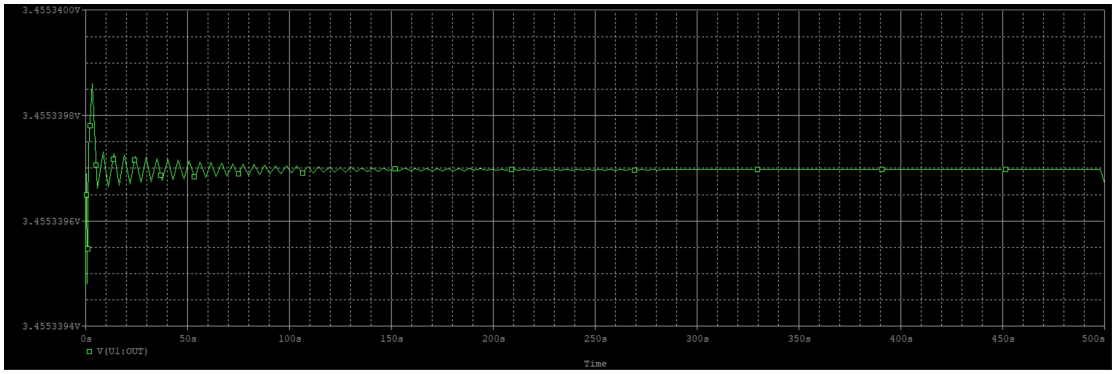
Result and observation:

1. Base operation and Use as a comparator

1.1.

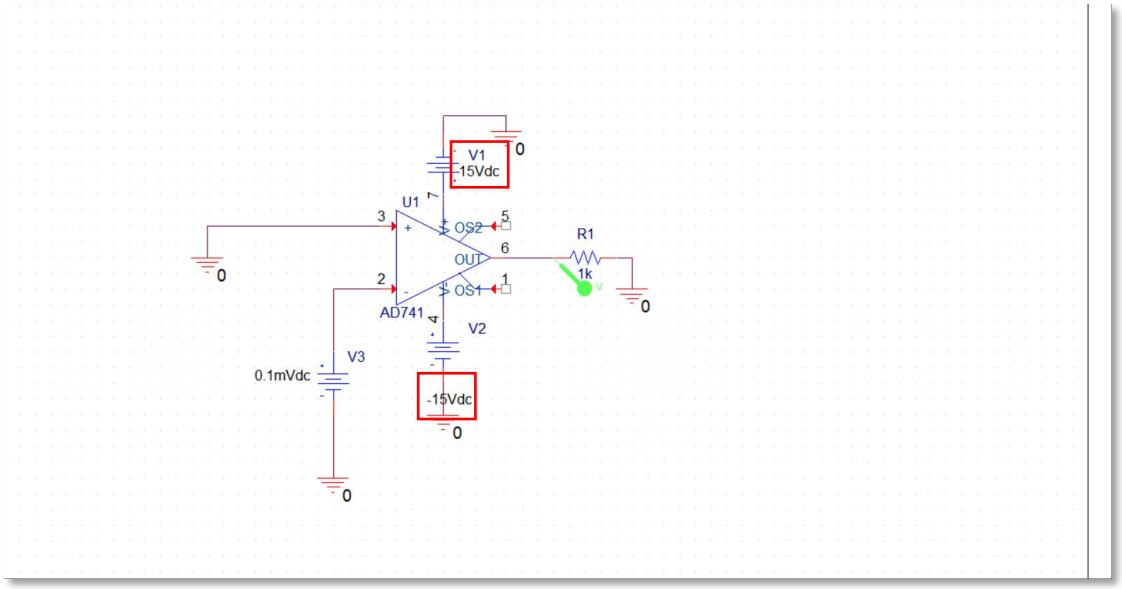


This is the circuit diagram.

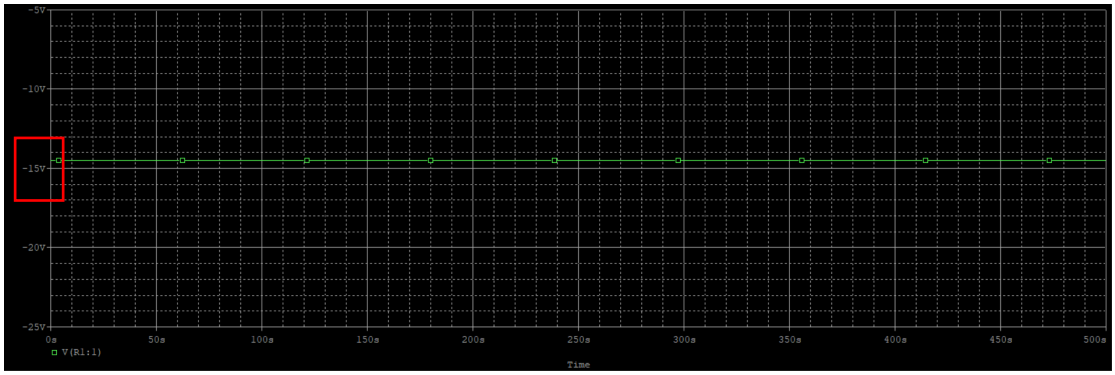


The simulation results. I set the time domain is 500s, so that the shock can be balanced regionally.

1.2.



This is the circuit diagram. This is the inverting input. I set the input is **DC voltage** and the value is **1 mV**.



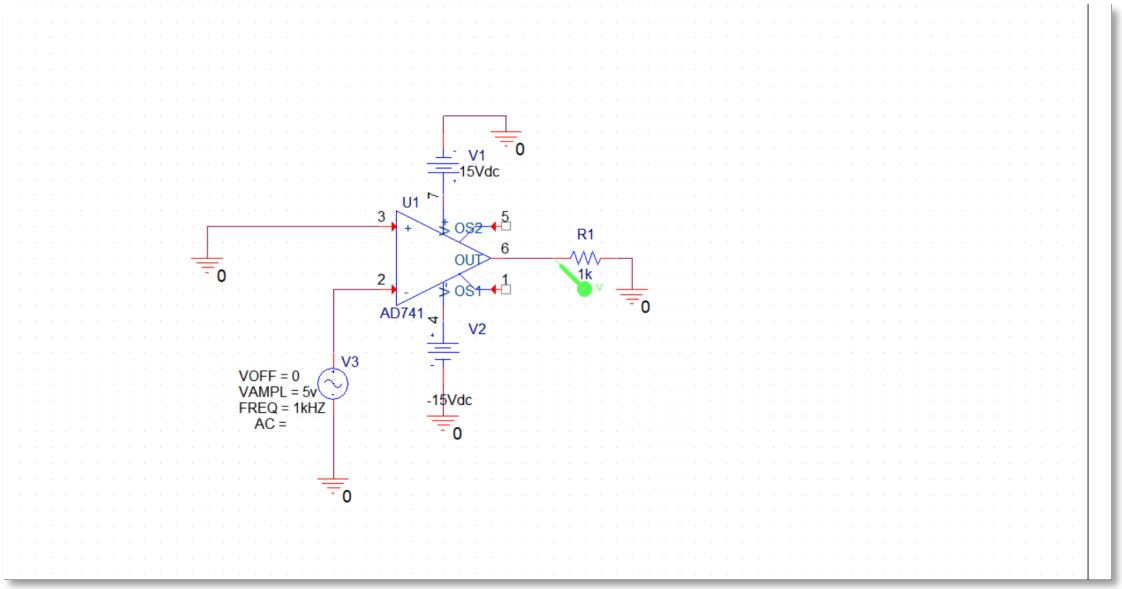
The positive supply and negative supply are +15V and -15V respectively. From the simulation result, I can find that the output voltage is nearly to 15V and no oscillation. Thus, I can assume that the Op-Amp is saturated. Due to the Op-Amp is in inverting input, the phase of output voltage is opposite to input voltage. Thus, the value of output voltage is negative value: -15V.

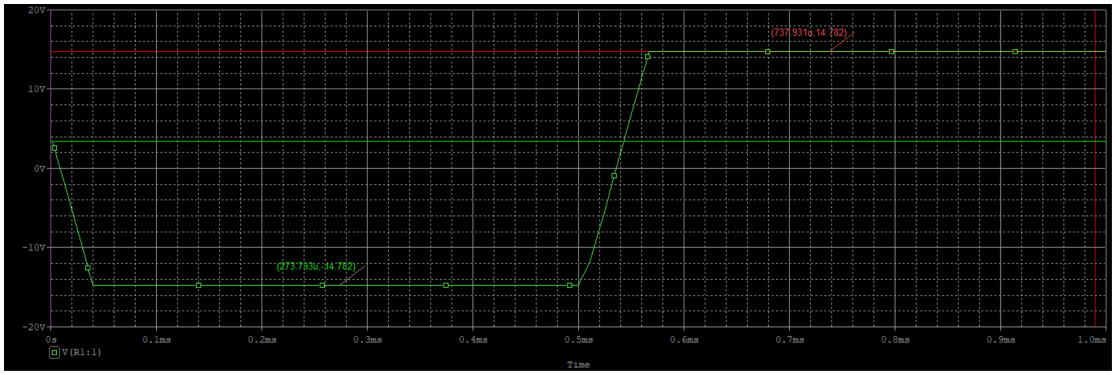
AD741 Series–SPECIFICATIONS (typical @ +25°C and ±15 V dc, unless otherwise noted)

Model	AD741C Min	AD741C Typ	AD741C Max	AD741 Min	AD741 Typ	AD741 Max	AD741J Min	AD741J Typ	AD741J Max	Units
OPEN-LOOP GAIN										
R_L = 1 kΩ, V_O = ±10 V							**50,000**	200,000		V/V
R_L = 2 kΩ, V_O = ±10 V	**20,000**	200,000		**50,000**	200,000					V/V
T_A = min to max R_L = 2 kΩ	**15,000**			**25,000**			**25,000**			V/V

Finally, I check the data of AD741 on the tutorial. The **open-loop gain is 200,000.** $200{,}000 \times 0.1mV = 20V$. Thus, I can verify that the Op-Amp is reach to saturation region.

1.3.

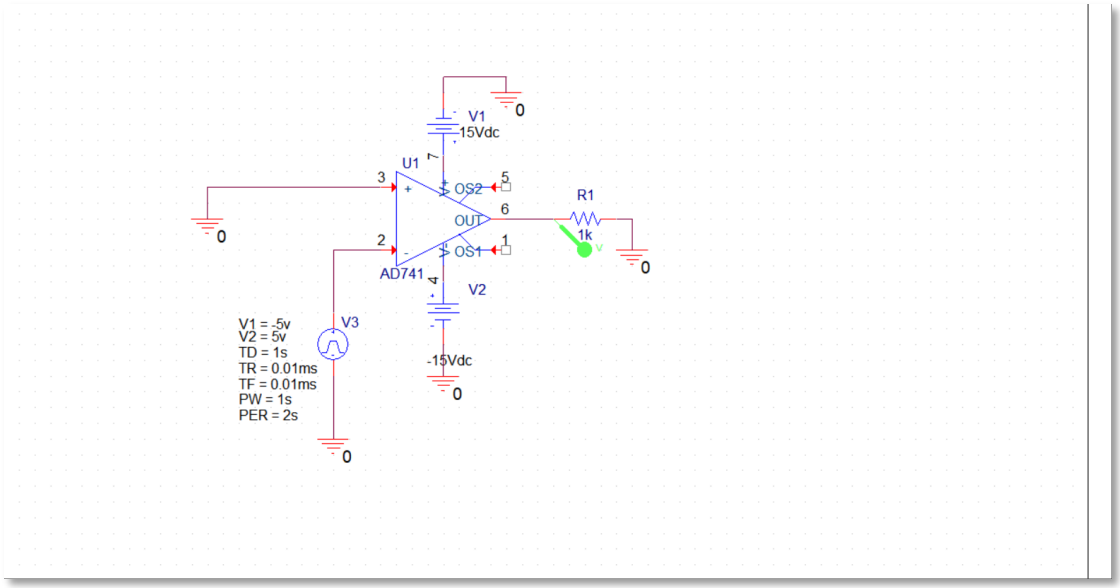




I set **VAMPL** is 5V, the frequency is 1kHZ. The input voltage is a sinusoid waveform. Thus, the output waveform should still be a

periodic one. Due to the Op-Amp can easily reach saturation, the output voltage is not a complete sinusoid waveform.

1.4.

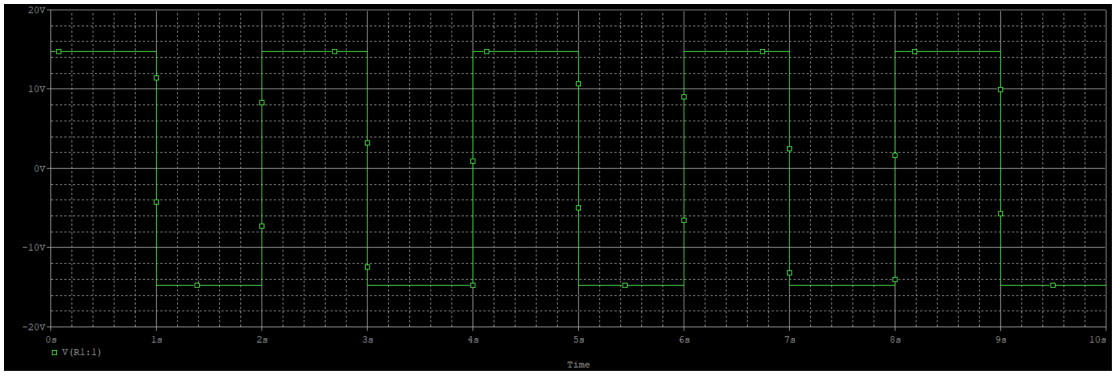


This is the circuit diagram of square wave input.

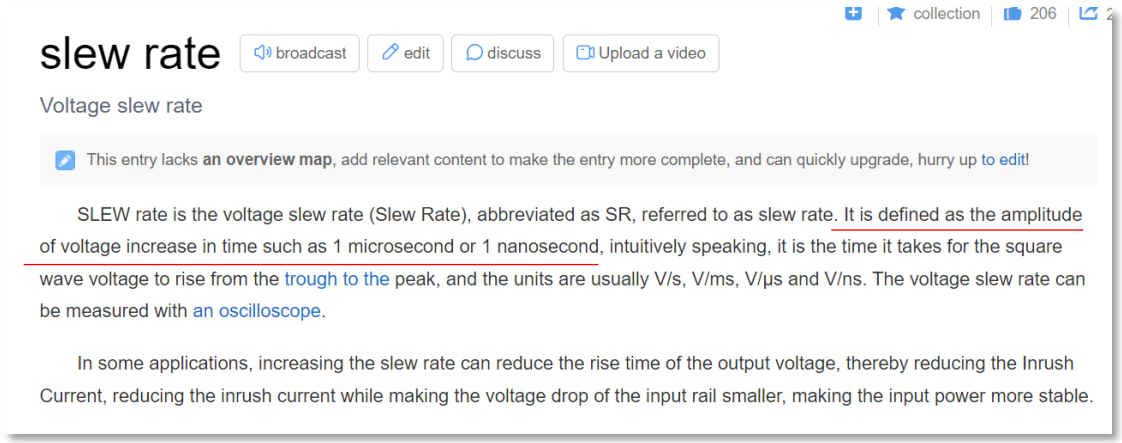
利用PSpice进行仿真时，用VPULSE产生方波，VPULSE在SOURSE库中，有七个参数：
V1：低电平，如-5V；
V2：高电平，如+5V；
TD：第一个脉冲相对于0时刻的延迟时间，一般为一个非零值，如1s，2s；
TR：脉冲上升时间，如果为方波，则为0s；
TF：脉冲下降时间，如果为方波，则为0s；
PW：脉冲宽度，为上升到V2后到下降前的宽度，即高电平宽度；
PER：脉冲周期，其值要大于TR+TF+PW，否则得到不想要的结果。
另外，PER如果不等于TR+TF+PW，则多出的部分其值为0；如果等于，则为一个标准的方波。

According to the information found. I set **V1 and V2** to +5V and -5V respectively. **TD** means time delay; the value is usually 1s. **TR** means time rise and **TF** means time fall. At first, I set to 0. However, the system reports an error during my simulation, the system tells me do not divide 0. Thus, I set the TR and TF are 0.01ms, it is a rather

small value, nearly to 0. **PW** means pulse width. I want to keep the high level for 1s, so I set the value of PW is 1s. **PER** means pulse period, and I set it to 2s.



This is the simulation result. The result is the same as my expected.

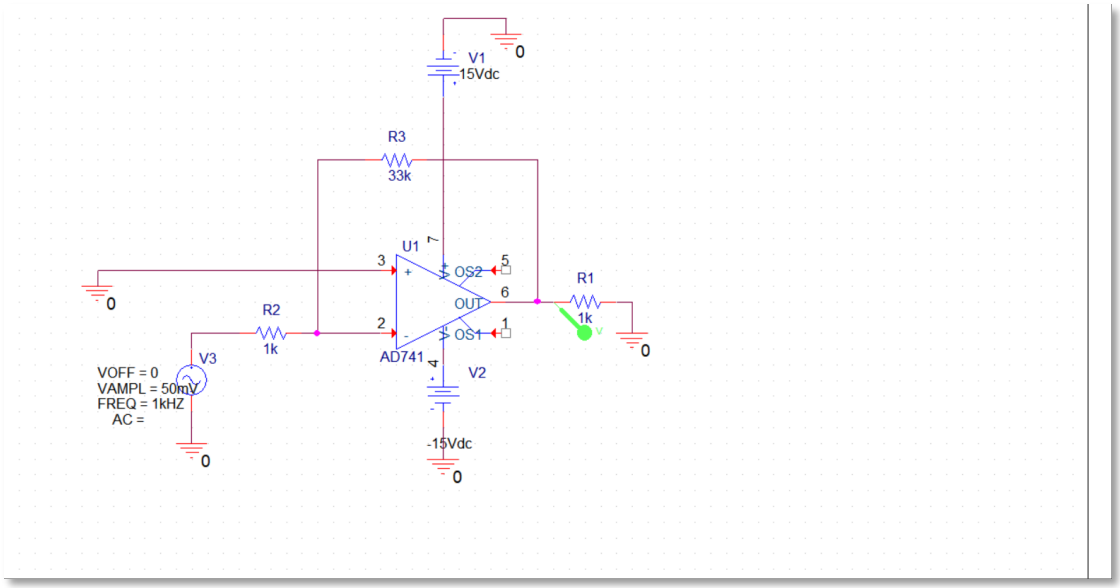


This is the definition of "**slew rate**". It is defined as the amplitude of voltage increase in time such as 1 microsecond or 1 nanosecond. Thus, the slew rate is

$$\frac{(15V-(-15V))}{0.01ms} = 3\ V/\mu s.$$

2. Use as Amplifiers

2.1. The inverting amplifier



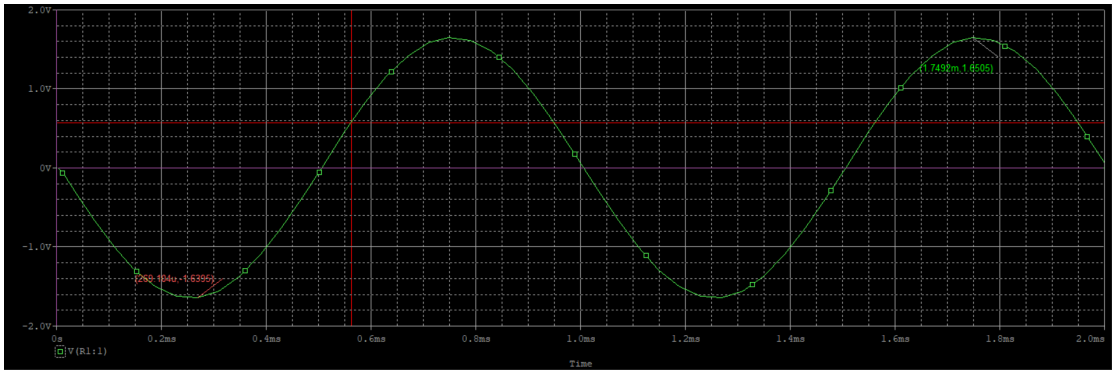


Fig. 1. The waveform of $\boldsymbol{V_0}$.

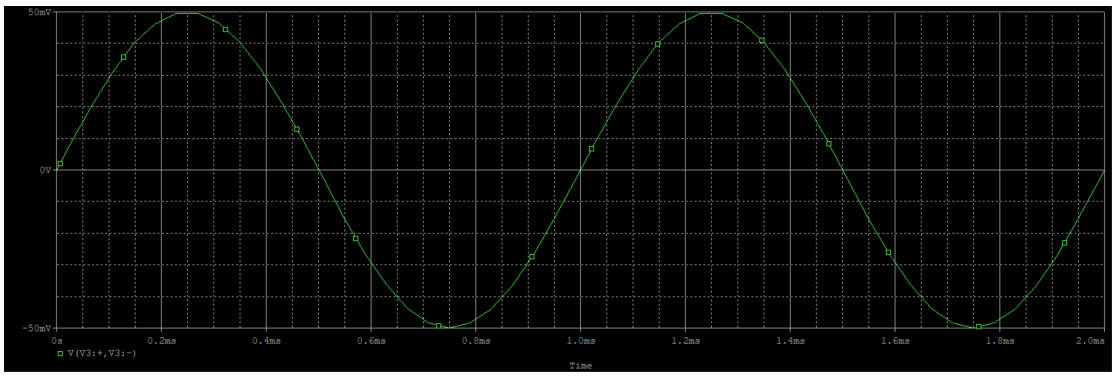


Fig. 2. The waveform of $\boldsymbol{V_i}$.

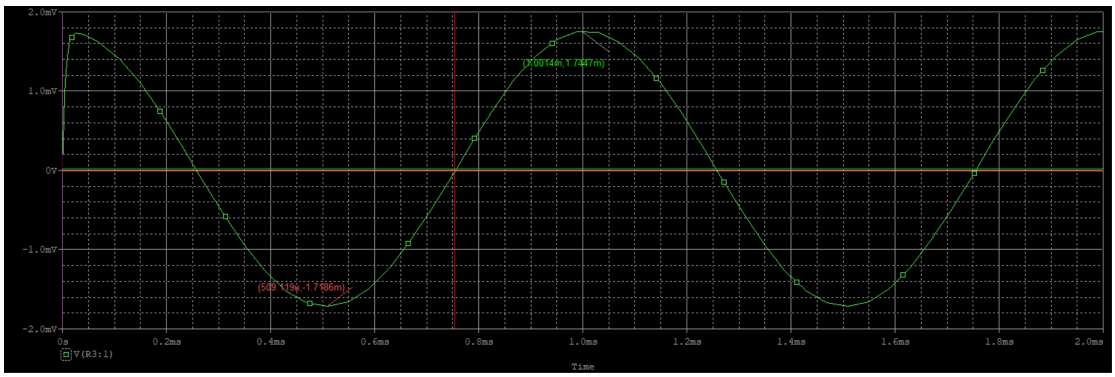
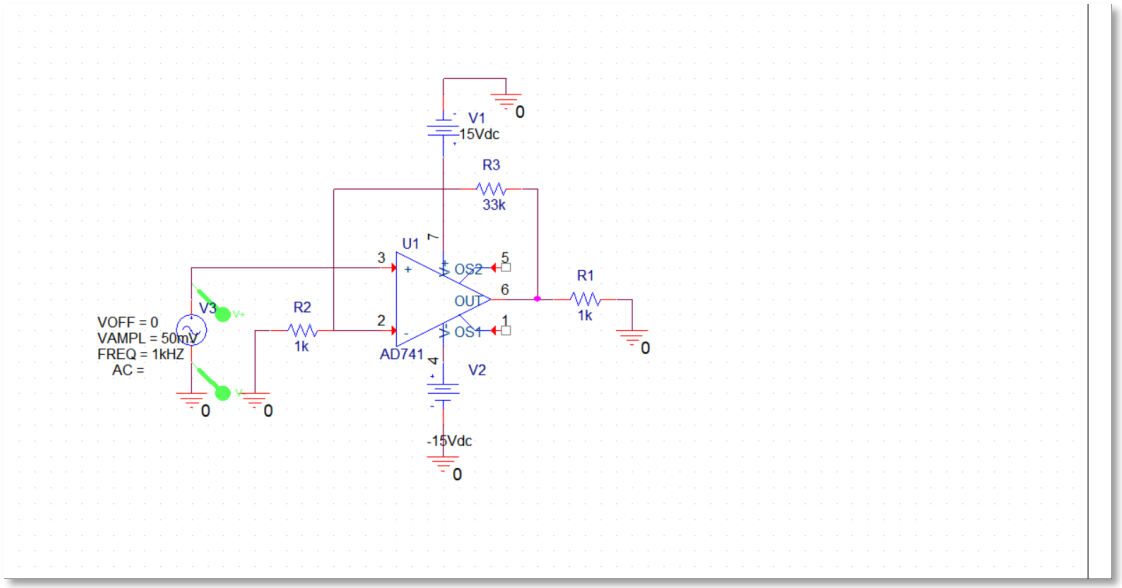


Fig. 3. The waveform of $\boldsymbol{V\_}$.

2.2. The non-inverting amplifier



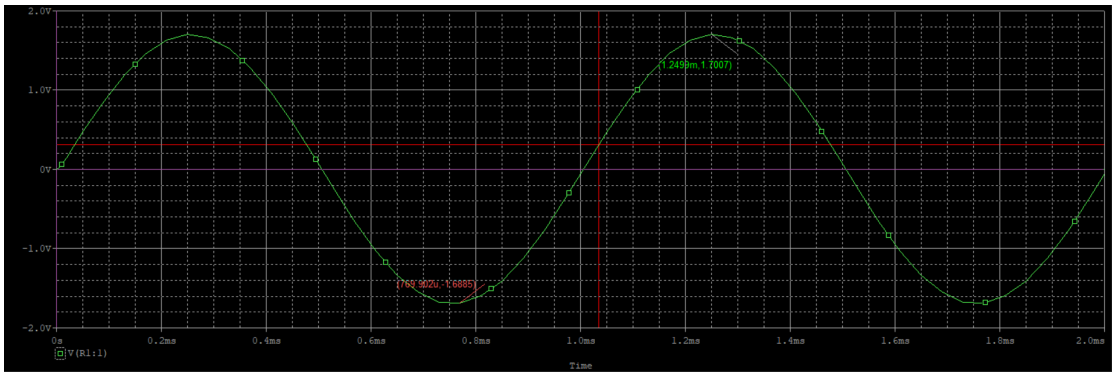


Fig. 4. The waveform of $\boldsymbol{V_0}$.

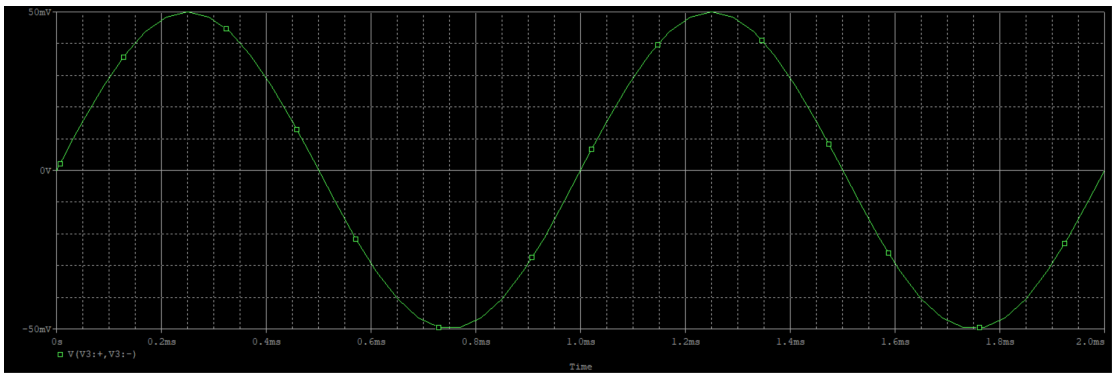


Fig. 5. The waveform of $\boldsymbol{V_i}$.

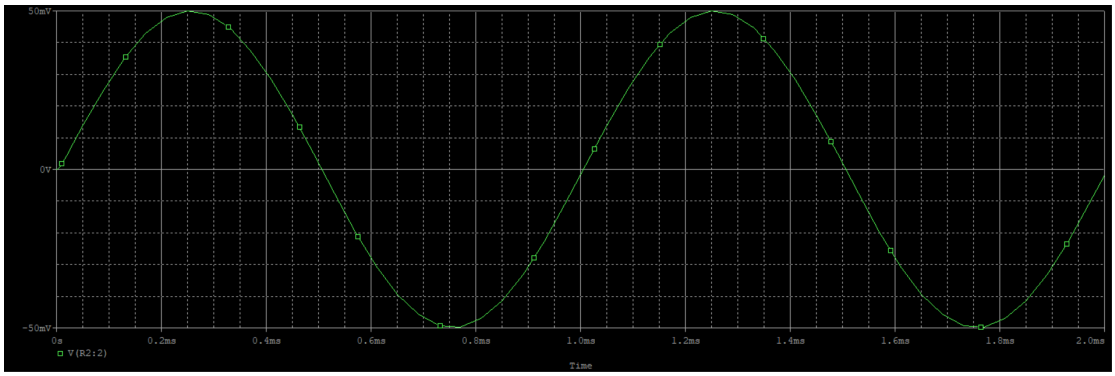


Fig. 6. The waveform of $\boldsymbol{V\_}$.

2.3.

In **inverting amplifier**, there exist a very important formula:

$$\frac{V_0}{V_i} = -\frac{R_3}{R_2}$$

In **non-inverting amplifier**, there also exist a formula:

$$\frac{V_0}{V_i} = 1 + \frac{R_3}{R_2}$$

In this situation, $\boldsymbol{R_2 = 1k\Omega, R_3 = 33k\Omega.}$

a) The part 2.1

The maximum value of $V_i = 50mV$.

$$V_0 = -\frac{33k\Omega}{1k\Omega} \cdot 50mV = -1.65V$$

After observing the figure 1, I can verify that the result is correct.

b) The part 2.2

The maximum value of $V_i = 50mV$.

$$V_0 = (1 + \frac{33k\Omega}{1k\Omega}) \cdot 50mV = 1.7V$$

After observing the figure 4, I can verify that the result is correct.

In part 2.1*,** it is inverting amplifier. Thus, the phase shift is $180°$, the input voltage is opposite to the output voltage. ***In part 2.2, it is non-inverting amplifier. Thus, the phase shift is $0°$, the input voltage is the same as the output voltage.

By observing the above waveforms, I can conclude that the results are consistent with the predictions.

2.4.

a) The part 2.1

Because this is inverting amplifier, $V_- = V_+$. The positive terminal is grounding, thus, V_- nearly to 0. From figure 3, I can find that the maximum value of V_- only a few millivolts. It shows that the

observation is consistent with the theory.

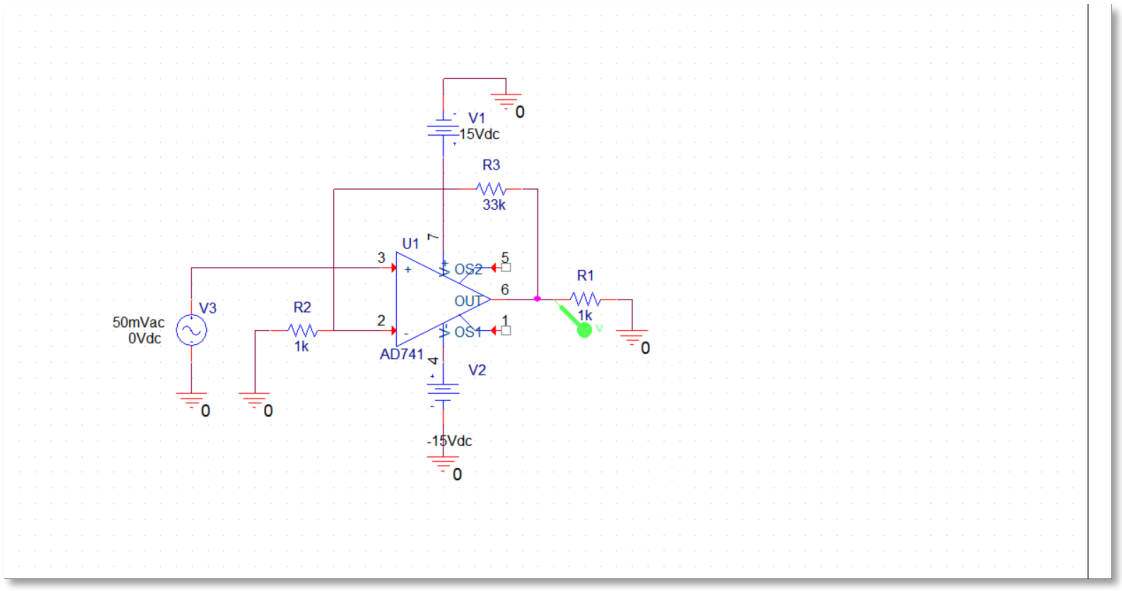
b) The part 2.2

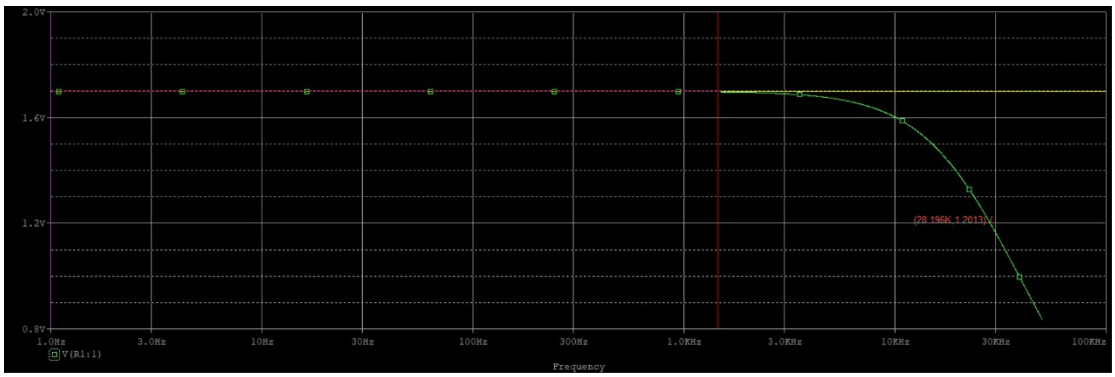
Because this is non-inverting amplifier, $V_- = V_+$. The maximum value of the positive terminal voltage is 50mV. Thus, the negative termina voltage should also be 50mV. It shows that the observation is consistent with the theory.

Since the internal resistance of the Op-Amp is very large, I can consider that **the current taken from the signal source** is close to 0.

3. Frequency Response

3.1.





The amplifier can be seen as a **low-pass filter**. When the frequency exceeds a certain value, the output voltage will drop. At 1kHz level, the maximum output voltage is 1.7007V. $1.7007 \times 0.707 = 1.2024V$. In the simulation results, I found the closest value to 1.2024 and marked. The cut-off frequency is 28.196kHz. Thus, the bandwidth frequency is **28.196kHz.**

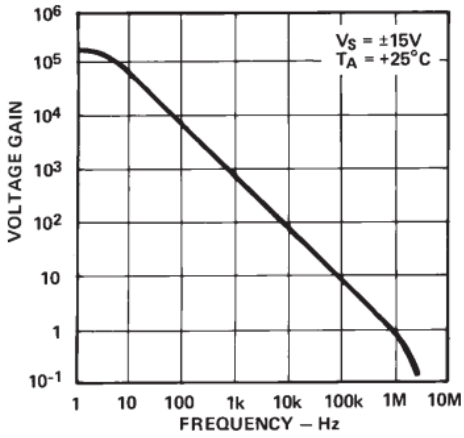


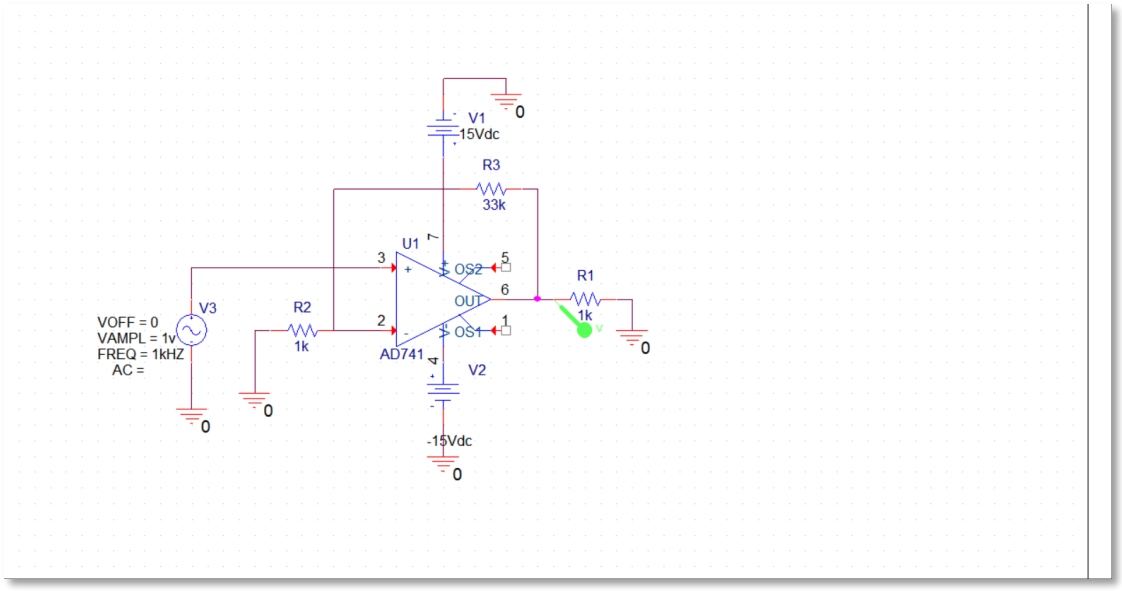
Figure 3. Open-Loop Gain vs. Frequency

This is the frequency response of open-loop gain. We can find that the output voltage decreases with the increase of input voltage frequency. It shows that the increase of frequency will lead to the decrease of gain, so the operational amplifier can be used as an **active low-pass filter**.

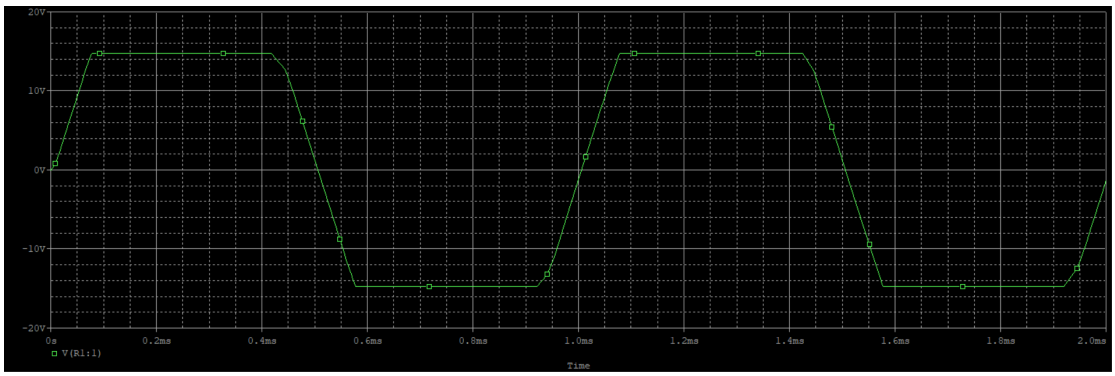
3.2.

Due to this is non-inverting amplifier. Therefore, V_0 *and* V_i are at **the same phase**.

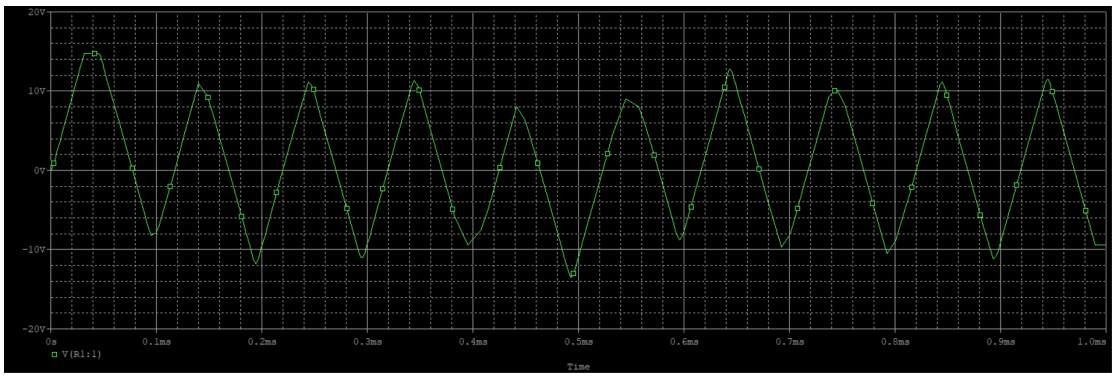
3.3.



This is the circuit diagram, and I set the VAMPL is 1V.



At **1kHz** level, this is the output waveform becomes distorted. Because the input voltage is too large, the Op-Amp sometimes reaches saturation. Therefore, the output voltage will be distorted.



At **10kHz** level, this is the output waveform becomes distorted.

Conclusion:

Due to Covid-19, we have to carry out the simulation lab of operational amplifier on PSPICE. In this lab, I simulate the inverting and non-inverting Op-Amp. I further understand the characteristics of Op-Amp and know how to simulate it on the software. By observing and commenting on the waveform results, we can verify the theoretical knowledge we learned in EE1618.