Exam Question Paper

College/ Institute	CEDPS		
Department	Electronic and Computer Engineering		
Exam Author(s)	Prof J. Stonham & Dr H Meng		
Module Code	EE1055		
Module Title	Digital Systems and Microprocessors		
Month	May	Year	2019
Paper Type	Full / ~~Re-sit~~		
Duration	3 Hours		
Question Instructions	Answer-ALL questions: Section A and B have equal marks		
Are Calculators Permitted?	Yes / ~~No~~		
Permitted Reference Materials	None		
Required Stationery	Please answer section A and section B using separate answer books		

SECTION A

1. Convert the following base 3 number 21022_3 to

   a) Decimal
   b) Binary
   c) 6, 4, 2, -3 weighted BCD.

[5 marks]

2. Devise a "2 in 4" code for Base 6 numbers and convert the base 6 number

   5142.35_6

   into your "2 in 4" code.

   How can this code be used for error detection?

[5 marks]

3. Use Truth Table Equivalence to determine whether the following equations are true or false.

   a) $\overline{A}B + ABC + BC = (A + B)(\overline{A} + C)(B + C)$

   b) $(A \oplus C) + (B \oplus C) + (A \oplus B) = 1$

[5 marks]

4. Obtain the MINIMAL 1st and 2nd Canonical forms of the following equation

   F = Σ (0, 1, 2, 3, 8, 9, 12)

   with Don't care inputs (13, 14, 15)

   [5 marks]

5. The following equation is in its minimal NOR form. Obtain its MINIMAL 1st Canonical (AND/OR/NOT) form.

$$F = \overline{(\overline{A+B}) + (\overline{\overline{A}+\overline{B}}) + (\overline{\overline{C}+D})}$$

   [5 marks]

6. A 4-bit shift register $Q_3Q_2Q_1Q_0$ has EXCLUSIVE-OR feedback. The feedback function is

$$I_0 = Q3 \oplus Q2$$

   If the initial state is 0001, what sequence of 4-bit numbers does the register generate when clocked?

   [5 marks]

7. Design a sequential circuit to continuously output in binary, the sequence

   0, 2, 4, 6, 7, 5, 3, 1 and repeat from 0

   Include a detailed block diagram in your answer and obtain any necessary logic functions in their MINIMAL forms.

   [5 marks]

8. Design a combinational logic system in its minimal 1st Canonical Form, which will convert 3-bit pure binary inputs into Gray code.

   [5 marks]

9. Programme the following function into a 16 to 1 multiplexer.

$$F = \Sigma (0, 1, 2, 4, 6, 9, 10, 12, 14)$$

Re-programme the same function into a two-layer system of 4 to 1 multiplexers.
Present you final answers in the form of circuit diagrams with all the inputs and outputs appropriately labelled.

[5 marks]

10. An incompetent engineer has produced the following circuit, which although it performs the function correctly, takes up too much silicon area and consumes excessive power. Redesign the circuit to obtain the best possible design in terms of power consumption, speed and size.

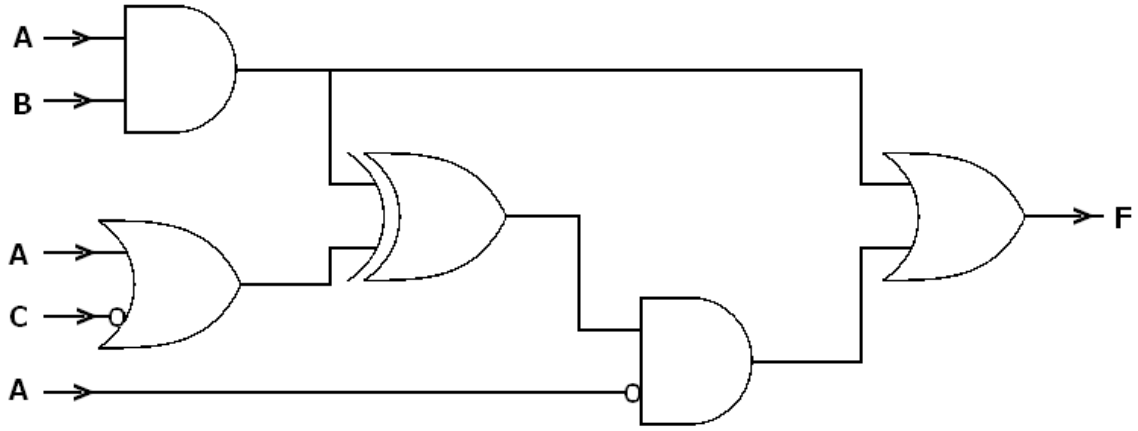


FIGURE Q10

SECTION B

11. Read the statements about the PIC16F877A microcontroller from the list below and judge it is true or false with a brief explanation.

    a) The Program Counter inside this PIC chip has 13 bits.
    b) The size of the code memory is 8k Bytes.
    c) The PICmicro instructions take up to 3 lines of code each.
    d) The size of the data memory is 512k bytes.
    e) It is a Von Neumann architecture.
    f) NOP instruction does nothing apart from generating a bit of delay.
    g) It has 35 instructions.
    h) It has 28 pins.
    i) STATUS register is used for monitoring the system and it has 8 bits.
    j) The BTFSC instruction is typically used for making programs run faster.

    [10 marks]

12. The piece of code below is written for a PIC16F877A chip in assembly language:

```
BSF     STATUS,5
CLRF    TRISB
BCF     STATUS,5
MOVLW   H'07'
MOVWF   PORTB
```

    a) With reference to the attached datasheet at the end of the question 15, write down the 14-bit binary machine code for each row of the code.

    [5 marks]

    b) Explain the meaning of each instruction and give the final value of the W register in the PIC microcontroller.

    [5 marks]

13. With reference to the attached instruction set (Datasheet 1), the following is a subroutine written for a PIC16F877A chip in assembly language:

```
DELAY   MOVLW    0x2F
        MOVWF    COUNT
LOOP    DECFSZ   COUNT,F
        GOTO     LOOP
        RETURN
```

a) Calculate the total number of PIC instructions that will be executed by calling this subroutine once.

[5 marks]

b) Assume that each PIC instruction takes 1μs to execute, except for CALL, RETURN and GOTO instructions that each take 2μs to execute. Calculate the total execution time that results from calling this subroutine once.

[5 marks]

14. The values in the data memory (8-bits registers) of a PIC microcontroller are stored in their two's complement form. Please give the hexadecimal and binary representations of the following decimal values in the data memory.

a) 60
b) -78
c) 45
d) -10
e) 98

[10 marks]

15.

a) What is meant by switch bounce and explain why it is a problem for a microcontroller system.

[4 marks]

b) A keypad as shown in FIGURE Q15 is to be interfaced to PORT A of a PIC microcontroller. Assume that the column pins (PA4..6) are inputs and the row pins (PA0..3) are outputs, describe (using words or a flowchart) how a subroutine can scan the keypad and return the ASCII value of any key pressed. If no key is pressed, a null character should be returned.

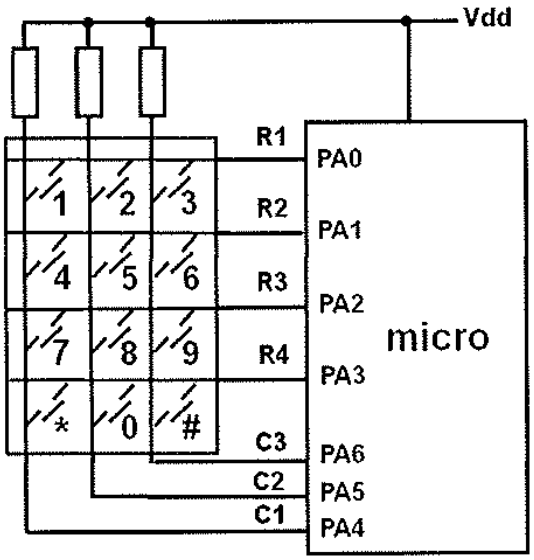


FIGURE Q15

[6 marks]

TABLE 15-2: PIC16F87XA INSTRUCTION SET

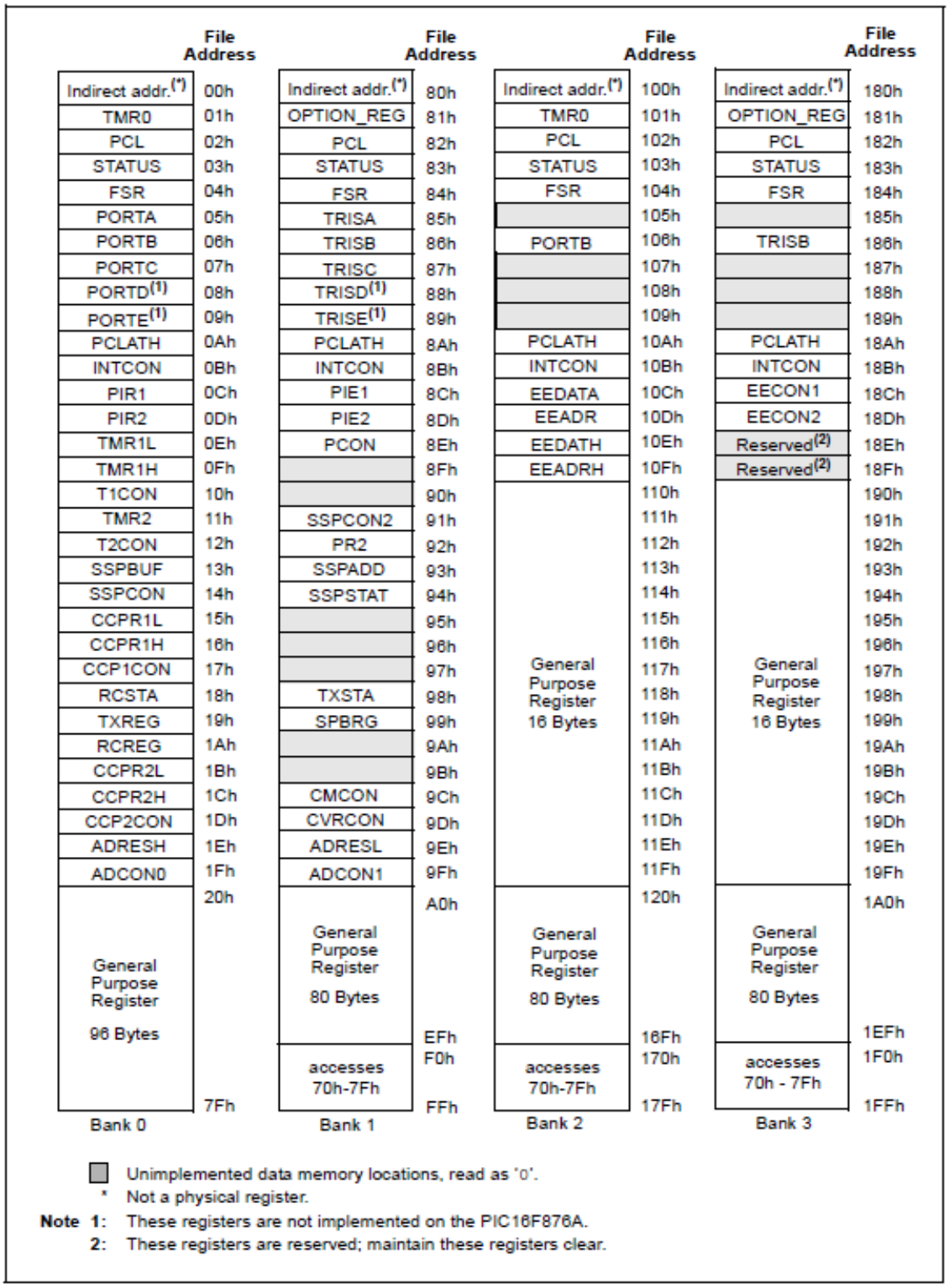
Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add Literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND Literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to Address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR Literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from Interrupt	2	00	0000	0000	1001		
RETLW	k	Return with Literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from Literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR Literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

FIGURE 2-3: PIC16F876A/877A REGISTER FILE MAP



Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: These registers are not implemented on the PIC16F876A.

2: These registers are reserved; maintain these registers clear.