

Sanjay Gandham

☎ (805)791-1805 | @ sanjay.gandham@ucf.edu | 🔗 LinkedIn | 📍 Orlando, Florida

EDUCATION

University of Central Florida

Orlando, Florida

Ph.D, Computer Engineering, GPA: 3.94

Aug 2019 – Apr 2025 (Expected)

Relevant Coursework: FPGA Design, Advanced Computer Arch., Parallel Computer Arch., Attacks and Defenses in Secure Arch., Intro to Neural Networks, 3D Computer Vision, Advanced AI, ML, and Design and Analysis of Algorithms

Jawaharlal Nehru Technological University

Hyderabad, India

B.E, Computer Engineering GPA: 9.23/10

Aug 2015 – May 2019

EXPERIENCE

AMD

Orlando, Florida

Research Intern

May 2024 – Aug 2024

Developed AI-assisted tools to perform RTL PPA optimizations automatically on arithmetic datapaths.

Synopsys

Sunnyvale, California

Machine Learning Research Intern

May 2023 – Aug 2023

Designed, implemented, and fine-tuned a novel Transformer and Graph Neural Network model for fast ASIC Post-PnR QoR Evaluation directly from RTL using Pytorch, and DGL libraries.

SiFive

San Mateo, California

CPU Design Engineer Intern

May 2022 – Aug 2022

Primarily worked on the Load/Store Unit of SiFive's highest performing scalar and vector processors.

- Contributed to the microarchitecture and RTL of cache allocation policy for vector processors
- Wrote RTL design, using Chisel HDL, for a subset of cache-block prefetch instructions from RVA22 extension

University of Central Florida

Orlando, Florida

Graduate Teaching Assistant

Aug 2021 – Present

Tutored and graded for the undergraduate courses related to Hardware Description Languages, Digital Design, FPGA and CAD for VLSI in the Department of Electrical and Computer Engineering.

Graduate Research Assistant

Aug 2019 – Present

- Designed the micro-architecture of a custom hardware accelerator for Graph Neural Network workloads, implemented using Chisel HDL, and prototyped it on AMD Xilinx U200 Acceleration card.
- Worked as part of an 8-member team on a 3-year-long project and designed RTL modules for FPGA-assisted crash consistency for secure Non-Volatile Memory on Intel Stratix 10 Development kit funded by DARPA.

SELECTED PUBLICATIONS (FULL LIST [↗](#))

- **Sanjay Gandham**, Lingxiang Yin, Mingjie Lin, Hao Zheng, "SCALE: A Structure-Centric Accelerator for Message Passing Graph Neural Networks", in Proceedings of International Symposium on Microarchitecture (MICRO), 2024
- **Sanjay Gandham**, Joe Walston, Sourav Samanta, Lingxiang Yin, Hao Zheng, Mingjie Lin, Stelios Diamantidis", CircuitSeer: RTL Post-PnR Delay Prediction via Coupling Functional and Structural Representation", in Proceedings of 43rd International Conference on Computer-Aided Design (ICCAD), 2024
- **Sanjay Gandham**, Lingxiang Yin, Hao Zheng, and Mingjie Lin, "SAGA: Sparsity-Agnostic Graph Convolutional Network Acceleration with Near-optimal Workload Balance", in Proceedings of 42nd International Conference on Computer-Aided Design (ICCAD), 2023

AWARDS & ACHIEVEMENTS

UCF Trustees Doctoral Fellowship: A Scholarship that covers full tuition and a \$100,000 stipend over 4 years awarded to one doctoral student of a department in 2019

AMD Graduate Research Fellowship: Recipient of the 2023 Fellowship in the ECE department at UCF, with a \$35,000 stipend, dedicated to advancing research in AI acceleration and High-Performance Computing

SKILLS

Programming: Verilog, C, C++, Python, Java, Scala, Chisel HDL