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Declaration:
This report was written entirely by the author, except where stated otherwise. The source of any material not created by the author has been clearly referenced. The work described in this report was conducted by the author, except where stated otherwise.

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1. Introduction:

The RISC-V 32-bit single-cycle processor is a fundamental and straightforward implementation of the RISC-V instruction set architecture (ISA), tailored to execute one complete instruction per clock cycle. This design is pivotal in understanding the essential components and functioning of a processor. In this architecture, all the key stages of instruction execution—fetching, decoding, executing, memory access, and writing back results—are accomplished within a single clock cycle. This simplicity in design makes the processor easier to analyze, build, and debug, making it a preferred choice for educational purposes and early-stage processor design.

The processor architecture incorporates essential components such as the instruction fetch unit to retrieve instructions from memory, the decode unit to interpret these instructions, the arithmetic logic unit (ALU) to perform computations, and memory access components to handle data read and write operations. The single-cycle approach eliminates the need for complex pipelining or multi-cycle control logic, ensuring that every instruction flows through the system without interruptions.

However, the simplicity of the single-cycle processor comes with trade-offs. Since every instruction, regardless of complexity, must complete in one clock cycle, the cycle time is determined by the longest instruction. This constraint can lead to inefficiencies, particularly for operations that require less time to execute, as the entire processor must synchronize to the slowest operation. Despite this limitation, the single-cycle design serves as a critical stepping stone for learning and prototyping, allowing designers to grasp the fundamentals of processor operations before advancing to more complex architectures like multi-cycle or pipelined processors.

The RISC-V 32-bit single-cycle processor exemplifies the modular and extensible nature of the RISC-V ISA. It provides a foundational framework for understanding core computational principles, enabling both students and professionals to experiment with and optimize designs. Its open and royalty-free nature further enhances its accessibility, fostering innovation and collaboration across academia and industry. This processor is not just a learning tool but also a testament to the simplicity and power of the RISC-V architecture, paving the way for more sophisticated processor designs.

1.1 Block Diagram of RISC V processor:

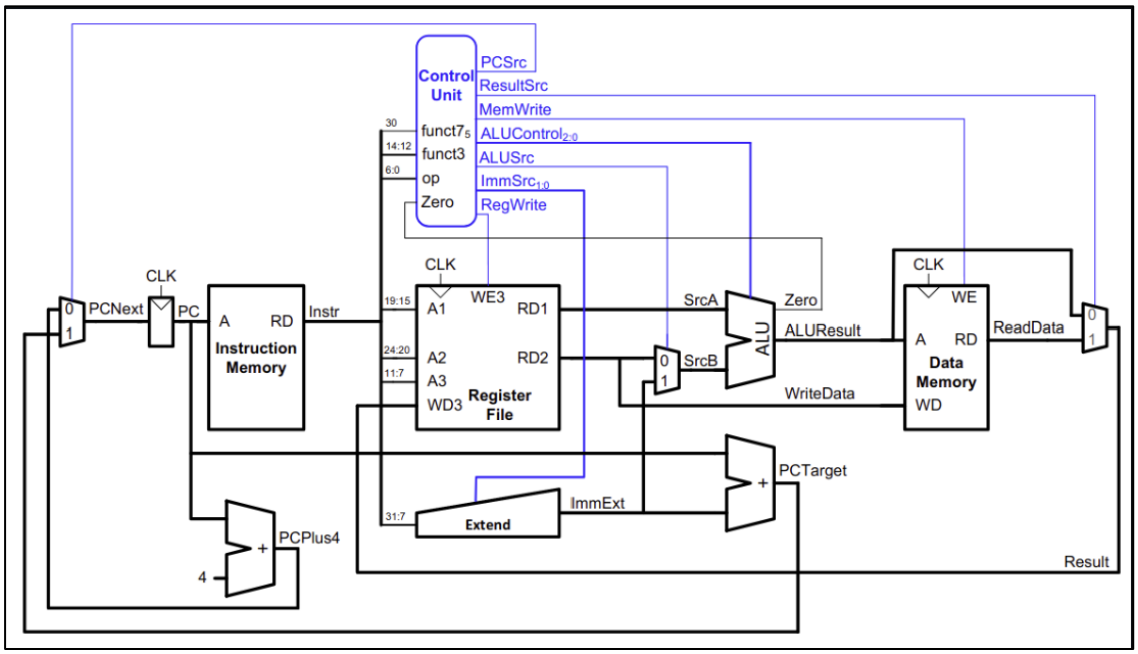


Fig.1

2. Functionality of each block:

2.1 Program Counter (PC):

The **PC** is a register that holds the address of the next instruction to execute. At the beginning of each clock cycle, the value in the PC is sent to the instruction memory to fetch the instruction. Depending on the control logic, the PC is updated either to the next sequential instruction (PC + 4) or to a branch target address, allowing conditional jumps.

2.2 Instruction Memory:

This block stores the program's instructions. The address from the PC is used to fetch the current instruction, which is then sent to the control unit and other components. Each instruction contains fields for opcode, source/destination registers, and immediate values.

2.3 Control Unit:

The control unit is responsible for decoding the fetched instruction and generating control signals for the processor's operations. Based on the opcode and function codes (funct3 and funct7), it determines the type of operation (e.g., ALU computation, memory access, or branch) and sets the necessary control signals, such as **RegWrite**, **ALUSrc**, **MemWrite**, and **PCSrc**.

2.4 Register File:

The register file consists of 32 general-purpose registers. It has two read ports and one write port, allowing two source operands to be read simultaneously and one destination register to be updated. The control signal **RegWrite** enables writing back results from the ALU or data memory to the destination register.

2.5 Immediate Extension Unit:

This block extracts immediate values from instructions and extends them to 32 bits, either by sign-extension or zero-extension, as required. The extended immediate value is often used in ALU operations or branch address calculations.

2.6 Arithmetic Logic Unit (ALU):

The ALU performs arithmetic and logical operations on the operands provided by the register file or the immediate value. The specific operation (e.g., addition, subtraction, AND, OR) is determined by the **ALUControl** signal. The ALU produces a result and a **Zero** flag, which indicates if the result is zero (used in branch decisions).

2.7 Data Memory:

The data memory block handles load and store operations. If the instruction is a memory access operation, the ALU result serves as the memory address. Data can either be read from memory and sent to the register file or written to memory based on the control signals **MemWrite** and **ResultSrc**.

2.8 Multiplexers (Mux):

Multiplexers select one input from multiple sources based on control signals:

- **2.8.1 SrcB Mux:** Chooses between a register value or an immediate value as the second operand for the ALU.
- **2.8.2 ResultSrc Mux:** Chooses between the ALU result or data memory output to write back to the register file.
- **2.8.3 PCSrc Mux:** Chooses between the sequential address (PC + 4) or the branch target address as the next value of the PC.

2.9 Branch Logic and Target Calculation:

For branch instructions, the branch target address is computed by adding the sign-extended immediate value to the current PC. If the branch condition is met (e.g., ALU Zero flag), the **PCSrc** signal directs the PC to update with the branch target.

3. Pipelining Concept in Processors:

Pipelining is a technique used in processor design to improve instruction throughput by overlapping the execution of multiple instructions. Instead of completing one instruction before starting the next, the processor is divided into stages, such as Fetch, Decode, Execute, Memory Access, and Write-Back. Each stage works on a different instruction simultaneously, allowing multiple instructions to be in different phases of execution within a single clock cycle.

For example:

- **Stage 1:** The first instruction is fetched.
- **Stage 2:** The second instruction is decoded while the first instruction is executed.
- **Stage 3:** The third instruction is fetched while the second is decoded and the first accesses memory.

This overlapping of stages increases the instruction throughput, as a new instruction is completed in every clock cycle after the pipeline is filled. However, it introduces challenges such as data hazards (dependency between instructions), control hazards (branches), and structural hazards (resource conflicts).

4. Functionality of the Single-Cycle Processor in the Diagram:

The single-cycle processor shown in the diagram does not implement pipelining. Instead, it completes all five stages of instruction execution—Fetch, Decode, Execute, Memory Access, and Write-Back—within one clock cycle. While this simplicity makes the design easier to understand and implement, it is less efficient because the cycle time is dictated by the slowest instruction. For instance:

- Memory access instructions (load/store) involve multiple steps, such as address computation and data transfer, requiring more time compared to ALU-only operations.
- This forces all instructions to operate at the speed of the slowest instruction, reducing overall efficiency.

Despite these limitations, the single-cycle design is valuable for understanding fundamental processor concepts. It forms the basis for more advanced architectures like multi-cycle and pipelined processors, which improve performance by addressing these inefficiencies.

In this diagram, the processor:

1. Fetches the instruction from memory using the PC.
2. Decodes the instruction and generates control signals.
3. Reads data from registers or extends immediate values.
4. Executes the operation using the ALU or calculates the memory address.
5. Accesses memory if needed and writes the result back to the register file.
6. Updates the PC for the next instruction, either sequentially or based on a branch.

This design provides a complete overview of how a basic processor executes instructions and sets the stage for more sophisticated optimizations.

5. Instruction Type Summary:

Instruction Type:

The RISC-V instruction set architecture (ISA) groups instructions into various types based on their format and functionality. Each type has a specific encoding pattern. The five types mentioned are:

1. **R-type:** Instructions that perform register-to-register operations.
2. **I-type:** Instructions that use immediate values as operands or access memory (load).
3. **S-type:** Instructions for storing data from a register to memory.
4. **B-type:** Branch instructions for conditional jumps based on comparisons.
5. **J-type:** Jump instructions for altering the program flow to a specific address.

Fig.2

Instruction Type	All Possible Instructions	Instructions Implemented
R-type	ADD, SUB, SLL, SLT, SLTU, XOR, SRL, SRA, OR, AND, MUL, DIV, REM	ADD, SUB, SLL, SLT, SLTU, XOR, SRL, SRA, OR, AND
I-type	ADDI, SLLI, SLTI, SLTIU, XORI, SRLI, SRAI, ORI, ANDI, LB, LH, LW, LBU, LHU, LUI, AUIPC	ADDI, SLLI, SLTI, SLTIU, XORI, SRLI, SRAI, ORI, ANDI, LB, LH, LW, LBU, LHU, LUI, AUIPC
S-type	SB, SH, SW	SB, SH, SW
B-type	BEQ, BNE, BLT, BGE, BLTU, BGEU	BEQ, BNE, BLT, BGE, BLTU, BGEU
J-type	JAL, JALR	JAL, JALR

6. All Possible Instructions:

This column lists all the instructions defined in the RISC-V ISA for each type. These are standard instructions supported by the architecture.

6.1. R-type (Register-to-Register Operations):

- Instructions like ADD, SUB, MUL perform arithmetic operations.
- AND, OR, XOR are logical operations.
- SLL, SRL, SRA perform shift operations.
- SLT, SLTU compare values for "set less than" results.

6.2. I-type (Immediate and Load Operations):

- Arithmetic/logical operations with immediate operands (ADDI, ANDI, ORI, etc.).
- Shift instructions (SLLI, SRLI, SRAI).
- Load instructions for memory access (LB, LH, LW, LBU, LHU).
- LUI and AUIPC help construct immediate values or update the PC.

6.3. S-type (Store Instructions):

- Store operations write register values to memory (SB, SH, SW).

6.4. B-type (Branch Instructions):

- Conditional branch instructions like BEQ, BNE compare register values for equality/inequality.

- BLT, BGE, BLTU, BGEU compare for less/greater (signed/unsigned).

6.5. J-type (Jump Instructions):

- JAL (jump and link) updates the PC to a target address while saving the return address.
- JALR (jump and link register) computes the target address dynamically based on a register value.

Observations:

1. The design implements a wide range of instructions, including arithmetic, logical, memory access, and branching operations, ensuring functionality for general-purpose computation.
2. Certain instructions, like multiplication (MUL) and division (DIV), are omitted in this design. This may be due to the processor being a simplified implementation targeting specific use cases.
3. The implemented set covers a complete minimal instruction set necessary for running basic programs and operating systems, adhering to the RISC-V philosophy of simplicity and modularity.

7. RTL Design Flow:

As shown in the Fig. We coded the source files to the design along with the constraint file. We resolved the errors that get encountered using reference code from GitHub. The GitHub link for our RISC-V project- **(https://github.com/Gandhamani/RISC-V-32-Single-cycle-Processor)**

Fig. 3

The **RTL (Register Transfer Level) design flow** for a RISC-V processor follows a structured process to design, simulate, and implement a processor. This flow ensures the processor functions as per the RISC-V ISA specifications. Below are the main steps:

7.1. Specification and ISA Definition:

- Define the functionalities of the processor based on the RISC-V ISA (e.g., supported instruction set types like R-type, I-type, etc.).
- Determine the architectural specifications, including the number of registers, datapath width (e.g., 32-bit), and memory size.

7.2. Microarchitecture Design:

- Design the architecture of the processor. This includes:
- Defining key components: Program Counter (PC), ALU, Control Unit, Register File, Instruction Memory, and Data Memory.
- Determining the data path flow (single-cycle, multi-cycle, or pipelined).

7.3. RTL Coding :

- Use a hardware description language (HDL) like Verilog or VHDL to describe the functionality of the processor.
- Develop modular blocks for:
- **Datapath:** Implements the core execution flow, including arithmetic/logic operations, memory access, and branch/jump instructions.
- **Control Unit:** Generates control signals based on the opcode and instruction format.
- **Pipeline Stages (if pipelined):** Divide the datapath into stages for instruction fetching, decoding, execution, memory access, and write-back.

7.4. Simulation and Debugging:

- Simulate the RTL code using testbenches to verify:
- Instruction execution.
- Correctness of arithmetic/logical operations, memory accesses, and branching.
- Fix functional bugs identified during simulation.

7.5. Synthesis:

- Convert the RTL design into a gate-level netlist using synthesis tools.
- Map the design onto target technology libraries, optimizing for speed, area, and power.

7.6. Physical Design:

- Transform the gate-level netlist into a layout for fabrication.
- Ensure timing, power, and signal integrity meet the design constraints.

7. 7. Verification:

- Perform functional, timing, and formal verification to ensure the design matches the specifications.

8. Adding Constraints File:

his constraints file defines the physical pin assignments, I/O standards, and timing constraints for a digital design implemented on an FPGA. Key elements are as follows:

1. **Clock and Reset Signals**:
    a. The clock signal is assigned to pin P16 and adheres to the LVCMOS33 standard, with a defined clock period of 10 ns.
    b. The reset signal is assigned to pin P17 and adheres to the LVCMOS33 standard. It is declared as a false path to prevent it from interfering with timing analysis.
2. **Data Signals**:
    a. Signals such as DataAdr and WriteData are assigned to individual pins (e.g., P18, P19, etc.), supporting a 32-bit data width. The LVCMOS33 standard is applied to ensure signal integrity and compatibility.
3. **Timing Constraints**:
    a. Input and output delays are set relative to the clock signal to define the maximum and minimum data arrival and departure times. These constraints guide the timing analysis tools to verify the design's timing closure.

4. **Power Optimization**:
    a. Power modes are defined for specific blocks (e.g., my_block is set to LowPower) to optimize power consumption during operation.
5. **Clock Gating**:
    a. Unused blocks are disabled through clock gating (e.g., unused_block), ensuring that no unnecessary power is consumed by inactive regions of the design.
6. **Expandability**:
    a. The file structure allows for easy additions of new signals, ensuring flexibility as the design evolves. For example, additional data or control signals like MemWrite and Result are already partially assigned for outputs and can be extended.

This constraints file ensures proper physical implementation and timing behavior while considering power optimization for specific modules. It can serve as a foundation for more complex designs requiring detailed pin management and performance tuning.

- ***Working Code:***
  Refer the Github link for the code: - https://github.com/Gandhamani/RISC-V-32-Single-cycle-Processor.

9. Pipelining in the RTL Design Flow:

Pipelining is implemented to improve the processor's throughput by overlapping the execution of multiple instructions. Here's how it's integrated into the RTL design flow:

9.1. Dividing the Processor into Pipeline Stages:

The processor's operation is divided into five primary pipeline stages:

- **IF (Instruction Fetch):** Fetch the instruction from the instruction memory.
- **ID (Instruction Decode):** Decode the instruction and read operands from the register file.
- **EX (Execute):** Perform ALU operations or calculate memory addresses for load/store instructions.
- **MEM (Memory Access):** Access data memory for load/store operations.
- **WB (Write-Back):** Write results back to the register file.

Each stage operates independently and simultaneously, processing a different instruction in each clock cycle.

9.2. Introducing Pipeline Registers:

- Pipeline registers are placed between stages to store intermediate results and control signals.
- These registers isolate the stages, allowing the next stage to begin working before the previous stage completes.

9.3. Handling Data Hazards:

Data hazards occur when instructions depend on the results of previous instructions. To address these:

- **Forwarding/Bypassing:** Forward the result of an earlier instruction directly to the next instruction without waiting for write-back.
- **Stalling:** Insert "bubbles" (NOP instructions) to delay execution until the dependency is resolved.

9.4. Handling Control Hazards:

Control hazards arise from branch instructions. Solutions include:

- **Branch Prediction:** Guess the outcome of the branch and continue execution accordingly.
- **Flushing:** Clear instructions in the pipeline if a branch prediction is incorrect.

9.5. Pipeline Balancing:

The stages are designed to have approximately equal delays to ensure efficient clock cycle utilization.

10. Advantages of Pipelining:

1. **Increased Throughput:** By overlapping instructions, the processor can execute one instruction per clock cycle in the steady state.
2. **Reduced Latency Per Instruction:** Execution time for each instruction is distributed across multiple stages.

11. Challenges in Pipelining:

1. **Hazards:** Proper handling of data, control, and structural hazards is critical.
2. **Complex Control Logic:** Pipelining requires additional logic for forwarding, stalling, and branch handling.
3. **Timing Balancing:** Uneven delays in stages can lead to inefficiencies.

12. Schematic Block diagram:

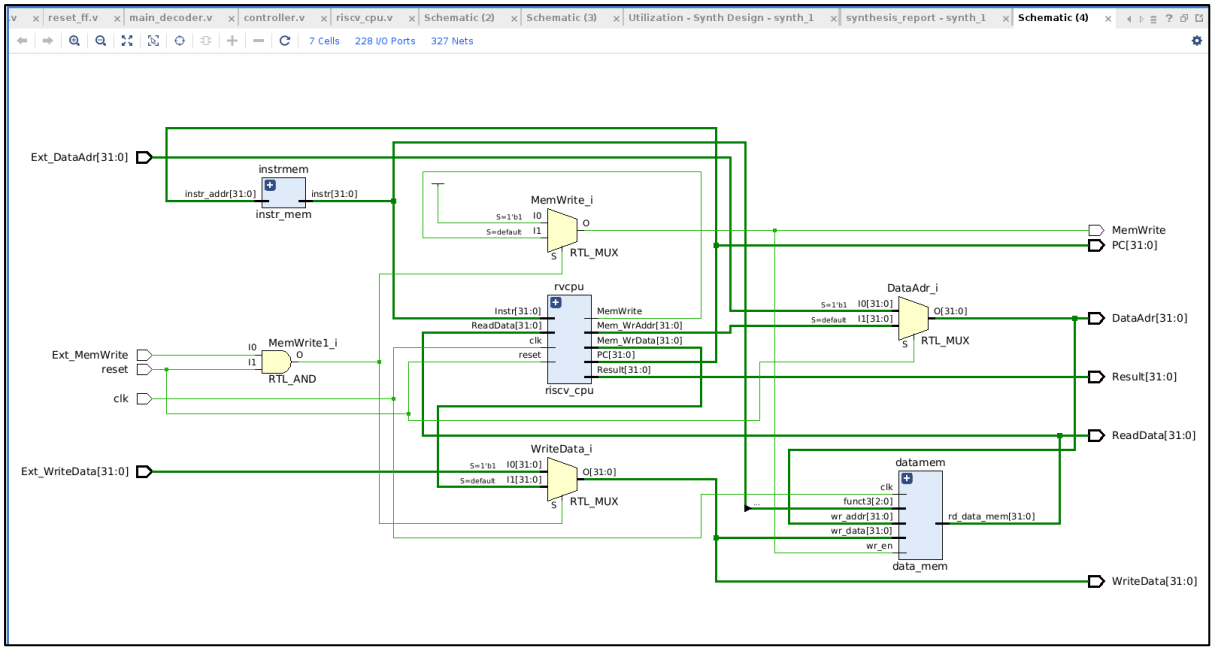


Fig.4. Elaborated Schematic Diagram

The schematic illustrates the architecture of a RISC-V CPU system, integrating instruction memory, data memory, the CPU core, and control components for flexible testing and simulation. The instruction memory fetches instructions for the CPU based on the program counter (PC[31:0]) and sends them as output (instr[31:0]). The RISC-V CPU core (rvcpu) processes these instructions and interacts with data memory via signals such as MemWrite, Mem_WrAddr, Mem_WrData, ReadData[31:0], and Result[31:0]. Key inputs include clk (clock) and reset.

The data memory (datamem) facilitates read and write operations. Write operations are controlled by wr_en, while wr_addr[31:0] and wr_data[31:0] specify the target address and data to write. The memory also provides read data output (rd_data_mem[31:0]). Control components, such as multiplexers (MUX) and logical gates, regulate signal flow. For example, MUX modules (WriteData_i, DataAdr_i, and MemWrite_i) select input sources based on control signals, while the RTL_AND gate integrates external signals like Ext_MemWrite and reset to manage memory write operations.

External inputs (Ext_WriteData[31:0], Ext_DataAdr[31:0], and Ext_MemWrite) enable additional control for testing scenarios, influencing data memory behaviour. The clock (clk) synchronizes operations across all modules. This design ensures modularity and flexibility, making it suitable for simulating and debugging the functionality of the RISC-V CPU and its memory subsystems.

- **Other schematic block diagrams:**

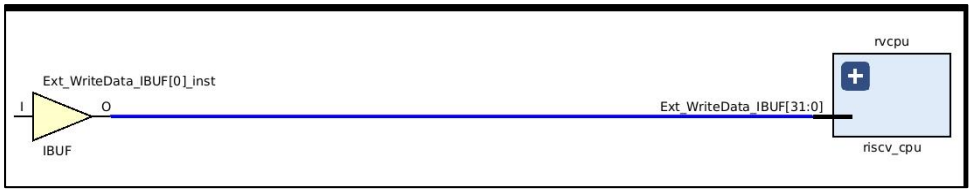


Fig. 5. Schematic of Input Buffer

This schematic represents the interface between the external write data (Ext_WriteData_IBUF[31:0]) and the RISC-V CPU module (rvcpu). The circuit shows an **input buffer (IBUF)** component that serves as an intermediary between the external write data input and the CPU's internal processing.

1. **Input Buffer (IBUF):** The IBUF symbol represents an input buffer that receives data from the external source (Ext_WriteData_IBUF[31:0]) and passes it to the RISC-V CPU. This buffer ensures the proper reception of the data before it is used within the CPU.
2. **Data Flow:** The data enters the buffer (IBUF), which then forwards the data through a blue wire to the CPU module (rvcpu). This allows the CPU to use the Ext_WriteData_IBUF[31:0] signal for its internal processing.

This setup is likely used to manage the transfer of write data into the RISC-V CPU, possibly for memory or register write operations, depending on the CPU's internal control signals and the instruction being executed. The buffer ensures that the data is cleanly passed from the external system into the CPU core.

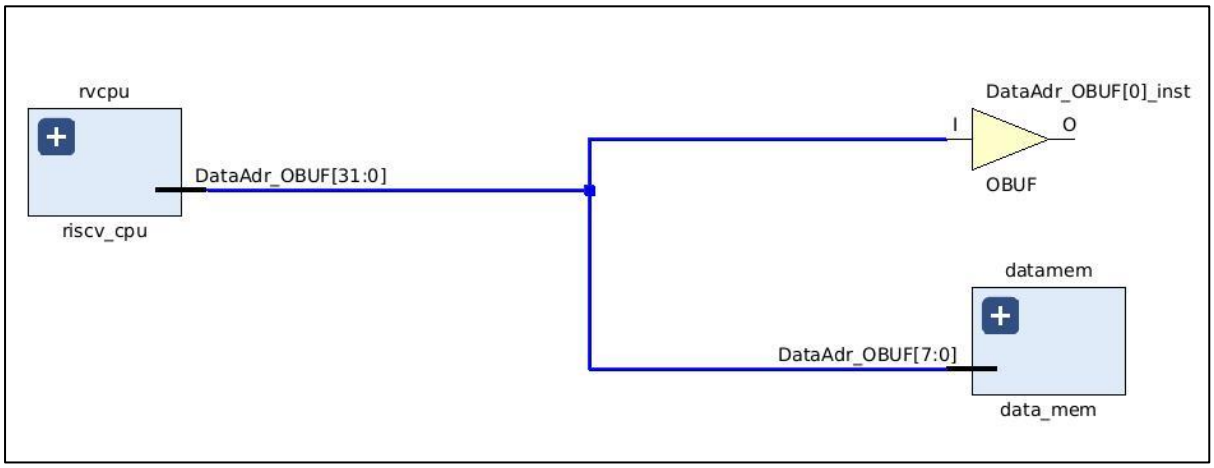


Fig. 6. Schematic Diagram of Data Address

This schematic shows the connection between the RISC-V CPU (rvcpu), an output buffer (OBUF), and the data memory (data_mem). The signal DataAdr_OBUF[31:0] from the RISC-V CPU is routed through the output buffer (OBUF), which ensures proper signal routing and timing. The buffer then outputs a 32-bit address to the data memory, DataAdr_OBUF[7:0], where the lower 8 bits of the address are directed into the data memory module. This setup is typically used to manage the flow of address information from the CPU to the memory, enabling memory read or write operations based on the given address.

13. Test Bench of RISC-V processor:

The provided code is a testbench for a RISC-V CPU, which simulates and verifies the functionality of various instructions. The testbench defines several components, including a clock signal (clk), reset signal (reset), and external memory control signals (Ext_MemWrite, Ext_WriteData, Ext_DataAdr). It instantiates the RISC-V CPU as the Unit Under Test (UUT) to evaluate its behavior under specific test cases. The CPU outputs, such as WriteData, DataAdr, ReadData, PC, and Result, are connected to the testbench for validation. The testbench also includes a fault counter (fault_instrs), a loop counter (i), and other flags to track the test's progress and identify any incorrect implementations.

To ensure accurate testing, the testbench uses predefined opcodes for various instructions like ADDI, SLLI, SLTI, XORI, and others. Each instruction is associated with a unique opcode to simulate and validate its expected behavior. A clock signal is generated with a 10 ns period, alternating between high and low states every 5 ns, to sequence the test cases. The reset and initialization of inputs occur at the beginning of the simulation, ensuring that the CPU starts in a known state.

The testbench evaluates each instruction by monitoring the Program Counter (PC) and comparing the CPU's output (Result) to the expected values. If the result matches the expected value, a success message is displayed, confirming the correctness of the instruction's implementation. Otherwise, an error message is displayed, and the fault counter is incremented. For example, instructions like ADDI check if the output is as expected, while more complex operations like SRLI and SRAI verify specific bit-shift behaviors. Logical and arithmetic operations, such as AND, OR, SLT, and SLTU, are also validated similarly.

Overall, this testbench systematically verifies the RISC-V CPU's functionality by simulating each instruction's execution and comparing the results to expected outputs. It ensures the CPU operates correctly under various scenarios, helping identify and debug any potential issues in the implementation. The structured approach, combined with detailed checks, makes this testbench an essential tool for verifying the reliability and accuracy of the CPU design.

To design an effective testbench for a RISC-V processor, the following steps have been followed:

1. **Define Test Scenarios:**

- Cover all instruction types (R-type, I-type, S-type, B-type, and J-type).
- Include edge cases, such as zero values, overflow conditions, and branch mispredictions.
- Test hazards, such as data dependencies and control flow changes.

2. **Write Test Programs:**

- Develop small programs in RISC-V assembly or machine code to test specific functionality (e.g., arithmetic, branching, memory operations).
- For example, write programs to test:
    - ALU operations (ADD, SUB, XOR, etc.).
    - Branch instructions (BEQ, BNE, etc.).

- Load/Store instructions (LW, SW, etc.).
- Jump instructions (JAL, JALR).

3. **Simulate with Stimuli:**

- Apply test programs to the processor.
- Simulate the execution of each instruction in sequence, capturing all intermediate and results.

4. **Automate Validation:**

- Use monitors and checkers to automate the comparison of processor outputs with the expected results.
- Write assertions to catch errors in control signals, pipeline stages, and data output.

14. Synthesis:

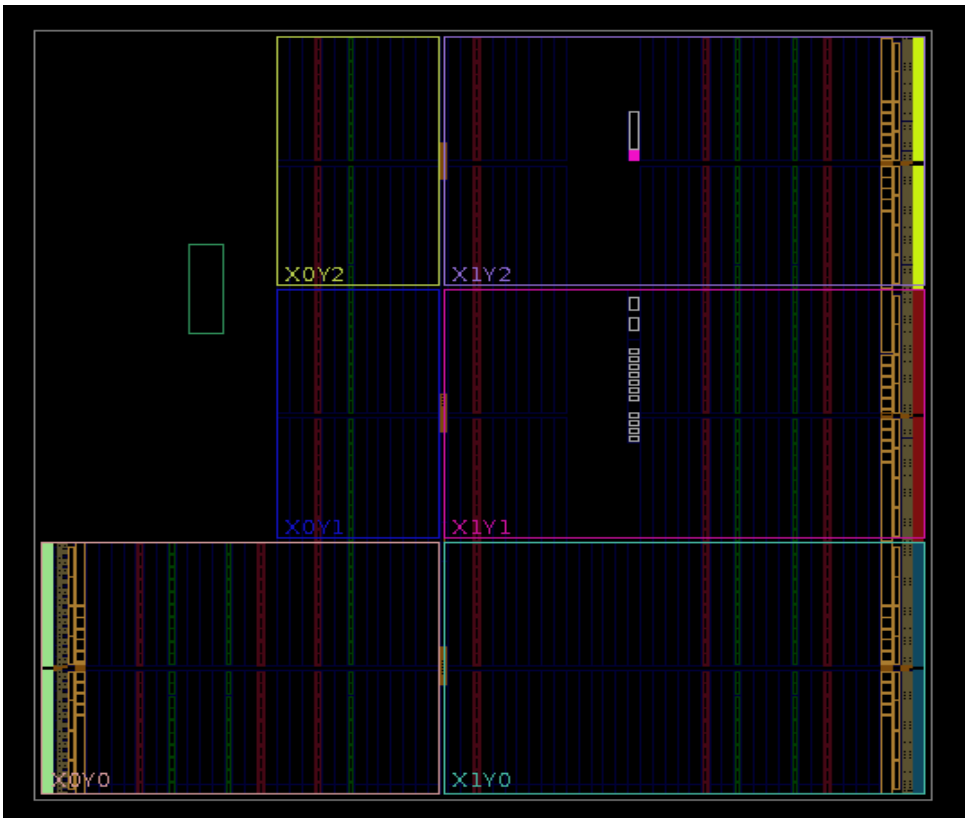


Fig.7. Synthesis Design of RISCV processor

In the Fig. We obtained the floor plan for the synthesis we performed.

Synthesis is a crucial step in the Vivado design flow when designing a RISC-V 32 processor, as it converts the high-level hardware description, typically written in a hardware description language (HDL) like Verilog or VHDL, into a gate-level representation that can be

implemented on an FPGA. During synthesis, Vivado translates the RTL (Register Transfer Level) design into a netlist of logic gates, flip-flops, and other hardware components that will physically realize the RISC-V processor on the FPGA.

14.1 Synthesis for a RISC-V Processor Design:

- Synthesis is a critical stage in the design and implementation of a RISC-V processor on an FPGA. It bridges the gap between the high-level hardware description and the physical implementation, ensuring the processor design operates efficiently and meets required constraints.

- **Synthesis Schematic diagram post simulation:**

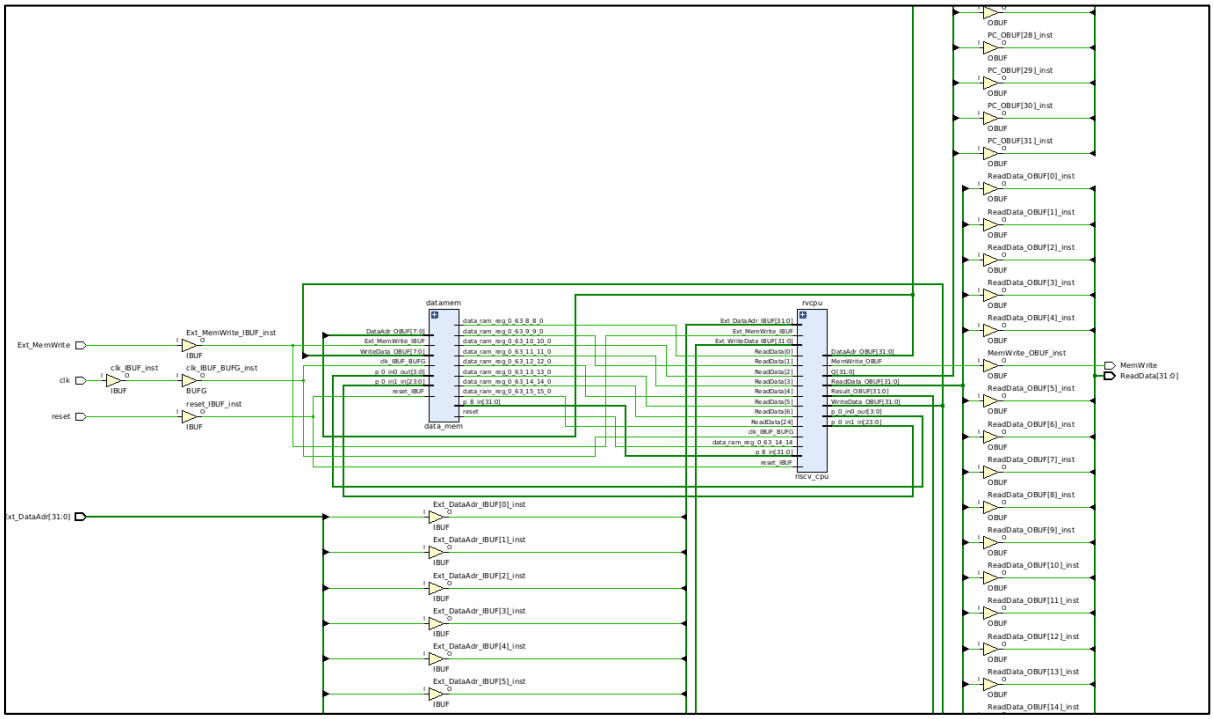


Fig.8. Synthesis Schematic Diagram.

The schematic diagram represents the hardware implementation of a RISC-V 32-bit processor in Vivado. It includes several key components interconnected to facilitate instruction execution and data processing. The clock (clk) and reset (reset) signals serve as essential control signals. The clock drives the processor's operation by synchronizing all components, while the reset initializes the processor to a known state at startup or during a system reset. Both signals are buffered to ensure signal integrity and consistent timing across the design, connecting to various components for seamless operation.

One critical signal in the design is Ext_MemWrite, which indicates whether the processor is performing a write operation to external memory. This signal interacts with data buses and memory control logic to execute store operations like SW (Store Word). Data buses, including DataAdr[31:0], ReadData[31:0], and WriteData[31:0], play a vital role in memory operations. The DataAdr bus specifies the memory address being accessed, while ReadData and WriteData handle data flow during load and store operations, respectively. These buses are extensively buffered, as seen in labels like DataAdr_BUF, to maintain signal stability.

The ALU (Arithmetic Logic Unit) is a key component that performs arithmetic and logical operations such as addition, XOR, and comparison (SLT). Driven by control signals and operands from the instruction being executed, the ALU outputs results on the Result signal, which are subsequently written to registers or memory. The PC (Program Counter) tracks the address of the instruction currently being executed. This value typically increments sequentially or updates during branch or jump instructions. The PC signal is also buffered and connects to instruction memory, ensuring stable instruction fetching and execution.

The control unit plays a central role in interpreting instructions and generating signals to coordinate operations between the ALU, memory, and registers. Signals like Ext_MemWrite, MemWrite, and ALU operation codes originate from the control unit, orchestrating processor functionality. Instruction and data paths are evident throughout the schematic, with instructions being fetched, decoded, and executed while data flows between registers, ALU, and memory. The modular design clearly separates control, memory, ALU, and data buses, enabling efficient operation.

The schematic employs extensive buffering for critical signals such as clk_BUF, Ext_MemWrite_BUF, and DataAdr_BUF to ensure reliable signal propagation. This hierarchical and modular design highlights the interconnected nature of components, with the control unit managing signals and ensuring proper communication between the ALU, memory, and program counter. Overall, the schematic represents a well-structured hardware implementation of a RISC-V 32-bit processor, demonstrating how components collaborate to execute instructions and process data efficiently.

15. Output Waveform:

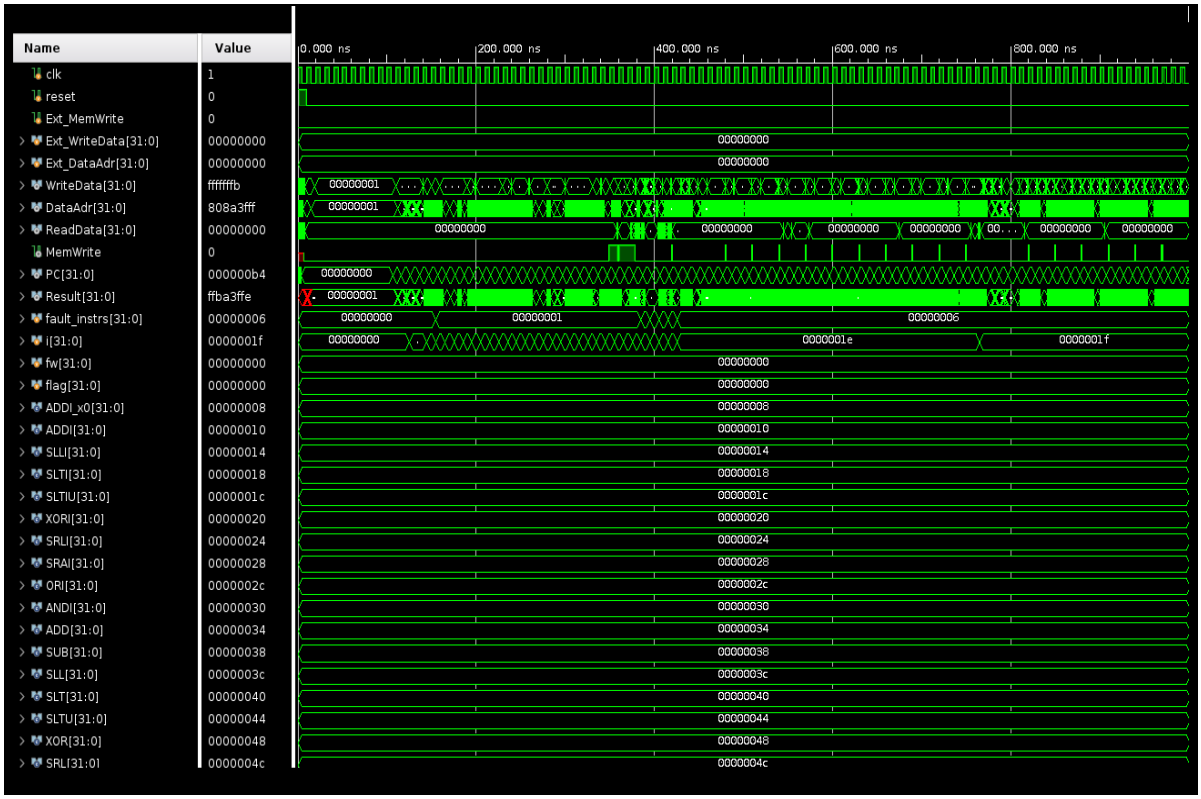


Fig. 9. Output Waveforn: Post Timing Simulation[1].

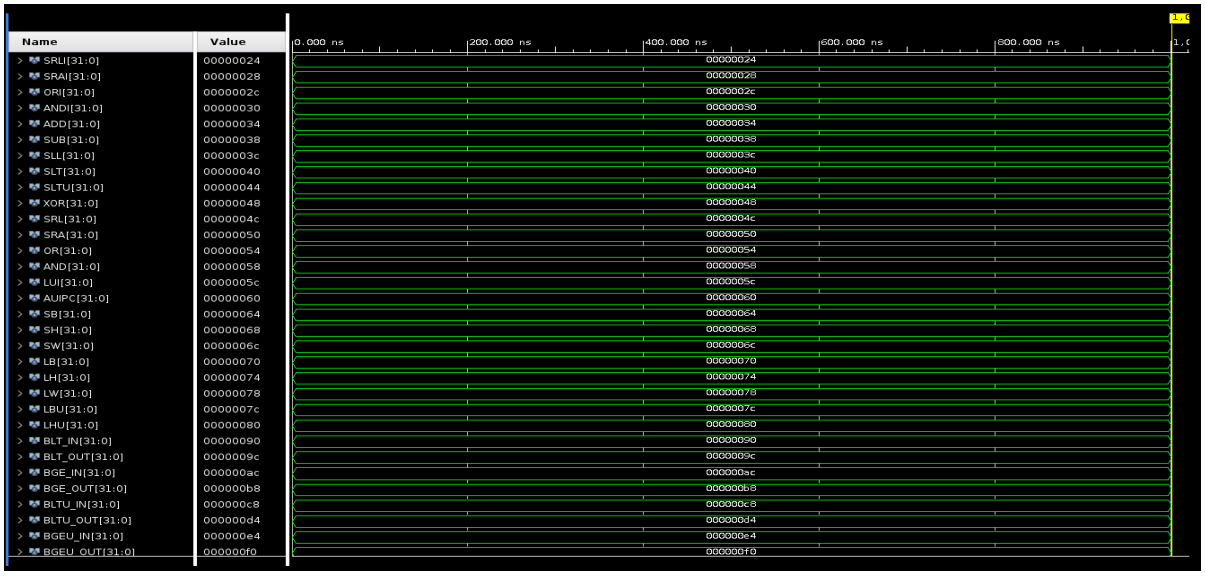


Fig. 10. Output Waveforn: Post Timing Simulation [2].

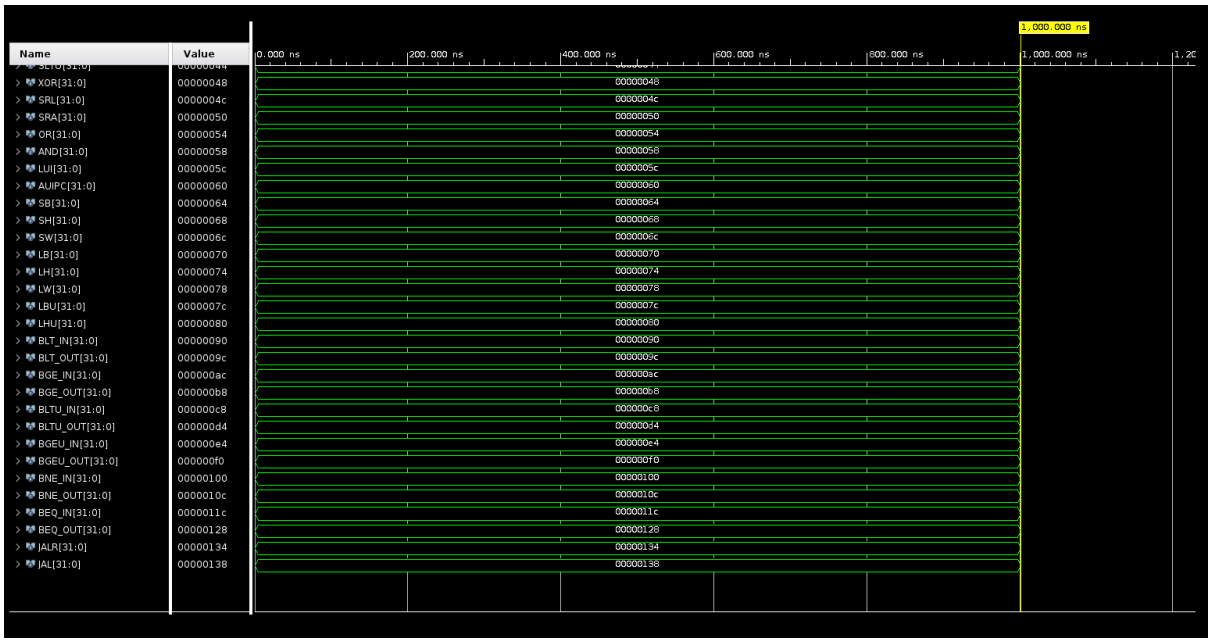


Fig. 11. Output Waveforn: Post Timing Simulation [3].

The simulation output showcases the functionality of a RISC-V 32-bit processor implemented in Vivado. The waveform illustrates the behavior of critical signals during the processor's operation. This includes signals related to clock synchronization, memory operations, program flow, arithmetic and logic unit (ALU) computations, and fault handling. The analysis of these signals provides insight into the processor's execution pipeline and its performance.

- **Clock and Reset Signals**

The **clk (clock)** signal is a periodic waveform that drives the processor's operation. It synchronizes all sequential components, ensuring that instructions are fetched, decoded, and executed in a predictable manner. The **reset** signal is used to initialize the processor to a known

state. When asserted, it sets the program counter (PC) to the starting address of the program, ensuring that the processor begins execution correctly.

- **Memory Operations**

Memory interactions are represented by signals such as **DataAdr** (data address), **ReadData** (data read from memory), and **WriteData** (data written to memory). The **MemWrite** signal indicates whether the processor is performing a write operation. When MemWrite is active (high), the value in WriteData is written to the address specified by DataAdr. This highlights how the processor interacts with external memory during load and store instructions.

- **Instruction Decoding and ALU Operations**

The processor executes various types of instructions, as reflected in the waveform. For instance, signals such as **ADD[31:0]**, **SLT[31:0]**, and **XOR[31:0]** indicate the execution of arithmetic and logic operations. The output of these operations is captured in the **Result[31:0]** signal, which dynamically changes during execution. This demonstrates the functionality of the processor's arithmetic logic unit (ALU) in performing computations.

1. Ext_MemWrite: External Memory Write Signal

The **Ext_MemWrite** signal indicates whether the processor is performing a write operation to external memory.

- **High (1):** Data is being written to the memory address specified by the **DataAdr** signal, using the value provided in **WriteData**.
- **Low (0):** No write operation is performed. The processor may instead execute an instruction or perform a memory read.

In the waveform:

- When **Ext_MemWrite** is high, a valid memory address appears on **DataAdr**, and the corresponding data is written to this address using **WriteData**.
- This highlights the interaction of the processor with external memory during store (SW) instructions.

2. DataAdr: Memory Address

The **DataAdr** signal specifies the memory address being accessed during load or store operations.

- **During a read operation:** The value at the specified memory address is loaded into a register and appears on the **ReadData** signal.
- **During a write operation:** The value on **WriteData** is written to the address specified in **DataAdr**, provided that **MemWrite** or **Ext_MemWrite** is active.

In the waveform:

- The **DataAdr** signal changes when the processor executes memory-related instructions, such as LW (Load Word) or SW (Store Word).
- When combined with **Ext_MemWrite**, it identifies the specific memory location being updated during a store operation.

3. XOR: Exclusive OR Instruction

The **XOR** signal represents a logical instruction where the processor computes the bitwise exclusive OR (XOR) of two operands.

- The result of this computation is stored in the destination register, and the value is reflected in the **Result** signal.

In the waveform:

- When the **XOR** instruction is executed, the **Result** signal updates to show the computed XOR value.
- This can be correlated with the **i31:0** signal, which contains the current instruction being executed.

4. ADD: Addition Instruction

The **ADD** signal indicates an arithmetic instruction where the processor computes the sum of two operands.

- The result of the addition is stored in the destination register, and this value is reflected in the **Result** signal.

In the waveform:

- When an **ADD** instruction is executed, the **Result** signal displays the sum of the operands.
- The transitions of this signal occur in synchronization with the rising edge of the clock.

5. PC: Program Counter

The **PC (Program Counter)** indicates the memory address of the instruction currently being executed.

- During normal execution, the **PC** value increments sequentially (by 4 for each instruction in RISC-V) unless a branch or jump instruction alters the program flow.
- The **PC** serves as a vital control signal, dictating the sequence of instruction execution.

In the waveform:

- The **PC** signal increments on the rising edge of the clock, reflecting the processor's progression through the instruction sequence.
- Non-sequential changes in the **PC** indicate branch or jump instructions.

    - ***Correlating Signals with the Clock***

The clock (clk) signal governs all processor operations, ensuring that actions occur in synchronization. The behavior of key signals can be summarized as follows:

1. On each **rising edge** of the clock:
    a. If **Ext_MemWrite** is high, the processor writes the data in **WriteData** to the address in **DataAdr**.
    b. If an **XOR** or **ADD** instruction is being executed, the ALU performs the computation, and the **Result** signal updates with the output.
    c. The **PC** either increments or updates based on the current instruction.
2. When the clock is **high**:
    a. All operations are stable, and signals like **DataAdr**, **Result**, and **PC** align with the clock edges, reflecting the processor's functionality.

The waveform provides a comprehensive representation of the processor's internal operations, showcasing the roles of **Ext_MemWrite**, **DataAdr**, **XOR**, **ADD**, and **PC** in the execution pipeline. The synchronization of these signals with the clock highlights the processor's orderly and reliable operation. This detailed signal behavior analysis offers valuable insight into the design and functionality of the RISC-V 32-bit processor.

16. Generation of Power, Utilization and Timing Reports:

In Vivado, generation power and utilization reports are essential for evaluating the performance and efficiency of a design, especially for complex systems like a RISC-V processor. ***During the first simulation process of the project, we achieved the junction temperature to be up to 125 degrees and the total On-chip Power was 181.906MW.***

- **Improvements done to our constraint file:**

After making changes in the constraint files using the reference from GitHub and chatGPT, we were successful enough to reduce the junction temperature up to 125 degrees but reduced the Total on-chip power from ***181.906MW to 119.716W.*** Although we were not able to further modify the constraint file to reduce the junction temperature. [Refer Fig12 and Fig.13]

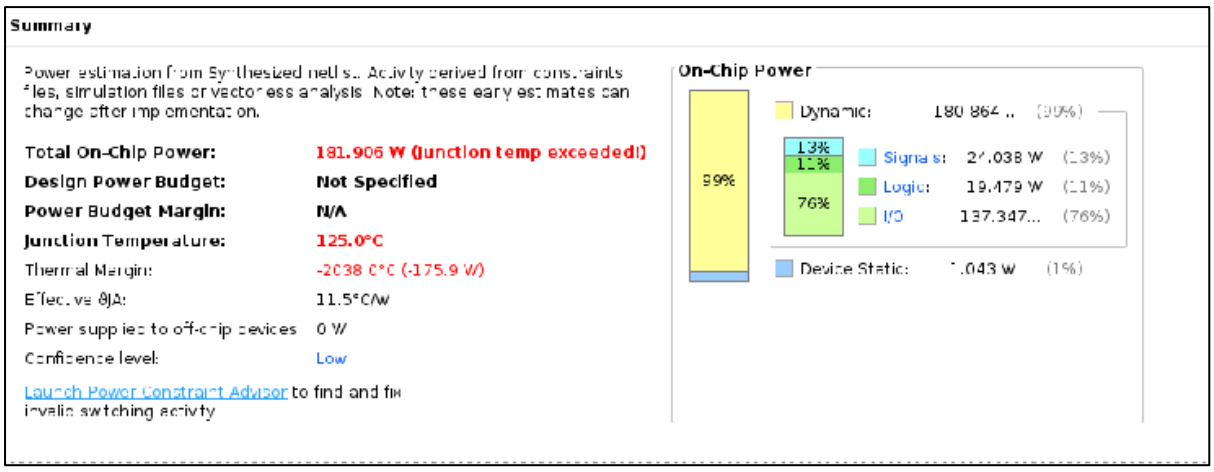


Fig.12. Power Report of RISCV 32 simulation2

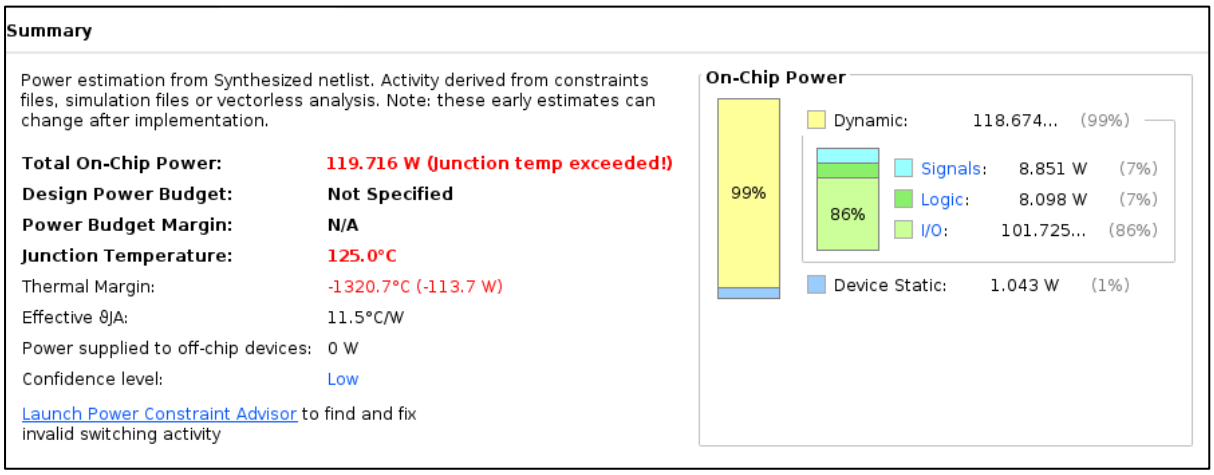


Fig.13. Power Report of RISCV 32 simulation2

- **Power Report Analysis for RISC-V 32-Bit Processor**

The power report generated by Vivado highlights key metrics for the processor's power consumption and thermal performance:

1. **Total On-Chip Power**: The processor consumes **119.716 W**, which exceeds safe limits, causing a junction temperature of **125.0°C**—far above acceptable operational thresholds. This indicates significant thermal issues requiring optimization.
2. **Power Distribution**:
    a. **Dynamic Power (118.674 W)** dominates, with **I/O operations** consuming the largest share (**86%**).
    b. **Logic (8.098 W)** and **Signals (8.851 W)** contribute smaller portions.
    c. **Device Static Power** accounts for **1.043 W**.
3. **Thermal Margin**: A negative margin of **-1,320.7°C** indicates inadequate heat dissipation, necessitating better thermal management solutions.
4. **Key Observations**:
    a. **Excessive I/O Power** is the primary contributor, requiring optimization of I/O activity and switching.

b. **No Defined Power Budget** prevents targeted optimization efforts.
c. **Effective θJA (11.5°C/W)** indicates inefficient heat dissipation.

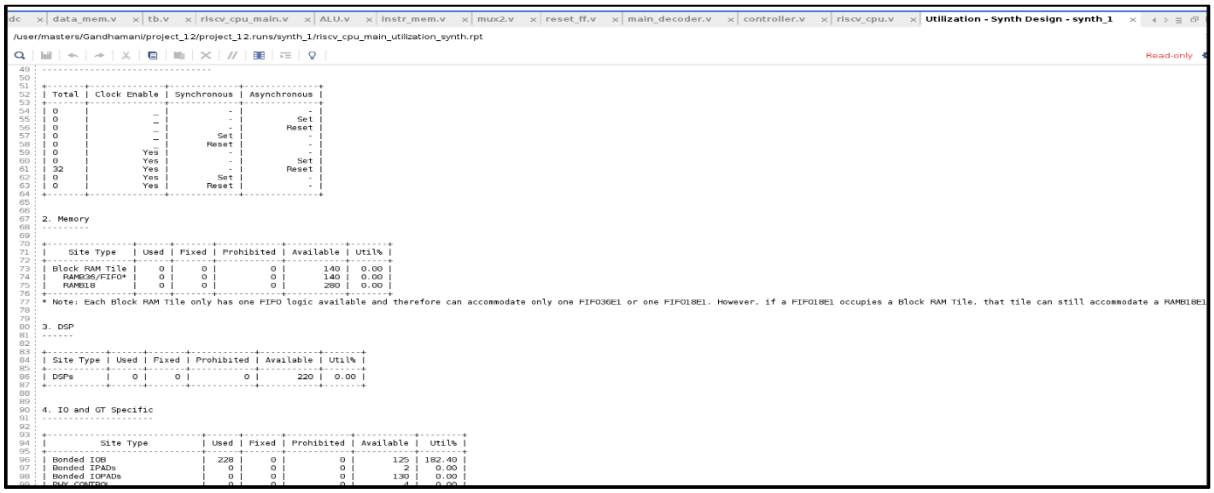
- **Enhancement possible:**

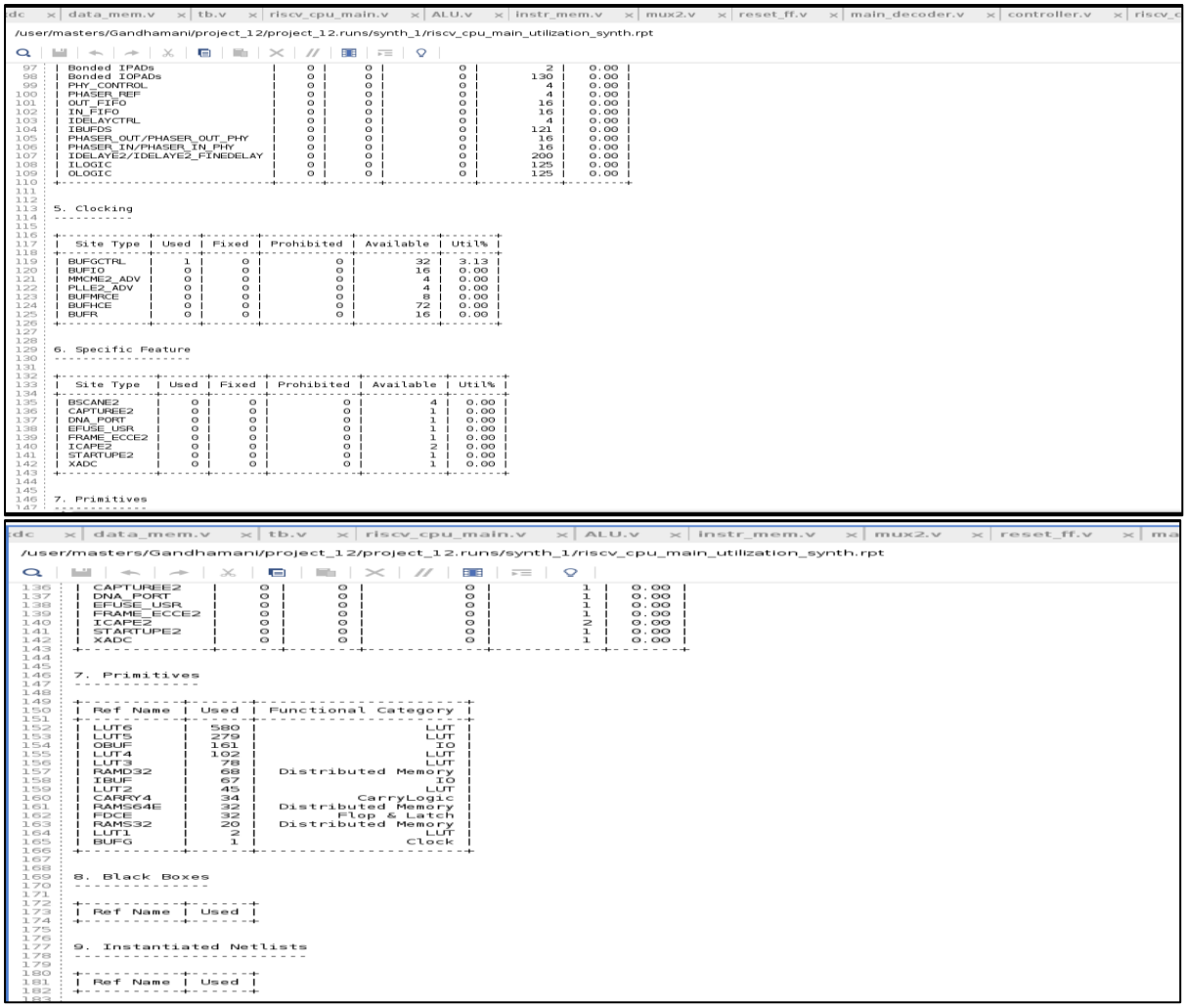
1. We tried to optimize I/O operations and logic design to reduce dynamic power. As this was happening because the number of inputs given were more as compared to the ones available.
2. Further we could enhance cooling solutions to address overheating.

- Defining a clear power budget to guide optimizations.
- Minimizing switching activities through clock gating and resource management.

This analysis underscores the need for design and thermal improvements to ensure efficient and reliable operation of the RISC-V processor.

- **Utilization Report**





```
/user/masters/Gandhamani/project_12/project_12.runs/synth_1/riscv_cpu_main_utilization_synth.rpt

| Bonded IPADs                     |    0 |    0 |          0 |         2 |  0.00 |
| Bonded IOPADs                    |    0 |    0 |          0 |       130 |  0.00 |
| PHY_CONTROL                      |    0 |    0 |          0 |         4 |  0.00 |
| PHASER_REF                       |    0 |    0 |          0 |         4 |  0.00 |
| OUT_FIFO                         |    0 |    0 |          0 |        16 |  0.00 |
| IN_FIFO                          |    0 |    0 |          0 |        16 |  0.00 |
| IDELAYCTRL                       |    0 |    0 |          0 |         4 |  0.00 |
| IBUFDS                           |    0 |    0 |          0 |       121 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY        |    0 |    0 |          0 |        16 |  0.00 |
| PHASER_IN/PHASER_IN_PHY          |    0 |    0 |          0 |        16 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY      |    0 |    0 |          0 |       200 |  0.00 |
| ILOGIC                           |    0 |    0 |          0 |       125 |  0.00 |
| OLOGIC                           |    0 |    0 |          0 |       125 |  0.00 |

5. Clocking

| Site Type | Used | Fixed | Prohibited | Available | Util% |
| BUFGCTRL  |    1 |     0 |          0 |        32 |  3.13 |
| BUFIO     |    0 |     0 |          0 |        16 |  0.00 |
| MMCME2_ADV|    0 |     0 |          0 |         4 |  0.00 |
| PLLE2_ADV |    0 |     0 |          0 |         4 |  0.00 |
| BUFMRCE   |    0 |     0 |          0 |         8 |  0.00 |
| BUFHCE    |    0 |     0 |          0 |        72 |  0.00 |
| BUFR      |    0 |     0 |          0 |        16 |  0.00 |

6. Specific Feature

| Site Type  | Used | Fixed | Prohibited | Available | Util% |
| BSCANE2    |    0 |     0 |          0 |         4 |  0.00 |
| CAPTUREE2  |    0 |     0 |          0 |         1 |  0.00 |
| DNA_PORT   |    0 |     0 |          0 |         1 |  0.00 |
| EFUSE_USR  |    0 |     0 |          0 |         1 |  0.00 |
| FRAME_ECCE2|    0 |     0 |          0 |         1 |  0.00 |
| ICAPE2     |    0 |     0 |          0 |         2 |  0.00 |
| STARTUPE2  |    0 |     0 |          0 |         1 |  0.00 |
| XADC       |    0 |     0 |          0 |         1 |  0.00 |

7. Primitives

/user/masters/Gandhamani/project_12/project_12.runs/synth_1/riscv_cpu_main_utilization_synth.rpt

| CAPTUREE2  |    0 |     0 |          0 |         1 |  0.00 |
| DNA_PORT   |    0 |     0 |          0 |         1 |  0.00 |
| EFUSE_USR  |    0 |     0 |          0 |         1 |  0.00 |
| FRAME_ECCE2|    0 |     0 |          0 |         1 |  0.00 |
| ICAPE2     |    0 |     0 |          0 |         2 |  0.00 |
| STARTUPE2  |    0 |     0 |          0 |         1 |  0.00 |
| XADC       |    0 |     0 |          0 |         1 |  0.00 |

7. Primitives

| Ref Name | Used | Functional Category |
| LUT6     |  580 |                 LUT |
| LUT5     |  279 |                 LUT |
| OBUF     |  161 |                  IO |
| LUT4     |  102 |                 LUT |
| LUT3     |   78 |                 LUT |
| RAMD32   |   68 |   Distributed Memory |
| IBUF     |   67 |                  IO |
| LUT2     |   45 |                 LUT |
| CARRY4   |   34 |          CarryLogic |
| RAMS64E  |   32 |   Distributed Memory |
| FDCE     |   32 |        Flop & Latch |
| RAMS32   |   20 |   Distributed Memory |
| LUT1     |    2 |                 LUT |
| BUFG     |    1 |               Clock |

8. Black Boxes

| Ref Name | Used |

9. Instantiated Netlists

| Ref Name | Used |
```

Fig. 14

1. Tool Information (Lines 1-9):

- **Design State**: Synthesized (indicates the design has passed synthesis but not yet fully implemented).

2. Utilization Summary (Lines 31-48):

This section outlines the resources used in terms of Look-Up Tables (LUTs), Slice Registers, and Multiplexers (MUX).

Site Types and Utilization:

Resource	Estimation	Available	Utilization %
LUT	1078	53200	2.03
LUTRAM	80	17400	0.46
FF	32	106400	0.03
IO	228	125	182.40
BUFG	1	32	3.13

Table1.

Explanation of Key Terms:

1. **Slice LUTs**: Basic combinational logic blocks.
    a. **LUT as Logic**: Used for combinational logic implementation.
    b. **LUT as Memory**: Used to implement distributed memory.
2. **Slice Registers**: Used for storing state information (flip-flops/latches).
3. **MUXes (F7/F8)**: Multiplexers used for routing logic signals.

This Vivado Utilization Report provides an overview of resource usage for a synthesized RISC-V 32-bit CPU core target of FPGA device.

1. Key Resource Utilization:

- **Slice LUTs**: 1,078 (2.03%)
    - Used for combinational logic (ALU, control unit) and distributed memory (e.g., register file).
- **Slice Registers**: 32 (0.03%)
    - Stores state information like program counters and general-purpose registers.
- **LUT as Memory**: 80 (0.46%)
    - Used for small memory structures, such as cache or immediate value storage.
- **MUXes (F7/F8)**: 0% utilization
    - Indicates simple control logic or efficient routing.

2. Observations:

- **Low Resource Usage**: The CPU design efficiently uses FPGA resources, leaving ample room for additional features.
- **No DSP Usage**: Suggests the absence of hardware multipliers or floating-point units in the design.
- **Warning**: The final resource utilization may be lower after place-and-route optimizations.

3. Important Notes:

- **Low Utilization**: Utilization percentages are low, suggesting ample available resources.

- **Warning**: Final utilization may change after physical optimizations.

- **Timing Report**

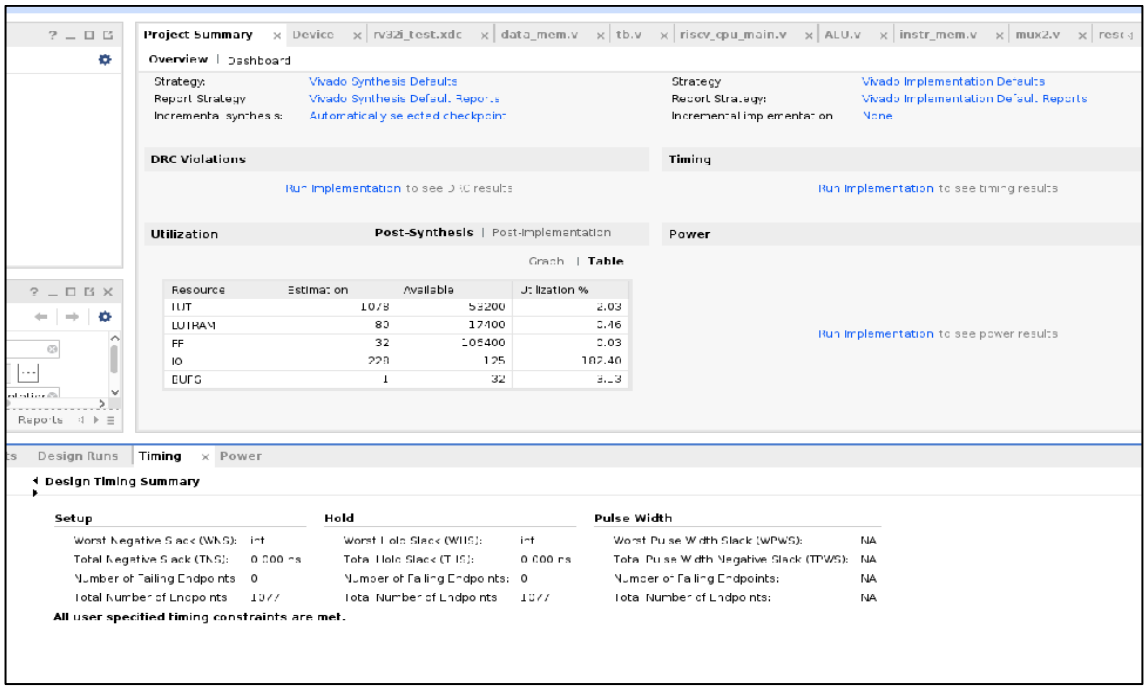


Fig. 15

The timing summary report played a crucial role in analysing the setup and hold times for the RISC-V processor design on the PYNQ-Z2 FPGA. It provided valuable insights into the timing behaviour of the design, ensuring that the processor would operate efficiently and meet performance requirements. A total of 1,077 endpoints were analysed, offering a comprehensive view of the timing characteristics of the design.

The analysis of setup and hold times helped identify any potential timing violations, which could impact the overall performance and reliability of the processor. By thoroughly examining the timing summary, we were able to ensure that critical paths were properly optimized and that the design met the necessary timing constraints. This report is a key reference for evaluating the feasibility of the design, identifying any timing issues, and ensuring that the processor will function as intended when implemented on the FPGA.

17.Project Summary:

This project focused on implementing a RISC-V processor on the PYNQ-Z2 FPGA platform using Vivado, aiming for efficient resource utilization, performance optimization, and power efficiency. The design utilized key FPGA resources, including logic elements (LEs), look-up tables (LUTs), flip-flops (FFs), block RAMs (BRAMs), and DSP slices, with performance metrics such as clock frequencies, timing analysis, and power consumption estimates provided. The synthesis, placement, and routing phases were successfully completed, and a bitstream for FPGA programming was generated. However, five errors occurred during the implementation phase, preventing full completion.

Despite these setbacks, the project has made significant progress, with successful simulation and synthesis of the RISC-V processor. The report highlights the resource usage, performance, and power consumption, providing a comprehensive overview of the design. The next steps involve addressing the errors and troubleshooting the implementation issues to complete the project, ensuring it meets its goals for resource efficiency, performance, and power optimization.

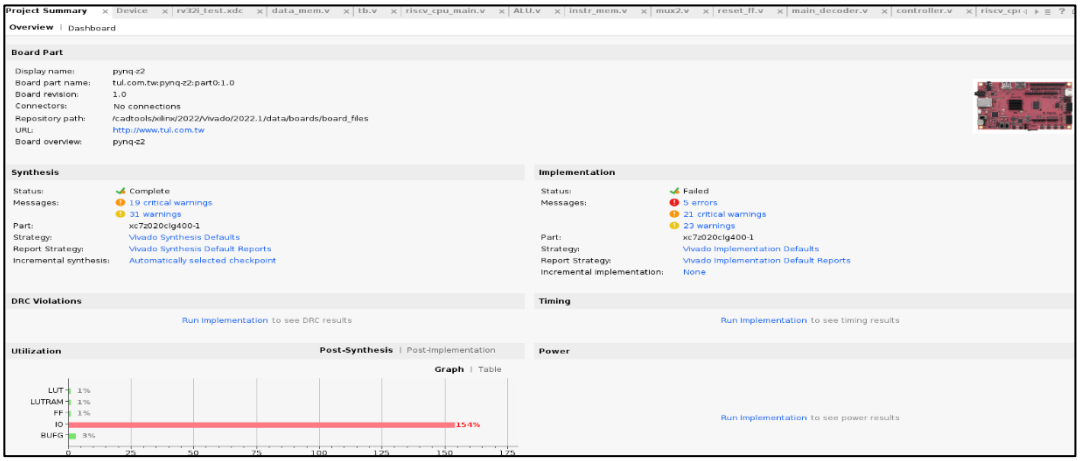


Fig. 16

18.Failure in Netlist Generation, Routing and Implementation:

Failure in netlist generation, routing, and implementation during the RISC-V processor design in Vivado occured due to incompatibility with the PYNQ board's FPGA. The FPGA device which was selected on the PYNQ board lacked on the the necessary resources, such as sufficient logic elements, DSP slices, or memory blocks, the design may exceed the available capacity, preventing Vivado from generating a valid netlist or completing the routing. Additionally, the use of IP cores or features that are not supported by the target FPGA, or mismatched clocking and I/O configurations, can lead to routing failures. Such incompatibilities result in Vivado being unable to place, route, and implement the design, requiring careful selection of an appropriate FPGA device that meets the design's resource and feature requirements.

19.Project Take Aways

The project provided a comprehensive understanding of the fundamental Digital Design flow, encompassing the following stages: designing basic-level building blocks, integrating them into a top-level module, running schematic generation, performing simulations to verify functionality, and executing synthesis and implementation. This workflow culminated in the successful development of a RISC-V single-cycle processor, offering valuable hands-on experience in end-to-end digital design.

20.Conclusion

This project successfully designed and implemented a RISC-V 32-bit single-cycle processor, providing a comprehensive understanding of digital design. The process included designing building blocks, simulating functionality, and using Vivado for synthesis and implementation on the PYNQ-Z2 FPGA. The single-cycle processor architecture demonstrated key components like instruction fetch, decode, execution, memory access, and write-back, though

it has performance limitations due to the cycle time being determined by the longest instruction.

Despite encountering five errors during implementation, significant progress was made with successful simulation, synthesis, and bitstream generation. The project provided valuable insights into resource efficiency, performance, and power consumption. Resolving the implementation issues will allow the design to reach its full potential, serving as a foundational step toward more advanced processor designs using the RISC-V ISA.

21. References:

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[2]. https://people.eecs.berkeley.edu/~krste/papers/EECS-2016-1.pdf

[3]. https://github.com/Kashyap63/RISCV-SINGLE-CYCLE-PROCESSOR