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# GATE:EC-49-2022

# EE23BTECH11025 - Anantha Krishnan

## I. QUESTION

Consider a boolean gate(D) where output Y is related to the inputs A and B as,  $Y = A + \overline{B}$ , where + denotes logical OR operation. The Boolean inputs '0' and '1' are also available separately. Using instances of only D gates and inputs '0' and '1' (Select the correct options)

- (A) NAND logic can be implemented
- (B) OR logic cannot be implemented
- (C) NOR logic can be implemented
- (D) AND logic cannot be implemented

### II. SOLUTION

If a NAND gate or NOR gate is implemented from the D-Gate, it will be a universal gate. For NOT gate:

$$\overline{A} = Dgate(0, A) \tag{1}$$

For NAND gate:

$$\overline{A.B} = Dgate(Dgate(0, A), B)$$
(2)

Therefore D-gate is a universal gate and all logic gates specified in the options can be implemented making (A),(C) to be the right options.

Code for implementation through C onto Vaman-ARM.

https://github.com/Gandubs/Digital-Design/tree/master/Assignments/ec'22-49