GATE:IN-42-2023

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I. QUESTION

In the circuit shown, the initial binary content of shift register A is 1101 and that of shift register B is 1010. The shift registers are positive-edge triggered, and the gates have no delay.

When the shift control is high, what will be the binary content of the shift registers A and B after four clock pulses?

(A) $A = 1101, B = 1101$
(B) $A = 1110, B = 1001$
(C) $A = 0101, B = 1101$
(D) $A = 1010, B = 1111$

II. SOLUTION

Code for implementation through Verilog onto FPGA. write link here