GATE:CS22-18

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I. question

Let R1 and R2 be two 4-bit registers that store numbers in 2's complement form. For the operation R1 and R2, which one of the following values of R1 and R2 gives an arithmetic overflow?

(A) R1 = 1011 and R2 = 1110
(B) R1 = 1100 and R2 = 1010
(C) R1 = 0011 and R2 = 0100
(D) R1 = 1001 and R2 = 1111

II. Solution

Converting each 2's complement to their binary equivalent, Adding up and converting to 2's complement form:

(A)

$$R1 = -(0101) \text{ and } R2 = -(0010) \tag{1}$$

$$R1 + R2 = 1001 \tag{2}$$

(B)

$$R1 = -(0100) \text{ and } R2 = -(0110) \tag{3}$$

$$R1 + R2 = 0110 \tag{4}$$

(C)

$$R1 = +(0011) \text{ and } R2 = +(0100) \tag{5}$$

$$R1 + R2 = 0111 \tag{6}$$

(D)

$$R1 = -(0111) \text{ and } R2 = -(0001) \tag{7}$$

$$R1 + R2 = 1000 \tag{8}$$

In option (B) the signed bit of the sum changed from each of the both same signed numbers indicating an overflow.

Code for implementation through platformio
https://github.com/Gandubs/Digital-Design/blob/master/Assignments/cs'22-18/Codes/cs22-18.c