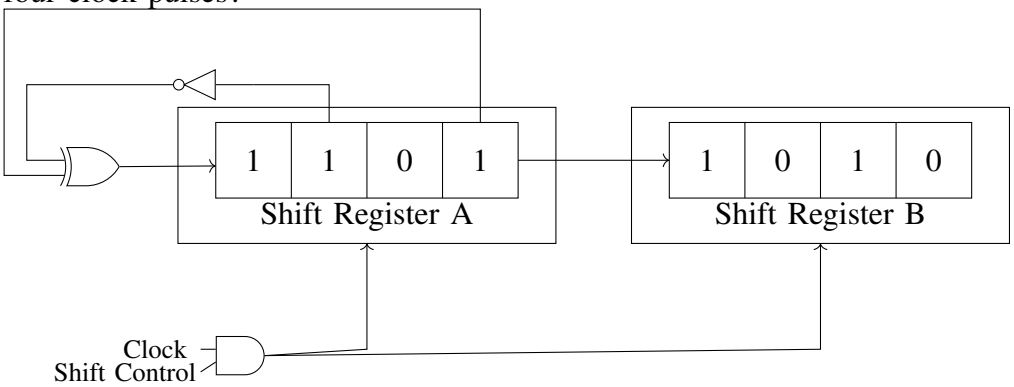
GATE:IN-42-2023

EE23BTECH11025 - Anantha Krishnan

I. QUESTION

In the circuit shown, the initial binary content of shift register A is 1101 and that of shift register B is 1010. The shift registers are positive-edge triggered, and the gates have no delay.

When the shift control is high, what will be the binary content of the shift registers A and B after four clock pulses?



1) $A = 1101, B = 1101$
2) $A = 1110, B = 1001$
3) $A = 0101, B = 1101$
4) $A = 1010, B = 1111$

II. SOLUTION

Clock and shift duration are always high here, therefore shifting occurs.
Let contents of register A be denoted by A(x,y,z,w) - (left to right) and same for B.
For the first cycle of shifting:

$$A = (0 \oplus 1, 1, 1, 0) \tag{1}$$
$$= (1, 1, 1, 0) \tag{2}$$
$$B = (1, 1, 0, 1) \tag{3}$$

After second cycle of shifting:

$$A = (0 \oplus 0, 1, 1, 1) \tag{4}$$
$$= (0, 1, 1, 1) \tag{5}$$
$$B = (0, 1, 1, 0) \tag{6}$$

After third cycle of shifting:

$$A = (0 \oplus 1, 1, 1, 1) \tag{7}$$
$$= (1, 0, 1, 1) \tag{8}$$
$$B = (1, 0, 1, 1) \tag{9}$$

After fourth cycle of shifting:

$$A = (1 \oplus 1, 1, 0, 1) \tag{10}$$
$$= (0, 1, 0, 1) \tag{11}$$
$$B = (1, 1, 0, 1) \tag{12}$$

Therefore option (C) is true. Code for implementation through Verilog onto FPGA.
https://github.com/Gandubs/Digital-Design/blob/master/Assignments/in'23-42/codes/fpga.v