GATE:EC-49-2022

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I. QUESTION

Consider a boolean gate(D) where output Y is related to the inputs A and B as, $Y = A + \overline{B}$, where + denotes logical OR operation. The Boolean inputs '0' and '1' are also available separately. Using instances of only D gates and inputs '0' and '1' (Select the correct options)

(A) NAND logic can be implemented
(B) OR logic cannot be implemented
(C) NOR logic can be implemented
(D) AND logic cannot be implemented