

1. Description

1.1. Project

Project Name	Delay_Timer
Board Name	custom
Generated with:	STM32CubeMX 6.13.0
Date	01/31/2025

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

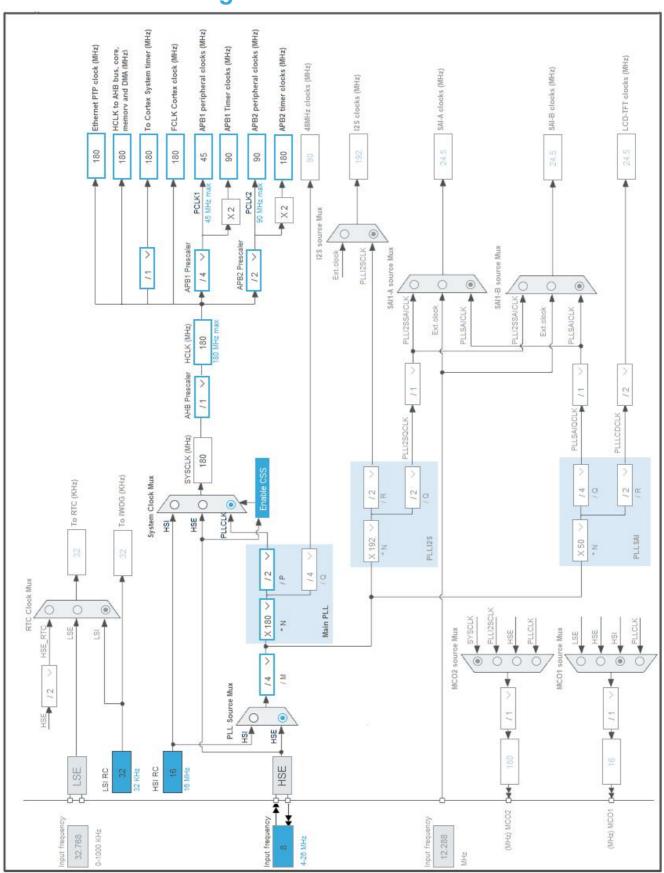


3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD	Power		
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
120	VSS	Power		
121	VDD	Power		
128	PG13 *	I/O	GPIO_Output	LED
130	VSS	Power		
131	VDD	Power		
138	воото	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	DS9405_Rev9

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

1.4. Sequence

C4am	Ct 4	Ct O
Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	57 mA	100 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	97.48	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	5.79 mA
Battery Life	24 days, 10 hours	Average DMIPS	225.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	Delay_Timer
Project Folder	C:\Users\cp199\OneDrive\Documentos\STM32Projects\STM32F_ExampleCodes
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_TIM1_Init	TIM1

3. Peripherals and Middlewares Configuration

3.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

3.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

Power Over Drive Enabled

3.2. SYS

Timebase Source: SysTick

3.3. TIM1

Clock Source : Internal Clock

3.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 2879 *
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 62499

Counter Period (AutoReload Register - 16 bits value) 62499 *
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Delay_	Timer	Pro	ject
Configu	uration	Re	port

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0/OSC_I	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_O UT	RCC_OSC_OUT	n/a	n/a	n/a	
GPIO	PG13	GPIO_Output	Output Push Pull	Pull-down *	Low	LED

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
TIM1 break interrupt and TIM9 global interrupt	unused			
TIM1 update interrupt and TIM10 global interrupt	unused			
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused			
TIM1 capture compare interrupt	unused			
FPU global interrupt	unused			

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

			Middleware			
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA		TIM1 ❷				
GPIO ♥						
NVIC ♥						
RCC ♥						
sys ♥						

6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f427-437_429-

439_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f427-437_429-

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System View https://www.st.com/resource/en/svd/stm32f4-svd.zip

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