EE 652 DIGITAL IC DESIGN

PROJECT PRESENTATION

Under the guidance of

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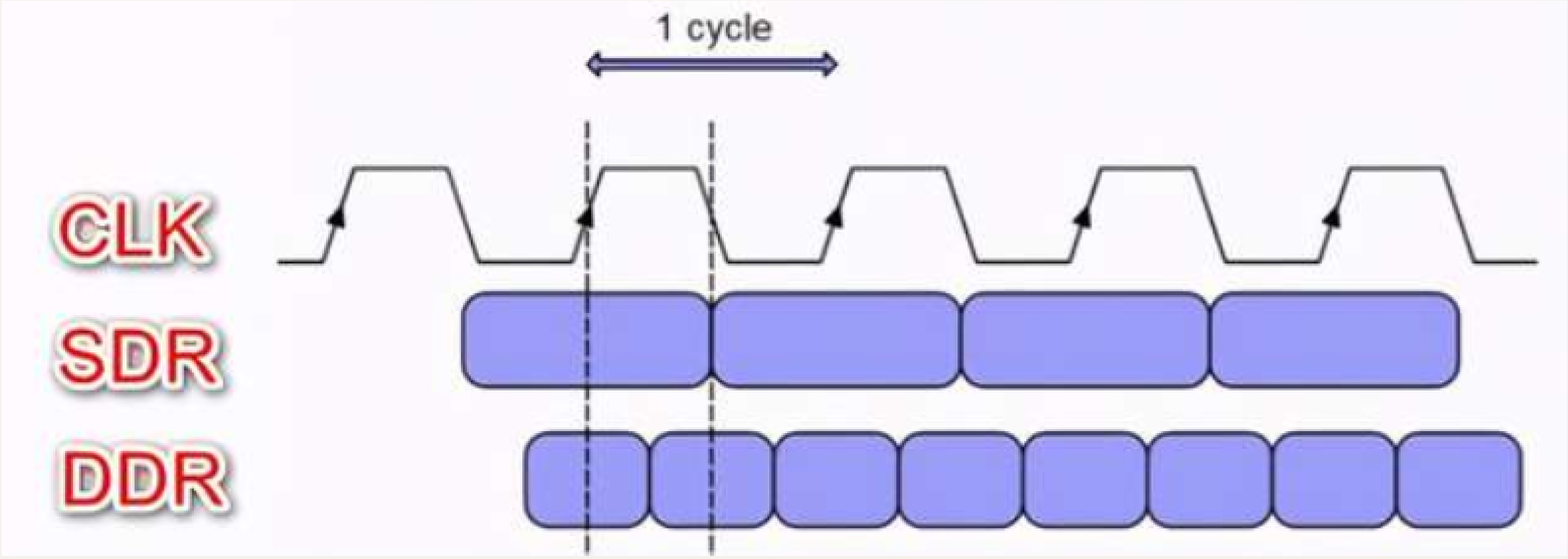
TOPIC:

Create a SystemVerilog module that models a DDR memory controller and verify its functionality with a testbench.

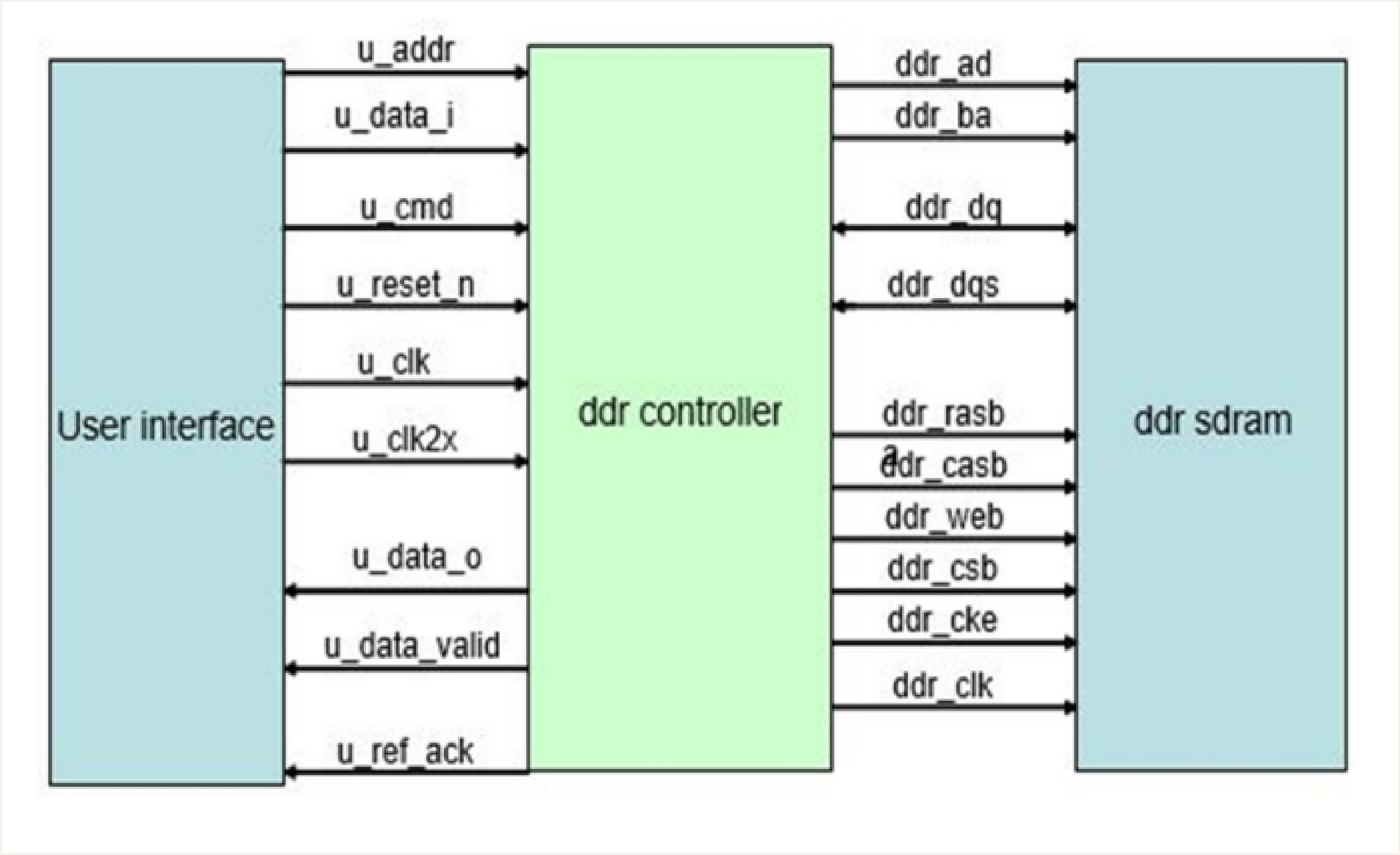
What is DDR?

DDR is a technique in computing in which the data transfers happen on both falling and rising edges of a clock cycle/signal at a double rate when compared to SDR.



2 transfers per cycle

Top Level Block diagram



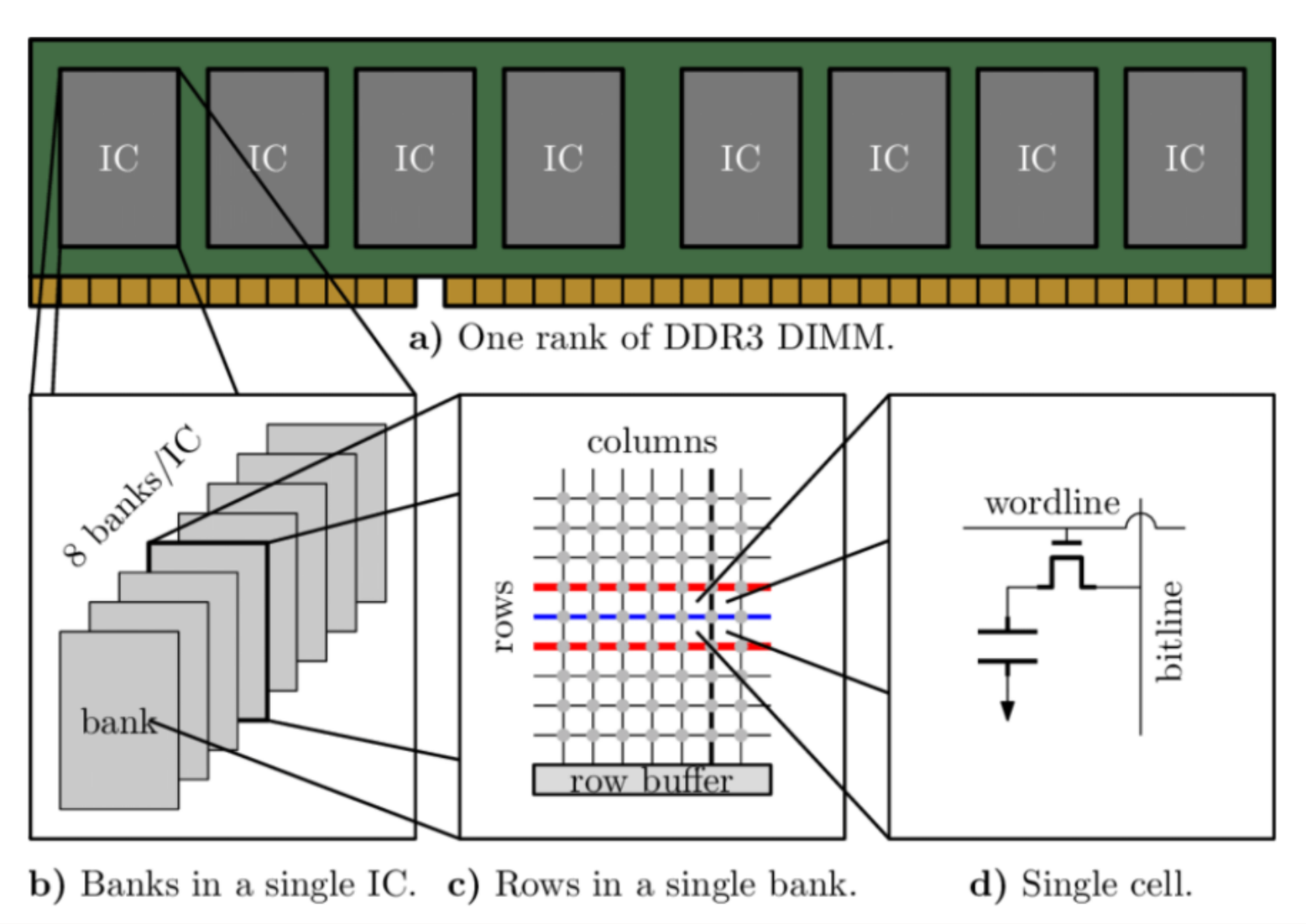
DDR memory contains three buses

Data bus
Data signals (DQ)
Data strobe signals (DQS)

Address bus
Row/ column Address (ADDR)
Bank address (BA)

Command bus
Column address strobe (CAS)
Row address strobe (RAS)
Write enable (WE)
Clock enable (CKE)
Chip-select (CS)

DRAM memory


IC
IC
IC
IC
IC
IC
IC
IC
a) One rank of DDR3 DIMM.
8 banks/IC
bank
columns
rows
row buffer
wordline
bitline
b) Banks in a single IC.
c) Rows in a single bank.
d) Single cell.

Fundamental DRAM Commands

CS: Enables or disables the command decoder

RAS: Activates a row address from where the data is retrieved.

CAS: Activates a column address from where the data is retrieved.

WE: Enables to write data into memory

Command	CS#	RAS#	CAS#	WE#
COMMAND INHIBIT	H	X	X	X
ACTIVATE	L	L	H	H
PRECHARGE	L	L	H	L
READ	L	H	L	H
WRITE	L	H	L	L
REFRESH	L	L	L	H

Truth table listing the decoder input combinations for executing different DRAM commands

Fundamental DRAM Commands

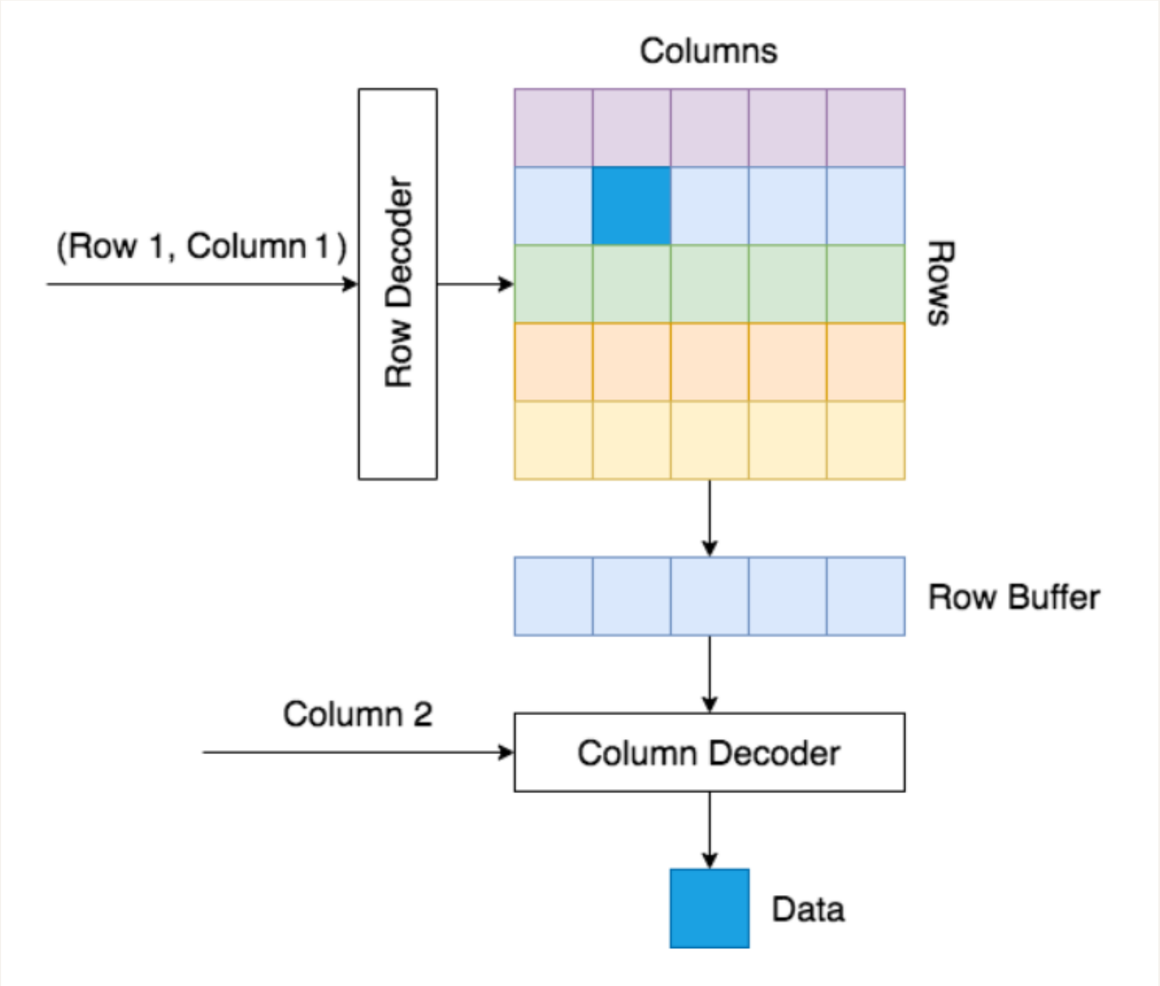
Activate: Senses and amplifies the data from the target row into the row buffer (open row).

Read: Transfers data from the row buffer to DDR bus.

Write: Tansfers data from the DDR bus to the row buffer.

Precharge: Clears the row buffer into DRAM and prepares the subarray for subsequent read/write operations.

Refresh: Refreshes memory rows often as capacitors used for memory storage will leak charge over time.



Refresh

DRAM

Refreshing Request: Received after specific number of clock cycles

Refreshing: Refresh is happening

Refresh row count: Count the number of rows being refreshed

Refresh Done: Sends as output after completion of refresh

DDR Controller

Refreshing Count (Down): Counts the number of clock cycles to send refresh request

Open Row policy:
In this policy we don't close the row after performing the read or write operation is done.
Until there is Row miss we can use the open row.
It would be more expensive when there is row miss because then we have to do the precharge.

Close Row policy:
In this policy we close the row after performing every read or write operation is done.
It seems that every time it is row miss, but the precharge would not be on the critical path. So, we can get all the memory operations at same time.

Both of these policies has advantages and disadvantages at their own costs and depends on the user which type of operations they want to perform. If we want to perform the operations.

Timing constraints of DDR

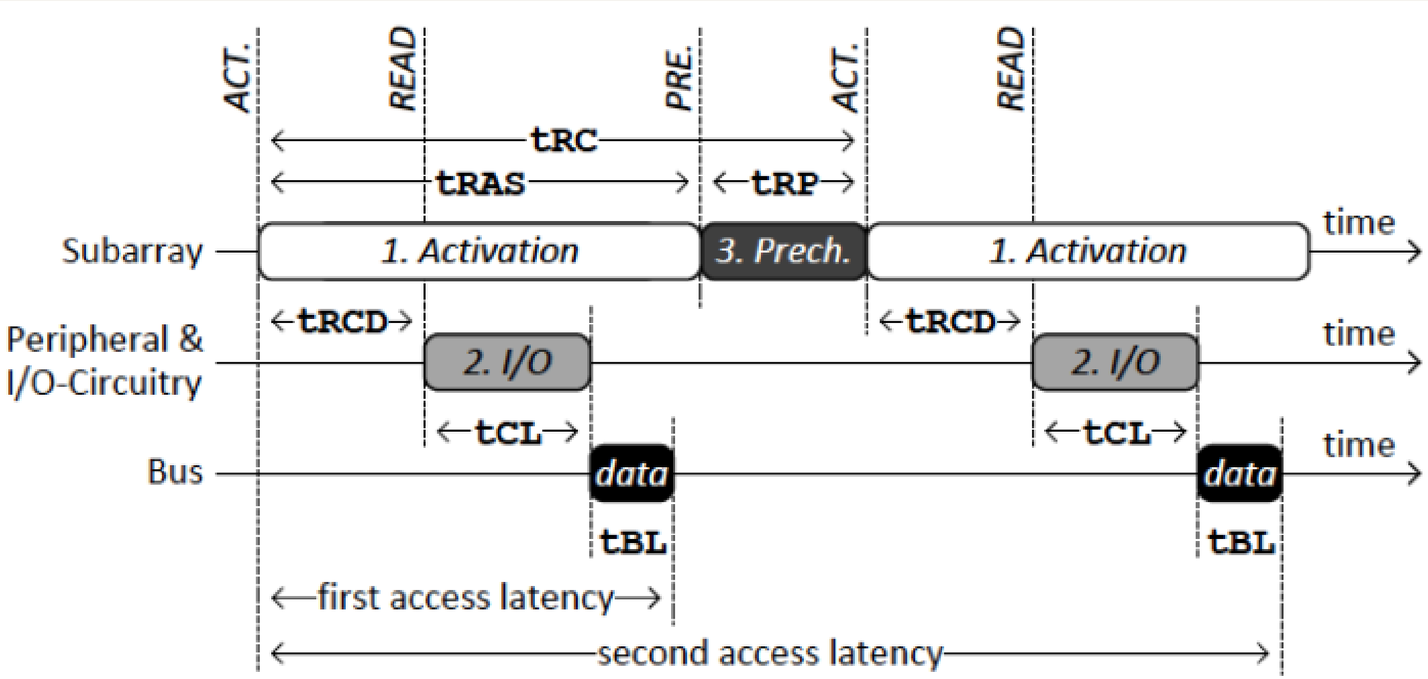


Table 2. Timing Constraints (DDR3-1066)

Phase	Commands	Name	Value
1	ACT → READ ACT → WRITE	tRCD	15ns
	ACT → PRE	tRAS	37.5ns
2	READ → *data* WRITE → *data*	tCL tCWL	15ns 11.25ns
	data burst	tBL	7.5ns
3	PRE → ACT	tRP	15ns
1 & 3	ACT → ACT	tRC (tRAS+tRP)	52.5ns

TRAS - the total time the row would be active until it is closed or precharged

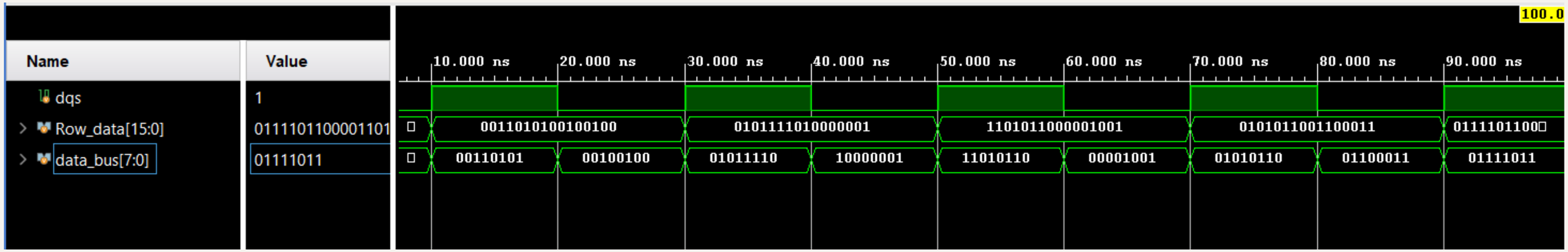
TCAS - the data present in the column would be read or write

TRCD- decoding the column and arranging the internal circuits to perform read or write operation

TBL - the time taken to transfer all the data in bursts

T_PRE - the time taken to write the data present in the row buffer to the respective row and making the sense amplifier bitlines to be precharged.

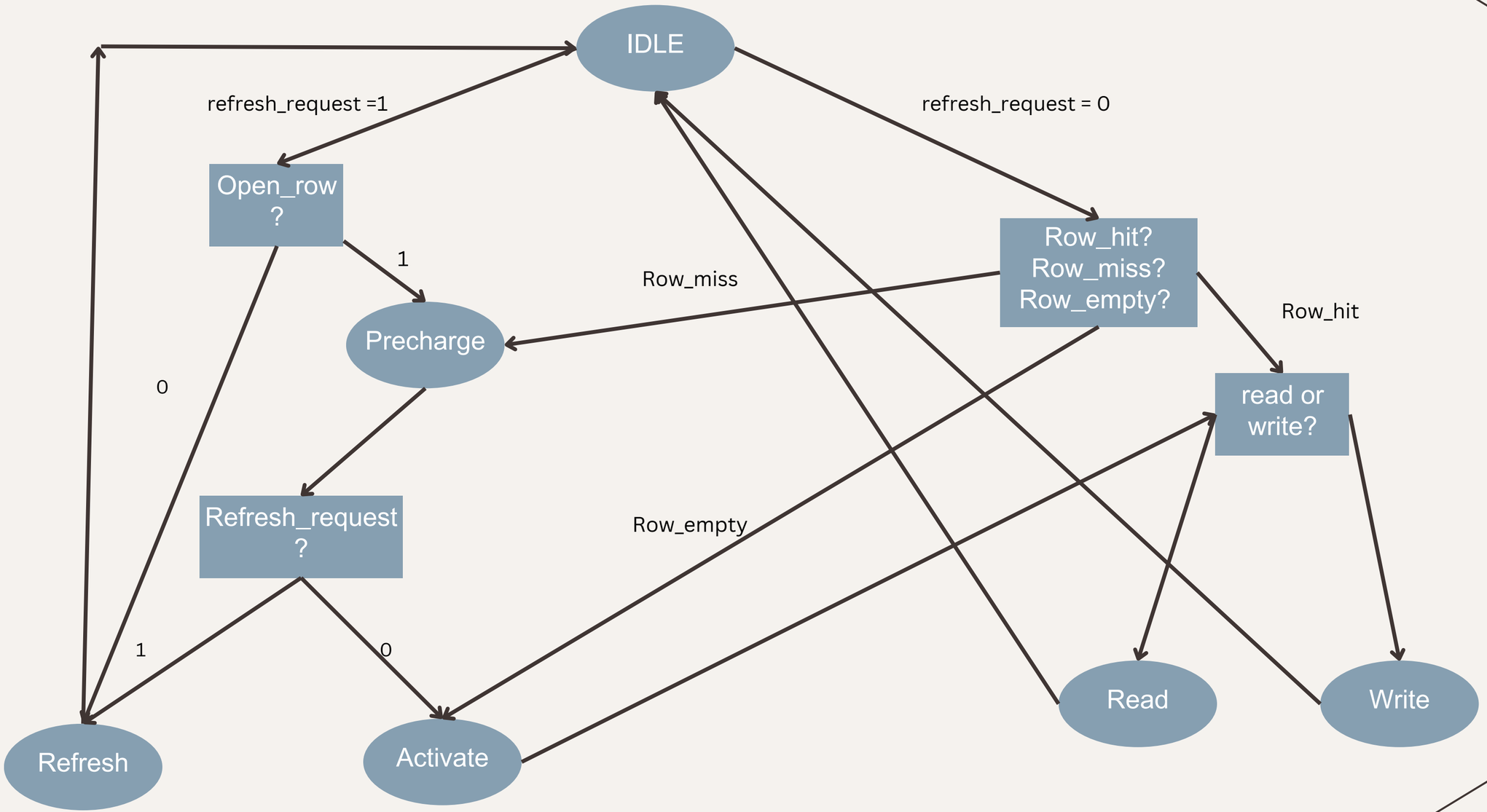
DDR functionaltiy



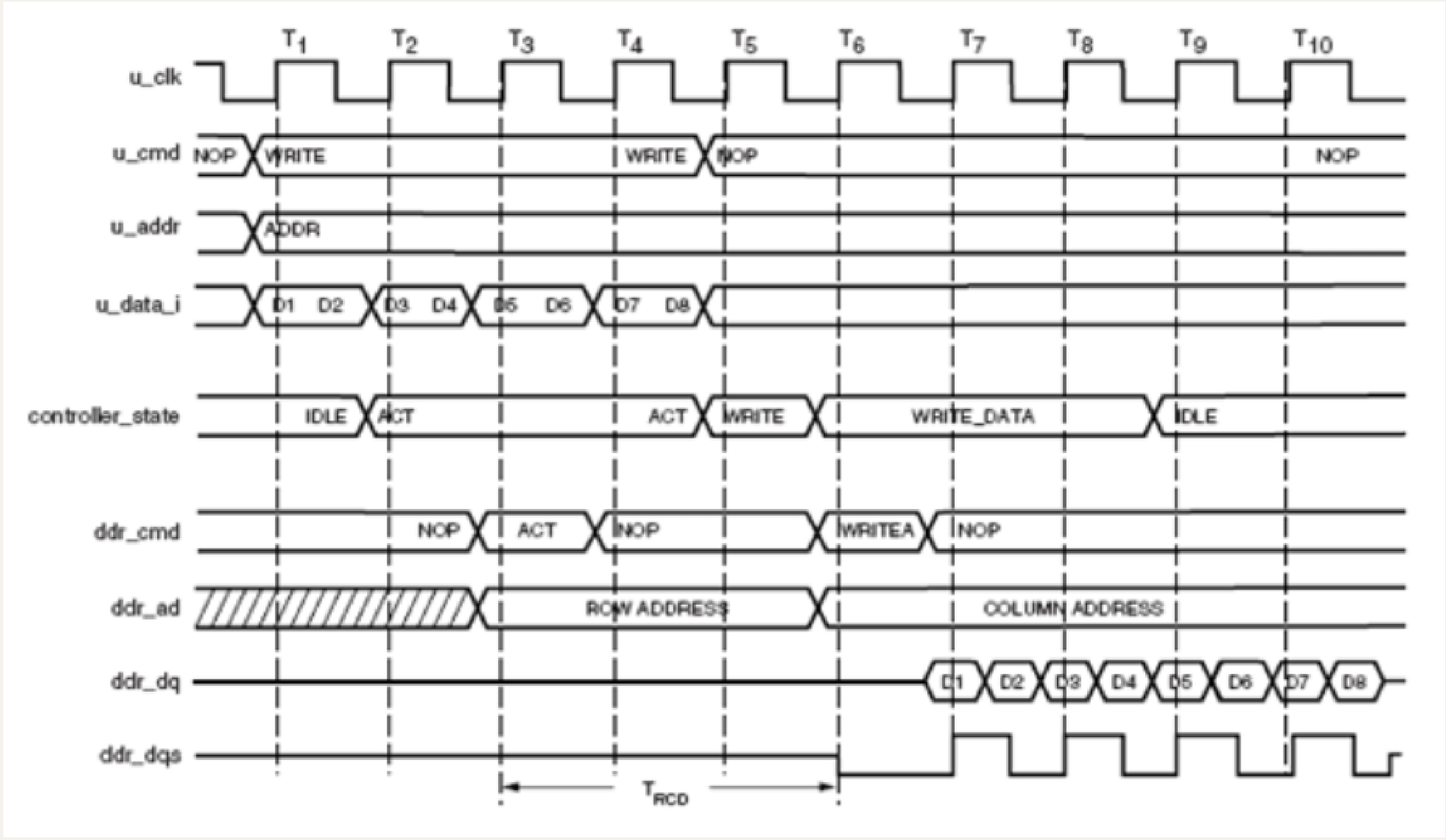
Transfer of the data will be transferred on the both edges of the clock, with the help of dqs signal which would be given by the controller in synchronous to clock, that would tell which data has to be latched.

FSM of the controller

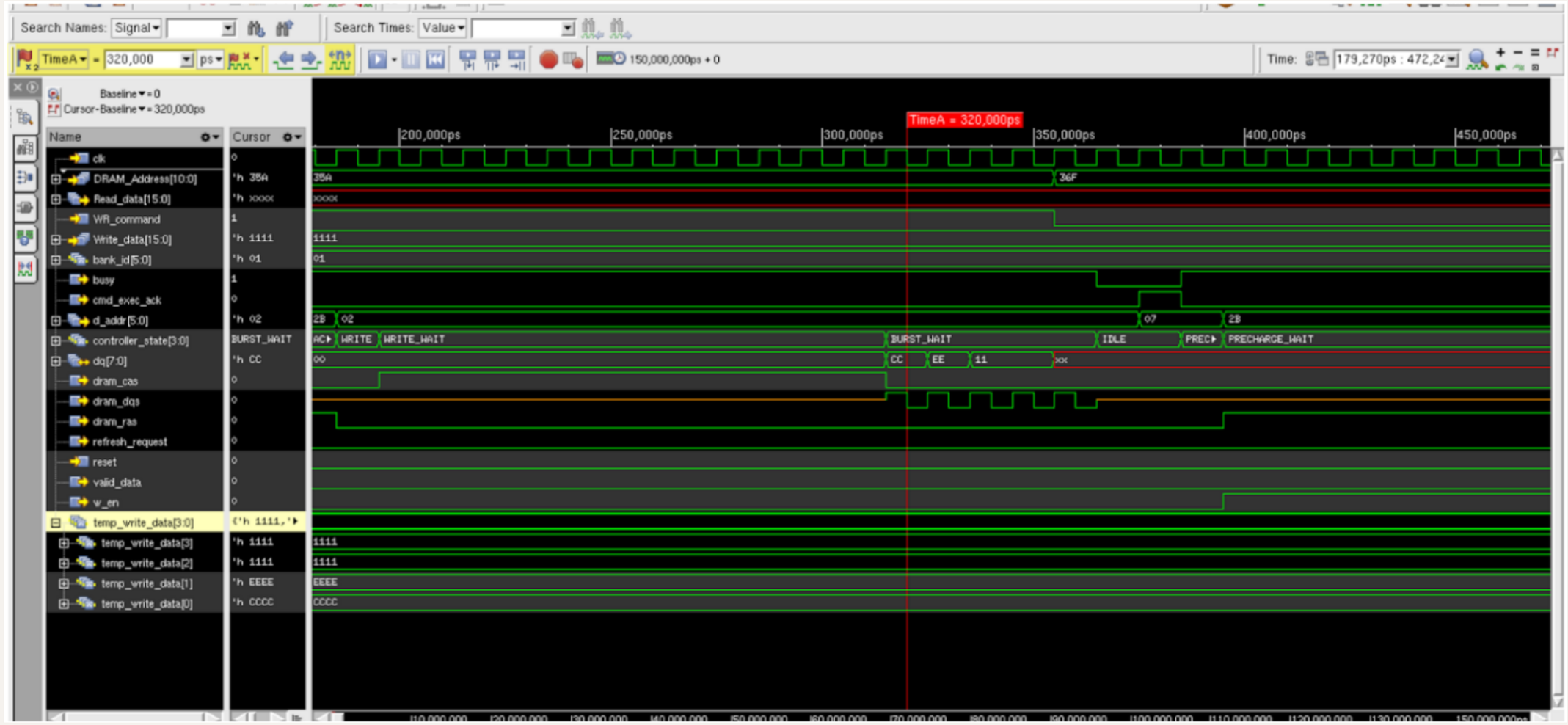
Implemented Open Row policy



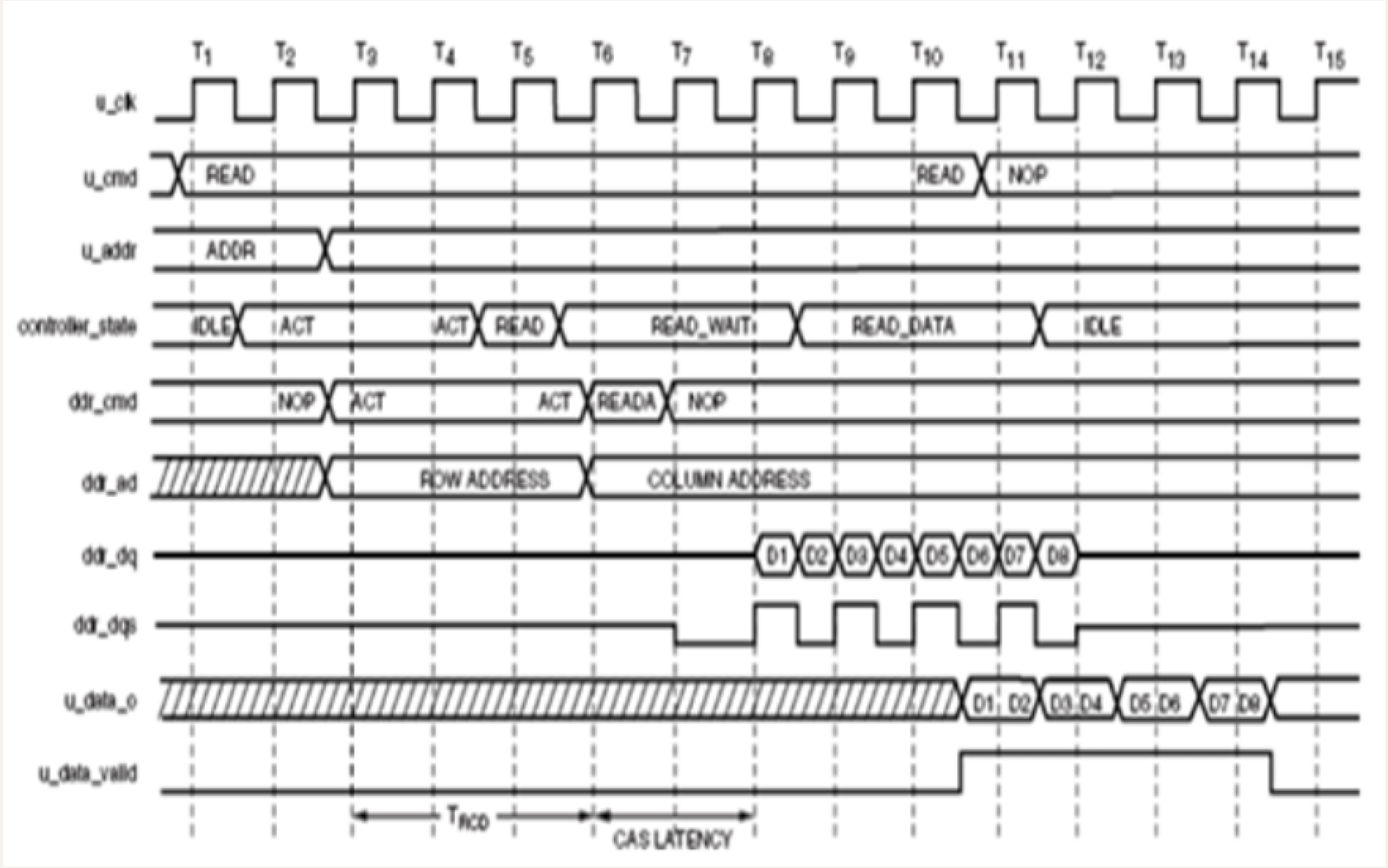
WRITE OPERATION



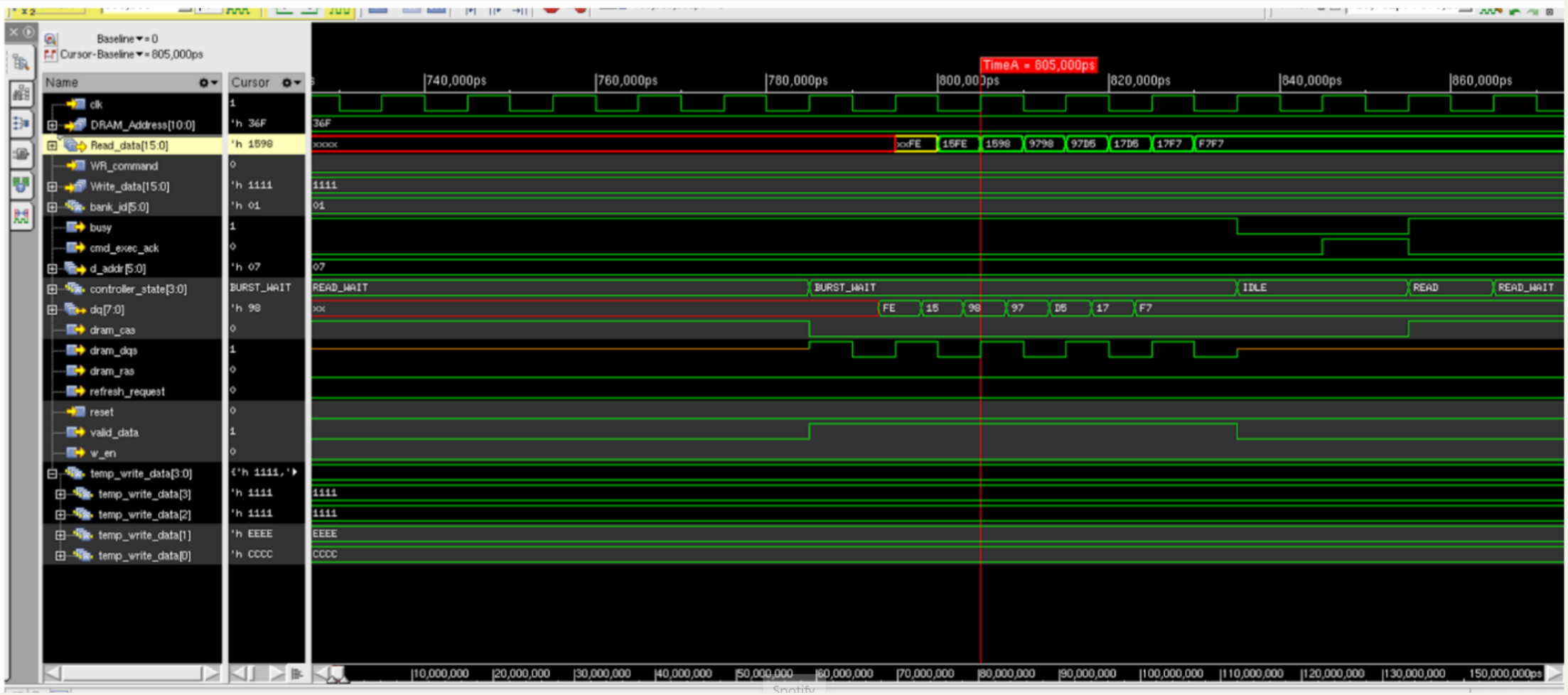
WRITE OPERATION



READ OPERATION



READ OPERATION



TIMING REPORT

```
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 21.10-p002_1
  Generated on:           Apr 16 2023  12:07:00 am
  Module:                 top_DDR_controller
  Technology library:     uk65lscllmvbbr_120c25_tc
  Operating conditions:   uk65lscllmvbbr_120c25_tc (balanced_tree)
  Wireload mode:          top
  Area mode:              timing library
====================================================================

               Pin                              Type       Fanout Load Slew Delay Arrival
                                                             (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------------------------
(clock clk)                                   launch                                 450 F
(create_clock_delay_domain_1_clk_F_0)         ext delay                  +0          450 F
clk                                    (i)    in port         131  0.0    0    +0     450 F
g11823__6131/A                                                           +0     450
g11823__6131/Z                                BUFTM22RA         4 25.6   26   +57     507 F
g15303__4319/A                                                           +0     507
g15303__4319/Z                                ND2M16RA         17 18.4   27   +24     531 R
g15291__15471/B                                                          +0     531
g15291__15471/Z                               ND2M1R            1  1.0   28   +26     556 F
g15218__5107/NA2                                                         +0     556
g15218__5107/Z                                OAI21B10M4R       1  1.4   30   +57     613 F
g15190__6260/A                                                           +0     613
g15190__6260/Z                                ND2M2R            1  1.1   22   +21     634 R
dram_wr_data_reg[7]/D                  <<<    LACQM2RA                           +0     634
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)                                   open                                   450 F
                                              uncertainty                 -10        440 F
dram_wr_data_reg[7]/GB                        borrowed                   +194        634
-------------------------------------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :       0ps
Start-point  : clk
End-point    : dram_wr_data_reg[7]/D

(i) : Net is ideal.
```

POWER REPORT

```
Instance: /top_DDR_controller
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     8.84164e-08  1.30004e-03  5.20234e-05  1.35216e-03  74.12%
       latch     1.41317e-08  2.62233e-05  6.22813e-06  3.24656e-05   1.78%
       logic     5.66538e-08  1.38572e-04  1.08481e-04  2.47110e-04  13.55%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     1.42336e-08  1.61216e-05  1.76307e-04  1.92442e-04  10.55%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     1.73435e-07  1.48096e-03  3.43039e-04  1.82417e-03 100.00%
  Percentage           0.01%       81.19%       18.81%      100.00% 100.00%
  ------------------------------------------------------------------------
```

AREA REPORT

Type	Instances	Area	Area %
sequential	171	1274.400	57.2
inverter	29	33.120	1.5
buffer	5	8.280	0.4
tristate	10	45.360	2.0
logic	345	867.240	38.9
physical_cells	0	0.000	0.0
total	560	2228.400	100.0

THANK YOU