An AI-driven EDA Algorithm-Empowered VCO and LDO Co-Design Method

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Abstract—Traditionally, the output noise and power supply rejection of low-dropout regulators (LDOs) are optimized to minimize power supply fluctuations, reducing their impact on the low-frequency noise of target voltage-controlled oscillators (VCOs). However, this sequential design approach does not fully address the trade-offs between high-frequency and LDO-induced low-frequency phase noise. To overcome this limitation, this paper presents a co-design method for low phase-noise LC-tank VCOs powered by LDOs. It is difficult to carry out the co-design using traditional manual design techniques. Hence, an efficient AI-driven EDA algorithm is used. To validate the proposed method, a 5.6 GHz LC-tank VCO with an integrated LDO is designed using a 65 nm CMOS process. Simulations show that the co-design method improves phase noise by 1.2 dB at a 1 MHz offset and reduces dynamic power consumption by 28.8%, with FoM increased by 2.4 dBc/Hz compared to the conventional sequential design method.

Index Terms—voltage regulator, power supply rejection, voltage-controlled oscillator, phase noise, EDA, AI

I. INTRODUCTION

Voltage-controlled oscillators (VCOs) are crucial components in high performance systems, particularly in wireless communication and radio-frequency applications. One of the major challenges in designing VCOs is optimizing phase noise (PN), which can lead to degraded signal purity and reduced system performance [1]. While traditional approaches have focused on improving the inherent noise performance of the oscillator's core components, such as minimizing thermal and flicker noise in the transistors or enhancing the quality factor of the LC tank, external influences also play a significant role. Power supply noise can introduce additional PN through power supply rejection (PSR) path and VCO's frequency pushing factor [2]. To mitigate this impact, low-dropout regulators (LDOs) are commonly used [3]. However, the LDO itself introduces new challenges, as its low-frequency noise can be up-converted into PN, complicating the overall noise management strategy in VCO designs.

To improve the PN, a natural idea is to design LDO and VCO together. [4] carries out a comprehensive analysis between frequency pushing and power supply-induced PN. Based on the influence of the combined effect of the LDO's PSR and the VCO's inherent phase noise sensitivity to supply
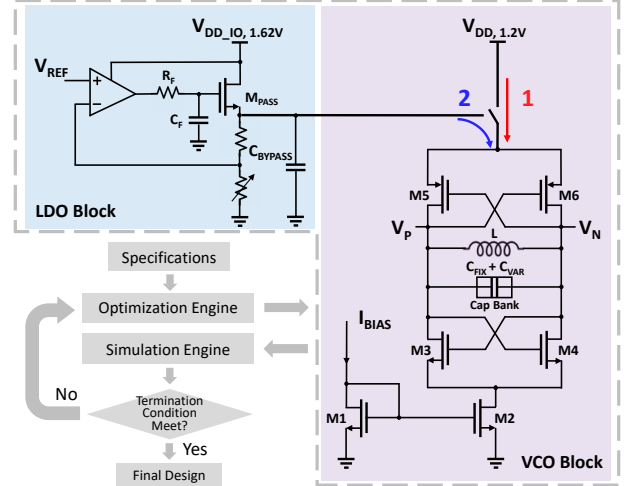
Fig. 1. Abstract of VCO and LDO co-design method including the schematic diagram of the LC-tank VCO with an integrated LDO. Two design approaches: the sequential approach, which involves two distinct design phases, and the co-design approach, which optimizes both building blocks simultaneously.

noise, the guidelines of LDO design are obtained. Reducing the width of the VCO's switching device is suggested in [4], which mitigates the frequency pushing effect. However, this may increase thermal noise, potentially degrading the VCO's PN performance at higher frequencies. Therefore, a holistic approach to obtain the optimal trade-off considering various kinds of noise is needed to obtain the truly optimal design.

For the traditional manual design method, it can be challenging to derive formulas due to the complex trade-offs described above. Hence, this paper presents an LDO and VCO co-design method empowered by an AI-driven EDA algorithm called efficient surrogate model-assisted sizing method for high-performance analog building blocks (ESSAB) [5]. The method optimizes the PN of an LC-tank VCO and the PSR of an integrated LDO while also accounting for PVT corners. Notably, while most existing AI-driven design research focuses on individual analog building blocks, this work emphasizes subsystem-level co-design, offering a more holistic and effective optimization approach.

To validate the proposed co-design method, a 5.6 GHz LC-tank VCO, regulated by an LDO, is designed using a

65 nm CMOS process. Simulation results show that the co-design approach improves the VCO's phase noise by 1.2 dB at a 1 MHz offset and reduces dynamic power consumption by 28.8%, with FoM increased by 2.4 dBc/Hz compared to the traditional sequential design approach using the same AI-driven EDA algorithm.

The paper is structured as follows: Section II presents the building blocks for the targeted LDO-VCO. Section III explains the implementation details of co-design method. Section IV compares the designs obtained by the traditional sequential method and the co-design method. Conclusions are presented in Section V.

II. ARCHITECTURE OF LDO-VCO

A diagram of an LDO-regulated VCO is shown in Fig. 1, where a cross-coupled LC-tank VCO is adopted [6]. The LC tank comprises an inductor, capacitor, and a varactor array. In parallel, the cross-coupled transistor pairs produce negative resistance to counteract the losses present in the LC tank. The LDO on the top provides the load current needed for the VCO. It consists of an error amplifier, a low-pass filter, an NMOS pass transistor, and a feedback divider. The error amplifier is implemented using a two-stage Miller-compensated op-amp. In addition, a bypass capacitor is used at the LDO output.

III. AI-DRIVEN CO-DESIGN METHOD

A. Setup of the Sizing Problem

1) Design Variables: Table I details the ranges of the 43 design variables, where W, R, NT, S, GR denotes the width, inner radius, number of turns, spacing between conductors and guard ring width of the inductor; L, W, F, M represent the channel length, width per finger, number of fingers and number of multiplier of the transistors; N_H, N_V, and M_{bot} represent the number of horizontal fingers, vertical fingers, and bottom starting layer for the MOM capacitors in the VCO. The inductor and MOM capacitor are implemented using PDK components. The biasing circuits for VCO and LDO, the LDO feedback divider, the varactor and the bypass capacitor are maintained constant.

2) Testbench and Measures: A 65 nm CMOS process is used. The VCO varactor is set to work at its highest frequency where supply pushing is the highest. The performance metrics include oscillation frequency f_0, phase noise $PN(\Delta f)$ at frequency offsets Δf of 100 kHz, 1 MHz and 10 MHz, total power consumption P_{dyn}, and the FoM at 1 MHz frequency offset [7]:

$$FoM = -10\log[(\frac{\Delta f}{f_0})^2 \cdot \frac{P_{dyn}}{1mW}] - PN(\Delta f), \quad (1)$$

Additionally, the maximum PSR, phase margin (PM), and maximum V_{DD} are extracted. The process corners considered include fast NMOS/fast PMOS, fast NMOS/slow PMOS, slow NMOS/slow PMOS, and slow NMOS/fast PMOS in combination with min inductor/max inductor and min capacitor/max capacitor. $-55°C$ and $125°C$ are considered as temperature corners. And the lowest supply voltage V_{DD_IO} (1.8 V · 90%) is used. In total, 32 corners are considered.

TABLE I
DESIGN VARIABLES AND SEARCH RANGES OF THE CMOS CROSS-COUPLED LC OSCILLATOR AND THE LDO.

	Var.	Unit	Lower bound	Upper bound	Co-design	Se-design
VCO	M_2	integer	1	1000	300	872
	$L_{3,4}$	m	60n	240n	225n	239n
	$W_{3,4}$	m	1u	6u	1.22u	4.60u
	$F_{3,4}$	integer	2	32	7	10
	$M_{3,4}$	integer	1	10	8	2
	$L_{5,6}$	m	60n	240n	205n	75n
	$W_{5,6}$	m	1u	6u	1.96u	1.72u
	$F_{5,6}$	integer	2	32	11	13
	$M_{5,6}$	integer	1	10	6	10
	N_H	integer	10	200	74	94
	N_V	integer	10	200	95	88
	M_{bot}	integer	1	3	1	1
	W	m	3u	30u	28.2u	27.9u
	R	m	15u	90u	89.4u	76.6u
	N	integer	1	3	1	1
	S	m	2u	4u	2.67u	3.18u
	GR	m	10u	40u	28.7u	21.7u
LDO	L_{nLoad}	m	500n	10u	6.64u	8.28u
	W_{nLoad}	m	400n	10u	3.93u	500n
	F_{nLoad}	integer	2	32	25	3
	M_{nLoad}	integer	1	10	2	2
	L_{pIn}	m	400n	10u	5.95u	470n
	W_{pIn}	m	400n	10u	3.25	1.43
	F_{pIn}	integer	2	32	29	5
	M_{pIn}	integer	1	10	5	1
	L_{bias}	m	400n	10u	5.55u	3.63u
	W_{bias}	m	400n	10u	4.58u	9.14u
	F_{bias}	integer	2	32	14	22
	M_{bias}	integer	1	10	7	9
	M_{biasIn}	integer	1	10	5	6
	$M_{biasOut}$	integer	1	10	8	1
	L_{nOut}	m	500n	10u	2.53u	3.42u
	W_{nOut}	m	400n	10u	2.08u	6.35u
	F_{nOut}	integer	2	32	31	20
	M_{nOut}	integer	1	10	7	7
	C_C	F	1p	100p	67p	60p
	R_C	ohm	1	1M	989K	514K
	C_F	F	1p	200p	182p	156p
	R_F	ohm	1	2M	1.66M	1.17M
	L_{pass}	m	1.2u	10u	1.69u	1.62u
	W_{pass}	m	500n	10u	8.86u	5.96u
	F_{pass}	integer	2	100	47	35
	M_{pass}	integer	1	32	15	15

3) Objective and Constraints: The targeting oscillation frequency is 5.5 GHz with a power consumption less than 7 mW. The phase noise constraints at 100 kHz, 1 MHz and 10 MHz are set to be -94 dBc/Hz, -120 dBc/Hz, and -140 dBc/Hz respectively, which meet industrial standards. The optimization objective for both approaches is FoM. The remaining performance parameters are set as constraints. These apply to all 32 corners.

B. Sizing Flow and Considerations

For the sequential design method, the VCO is first optimized independently with an ideal 1.2 V power supply to achieve an optimal FoM, as illustrated in Fig. 1. The LDO is then incorporated and optimized for this VCO load to generate

a clean supply. Although this approach seems intuitive, the primary challenge lies in preventing the LDO noise from being upconverted and affecting the PN of the VCO. To mitigate these, the VCO may need to be re-designed to reduce its sensitivity to the noise introduced by the LDO. This iterative process often requires multiple sizing loops, which can be time-consuming and labor-intensive. Additionally, a bypass capacitor is typically used to reduce high-frequency supply noise, but its impact is often overlooked in the sizing stage of VCO. Not considering this can lead to discrepancies between the designed and measured PN performance due to changed VCO's voltage swing.

To address above issues, a simultaneous co-design of the LDO and VCO is implemented. By treating them as an integrated system rather than separate blocks, mutual interaction is considered throughout the design process, ensuring that the contributors are jointly optimized to minimize PN. Fig. 1 presents the whole sizing flow.

C. Sizing Algorithm

The ESSAB algorithm based on a single objective Bayesian optimization framework is used for both the sequential and co-design methods for a apple-to-apple comparison. It starts by initializing a database and iteratively refining designs until a predefined stopping criterion is met. Each iteration involves selecting the top candidate and applying differential evolution operations. An online ANN model and beta ranking are used to guide the selection of the most promising candidate for simulation. The steps are abstracted as Algorithm 1 and algorithm details can be found in [5].

Algorithm 1 Optimization Framework

1: Initialize Database
2: Finish ← false
3: **while** Finish = false **do**
4:    Rank and select top λ designs
5:    Apply Differential Evolution (DE) operations
6:    Train ANN and predict performance
7:    Select best predicted design and simulate
8:    **if** Stopping criterion met **then**
9:        Finish ← true
10:    **else**
11:        Update Database
12:    **end if**
13: **end while**
14: Output Final Design

IV. PRE-LAYOUT SIZING RESULTS AND ANALYSIS

Using Cadence Virtuoso and ESSAB tool implemented in MATLAB on a workstation with an AMD Ryzen Threadripper PRO 3975WX (32 cores, 290 GB RAM), the sequential method used 18 hours in total with 7 hours in VCO sizing and 11 hours in LDO sizing, while the co-design method used 6 hours in total. The sizing details for the obtained designs are provided in Table 1, labeled as co-design and se-design, respectively. The pre-layout simulation results are summarized in Table II. The results of nominal corner and the corner with

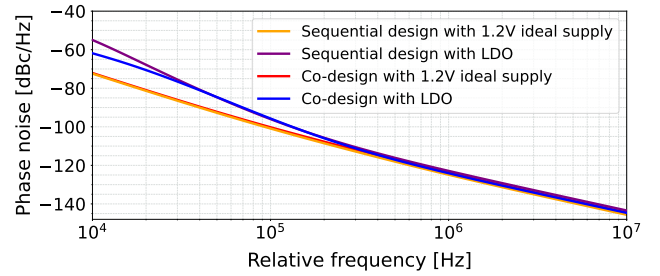| Symbol	Specs.	Se-design (Nominal)	Co-design (Nominal)	Se-design (Worst corner)	Co-design (Worst corner)
FoM (dBc/Hz)	Minimize	−190	−192.4	−187.3	−187.8
Frequency (GHz)	≥ 5	5.69	5.60	5.35	5.27
PN@100kHz (dBc/Hz)	≤ −94	−96.2	−95.6	−93.8	−92.0
PN@1MHz (dBc/Hz)	≤ −120	−122.9	−124.1	−120.9	−119.7
PN@10MHz (dBc/Hz)	≤ −140	−143.4	−144.7	−142	−141.5
P_{dyn} (mW)	≤ 7	6.40	4.56	6.60	4.33
PSR_{max} (dB)	≤ −30	−33.7	−31.4	−31.6	−31.0
$V_{DD,max}$ (V)	≤ 1.32	1.24	1.23	1.24	1.23
PM (°)	≥ 50	67	82	59	81

Fig. 2. Phase noise performance of the VCO designs with 1.2 V ideal supply and with LDO.

slow NMOS/slow PMOS, max inductor and max capacitor at 125°C (worst corner) are listed.

To assess the impact of LDO in two approaches, the LDO output noise and PSR are analyzed. In addition, the VCO phase noise is extracted under two conditions: 1) powered by a 1.2 V ideal voltage source, and 2) powered by the LDO with a 1.62 V DC input and a 1.2 V output voltage.

At a 100 kHz offset, the LDO noise significantly deteriorates the VCO phase noise. The primary contributor to the LDO noise differs between the two designs: For the co-designed LDO, the main source of noise is the thermal noise from the NMOS load in the input stage. For the sequential design, the primary contributor is the thermal noise from the PMOS input pair. In the PMOS input pair, the transconductance (g_m) is 61.89 μS for the sequential design and 73.42 μS for the co-designed LDO. For the NMOS load, g_m is 73.9 μS in the co-designed case, compared to 18.7 μS for the sequential design, resulting in higher output noise for the co-designed LDO. Further, as shown in Fig. 2, the co-designed VCO with ideal supply has a slightly worse PN at 100 kHz due to the smaller switching transistors. With LDO's output noise, the co-designed system exhibits worse phase noise performance at the 100 kHz offset, with −95.6 dB compared to −96.2 dB.

At 1 MHz offset, the primary contributor to phase noise is the thermal noise from the switching transistors, while the flicker noise of transistors M3-M6 dominates across corners. With ideal supply, M5 and M6 have five times smaller W/L in the co-designed VCO, which reduces the effective transcon-
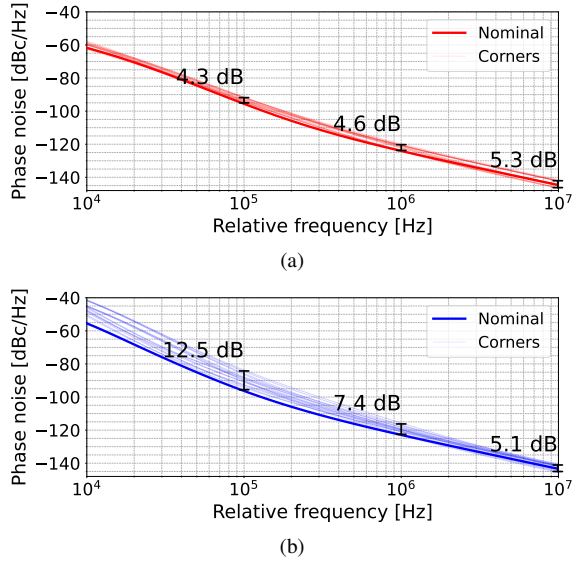
Fig. 3. (a) Corner spread of PN for the co-designed LDO-VCO. (b) Corner spread of PN for the sequentially designed LDO-VCO.

Fig. 4. Co-designed LDO-VCO layout.

Symbol	Specs.	Co-design (Nominal)	Co-design (Worst corner)
FoM (dBc/Hz)	Minimize	-192.1	-187.8
Frequency (GHz)	≥ 5	5.51	5.19
PN@100kHz (dBc/Hz)	≤ -94	-95.9	-96.8
PN@1MHz (dBc/Hz)	≤ -120	-123.9	-119.1
PN@10MHz (dBc/Hz)	≤ -140	-144.3	-139.3
P_{dyn} (mW)	≤ 7	4.67	3.59
PSR (dB)	≤ -30	-30.2	-30.1
$V_{DD,max}$ (V)	≤ 1.32	1.22	1.22
PM ($^\circ$)	≥ 50	82	81

ductance of the switching pairs, resulting in higher thermal noise and 1 dB worse PN than se-design. However, with LDO incorporated, the PN performance of the se-design degrades from 124.9 dBc/Hz to 122.9 dBc/Hz, partly due to frequency pushing mechanism, which is significantly suppressed in the co-design. Consequently, the co-design achieves a 1.2 dB PN reduction at a 1 MHz offset and a 1.3 dB improvement at 10 MHz with the LDO incorporated. Additionally, the power consumption is reduced due to the lowered total capacitance at the output nodes. The decrease in transconductance reduces the current flowing to the LC tank and affects the startup time. However, the startup is still achieved reliably across corners thanks to the corner analysis during optimization.

In the sequentially designed LDO-VCO, the effect of the bypass capacitor is not well accounted for in the VCO design. To maintain low phase noise, the supply voltage swing is kept large. However, when a bypass capacitor is added at the V_{DD} of the VCO, it flattens the voltage swing, which worsens the optimized phase noise performance. In contrast, the co-design approach considers the impact of the decoupling capacitor from the start. This approach constrains the reliance on voltage swings, resulting in lower phase noise. The inclusion of a bypass capacitor also degrades the VCO phase noise across corners. According to Fig. 3, the pre-designed VCO exhibits a much larger variation in phase noise when the LDO and bypass capacitor are included. In contrast, the co-designed VCO shows a more consistent performance. Overall, the co-design approach leads to a better FoM of 2.4 dBc/Hz and superior performance across corners by accounting for block interactions and multiple effects.

The layout was manually implemented, shown in Fig. 4. The post-layout simulation results are presented in Table III. The impact of layout on the FoM is limited to 0.3 dB, which is caused by the routing parasitics in the V_P and V_N nets.
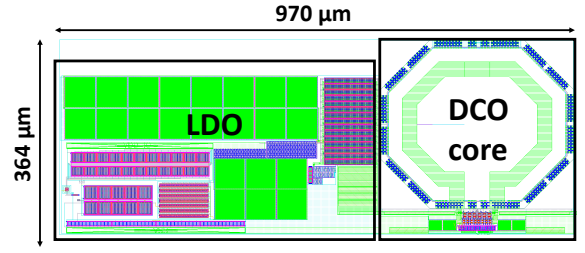
V. CONCLUSION

This paper has presented a VCO and LDO co-design method for PN reduction and performance enhancement, which is empowered by ESSAB. Compared to the traditional sequential design method, the proposed approach improves the FoM by 2.4 dB, highlighting its ability to consider analog building block interactions and trade-offs to optimize overall performance.

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