

A beyond 60GHz Cross-Coupled Fundamental VCO in 45nm CMOS

Alex Katz⁽¹⁾, Ofir Degani⁽¹⁾, Yosi Shacham-Diamand⁽²⁾ and Eran Socher⁽²⁾

(1) Intel, Wireless division, Israel, Alex.A.Katz@Intel.com

(2) Tel-Aviv University, Israel

Abstract - A beyond 60 GHz cross-coupled NMOS differential LC CMOS VCO is presented in this paper, which is implemented in 45nm standard CMOS technology. Working with a supply voltage of 1.2 V the circuit draws a current of 38mA (72mA including output buffer) and requires a circuit area of 0.037 mm² including the differential output buffer without pads. The circuit delivers an output power of -9dBm to -11dBm and yields a measured phase noise of -100.02dBc/Hz at 10MHz offset. The VCO offers a frequency tuning range of 0.2GHz, while statistical process variation is manifested in a 4.5GHz VCO central frequency drift for different measured samples (from 68GHz to 72.5GHz).

Index Terms – voltage-controlled oscillators (VCO), push-push, cross-coupled, CMOS, phase noise.

I. INTRODUCTION

There are growing demands in millimeter-wave and upper millimeter-wave electronics for various applications, especially V-band radio (57 to 64 GHz according to FCC). V-band systems are primarily used for high capacity; short distance (less than 1 mile, because high oxygen absorption in this band) communications. The use of other frequency bands beyond 60 GHz offers advantages such as smaller antenna and chip sizes and unlicensed spectrum usage.

Due to increasing process variation in sub-90nm technologies, VCO designs in advanced CMOS processes are expected to require statistical design for functional yield, in addition to common VCO performance specifications. In this work we demonstrate a 70GHz VCO in 45nm CMOS technology and evaluate the variability in its oscillation frequency.

II. SIGNAL SOURCES

A voltage-controlled oscillator (VCO) is a mandatory part of each communication system – wireless and wired. A critical issue for a signal source is stability and must be locked using a phase locked loop (PLL).

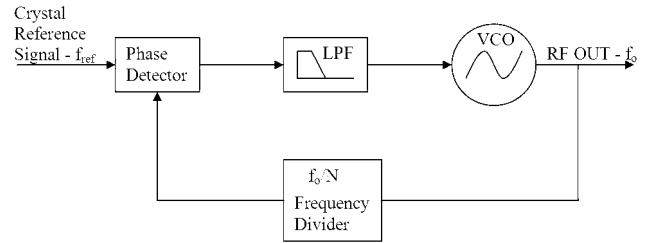


Fig.1. Basic PLL block scheme

As the feature size of the transistors continues to shrink - f_t increasing, CMOS VCO operating at low millimeter-wave region has become feasible and replaces compound III-V column semiconductors.

Each oscillator can be presented as negative-resistance model with unequivocal defined conditions.

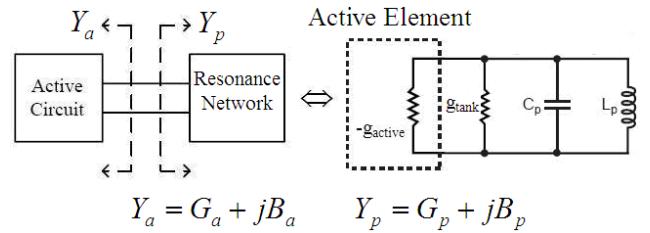


Fig.2. Negative-resistance model block scheme

start-up criteria

$$\begin{aligned} |G_a(\omega_0)| &> |G_f(\omega_0)| \\ B_a(\omega_0) + B_f(\omega_0) &= 0 \end{aligned} \quad (1)$$

steady state criteria

$$\begin{aligned} |G_a(\omega_0)| &= |G_f(\omega_0)| \\ B_a(\omega_0) + B_f(\omega_0) &= 0 \end{aligned} \quad (2)$$

In general, two main kinds of LC VCO are useful in mm-waves range - fundamental and push-push techniques.

Push-push output is even harmonic (usually second) of the fundamental differential signal. Even harmonics behavior is common mode and it causes push-push output to be single-ended.

Typically, the realization of fundamental oscillators at a desired frequency is restricted by the cut-off transistors frequency and quality factor of the passive elements – tank's losses increase with frequency.

Push-push topology is overcoming this frequency issue, but causes other design limitation; single-ended output phase, instead of intrinsic differential output in fundamental VCO, reduced output RF power (second harmonic power) and significant more design size, because passive elements.

Result of these considerations, fundamental VCO technique in most cases more preferable as integrated part of communication system, if possible to generate necessary frequency.

III. CIRCUIT DESIGN

The simplified circuit schematic of the cross-coupled differential LC oscillator and differential buffer drives VCO outputs are shown in Fig. 3 and Fig.4 respectively. Cross-coupled NMOS transistors (M1, M2) are forming the VCO core. Accumulation MOS (AMOS) varactors are used for frequency tuning with series MOM capacitors for higher quality factor (Q). The Q of this branch over the tuning range achieves values between 11 and 22 (AMOS only provide Q between 6 to 17). The VCO core inductor, that has been modeled using an electromagnetic simulator, is a coplanar transmission line in the top layer of the 6-metal stuck with radius of 20 μ m, yielding a 75 pH loop inductance with a differential Q of 23 at 60GHz. The significant interconnects in the layout have been modeled in the EM simulations as well. Total worst case Q of the VCO tank at 60GHz obtained ~10 as shown in Fig.7. To ensure startup of the VCO, the negative transconductance of the cross-coupled pair, which should have a larger absolute value than the total loss conductance at 60GHz, is oversized with a factor ~3, as shown in Fig.5 and Fig.6. Pre-layout simulations over all possible process corners showed up to 3GHz central frequency drift.

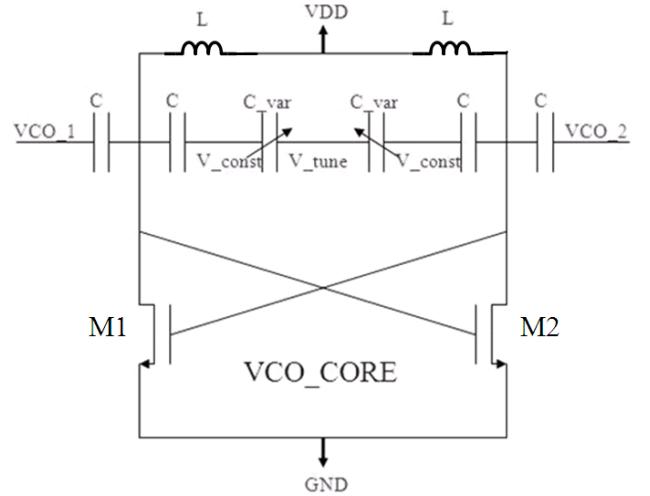


Fig.3. Cross-coupled NMOS VCO

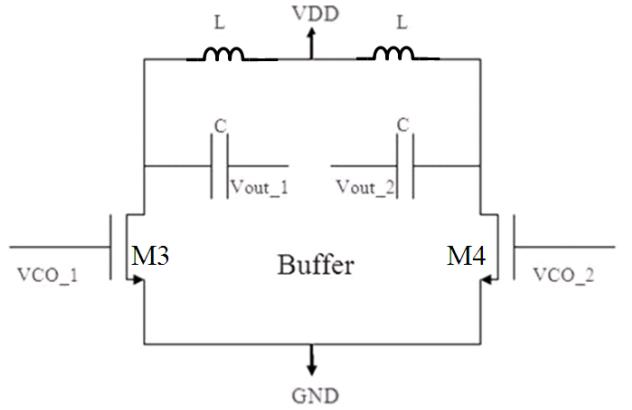


Fig.4. Output differential buffer

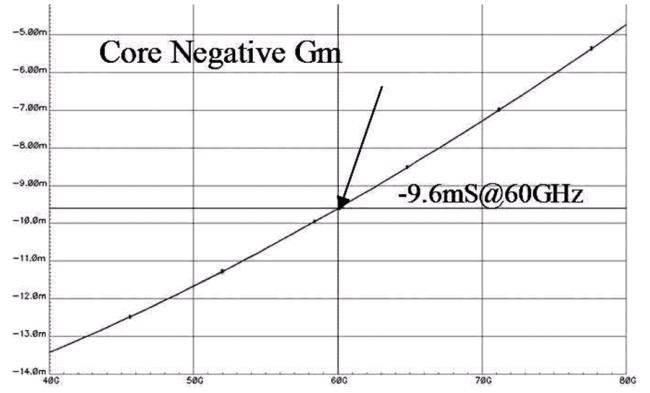


Fig.5. Core negative Gm

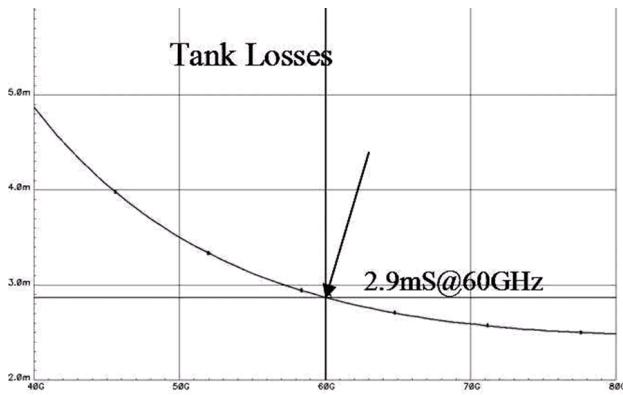


Fig.6. Tank Losses

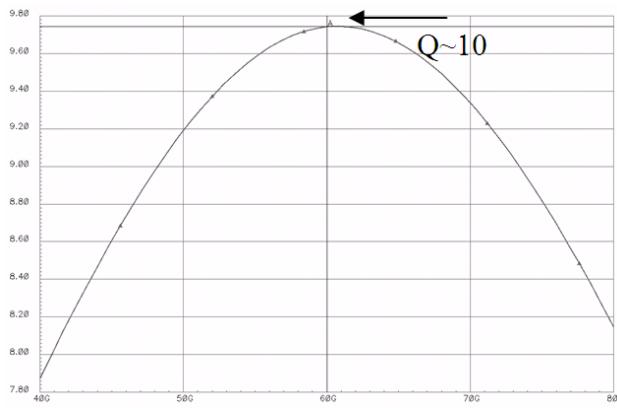


Fig.7. Q of the VCO tank

IV. RESULTS

The proposed fundamental VCO circuit is implemented in a 45nm CMOS commercial process. The chip, shown in Fig. 10, was characterized using on-chip probing and a V-band harmonic mixer and spectrum analyzer test setup. The VCO core consumes 38mA (VDD = 1.2V) and achieves a phase noise -100.02dBc/Hz at 10MHz. The tuning range is 0.2GHz and the output power is -9dBm to -11 dBm. Measured output spectrum and phase noise are shown in Fig.8 and Fig.9 respectively. Measured results show a wider range of output frequencies due to process variability amounting to 4.5 GHz compared to the simulated 3GHz and observed on 8 different samples. These results are compared in Table I to state of the art CMOS VCOs at frequencies above 50GHz.

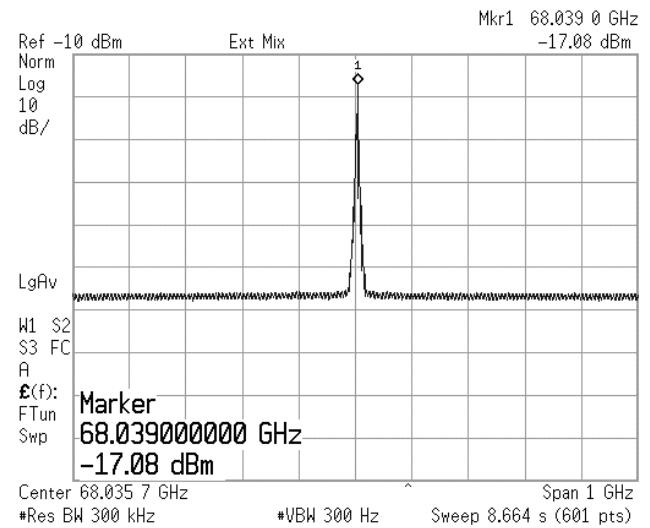


Fig.8. Measured output spectrum at 68GHz without probe and cable loss compensation

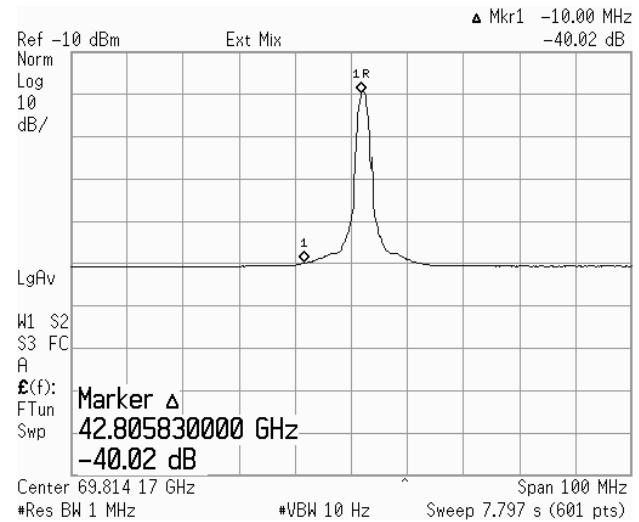


Fig.9. Measured phase noise at 69.8GHz frequency.

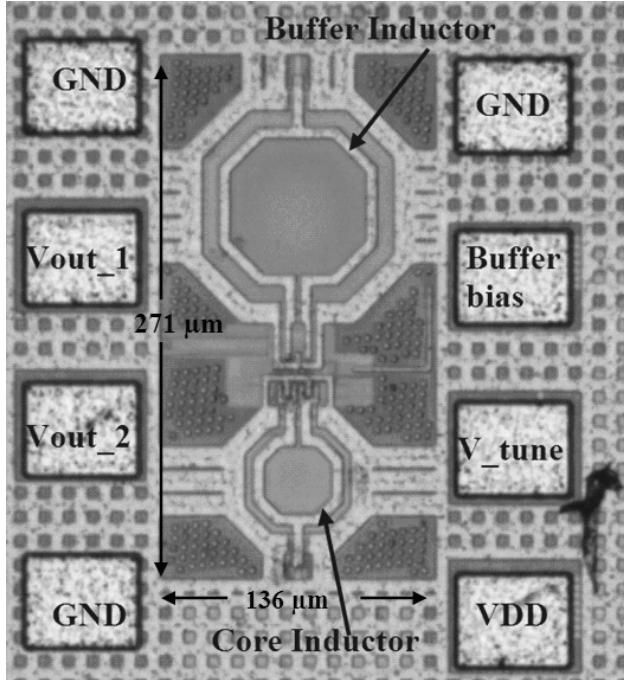


Fig.10. Photograph of the VCO with buffer chip.

V. SUMMARY

A 70 GHz CMOS VCO has been presented in this paper. Wide statistical process drift was observed for this technology node and must be taken into account for the VCO design additional to the common considerations.

TABLE I
STATE-OF-THE-ART CMOS VCOs OVER 50GHz

Ref#	Technology	Center Frequency [GHz]	Tuning Range[GHz]	Power Consumption(mW)	Output Power(dBm)	Phase Noise (dBc/Hz)
[1]	90nm CMOS	103.9	---	30	-65	-110@10MHz*
[2]	90nm SOI	56.5	8.4	21	-6.8	-92@1MHz
[3]	65nm SOI	70.2	6.7	5.4	-35	-106.14@10MHz
[4]	0.13μm CMOS	105.2	0.2	7.2	-25	-97.5@10MHz
[4]	0.13μm CMOS	59	5.8	9.8	---	-89@1MHz
[5]	0.12μm CMOS	51.5	0.7	1	-30	-85@1MHz
[6]	90nm CMOS	60	0.1	1.9	---	-100@1MHz
[7] **	45nm CMOS	61.5	9	78	---	-82@3MHz
[8]	90nm CMOS	139.6	1.2	---	-19	-85@2MHz
[This Work]	45nm CMOS	70	0.2	45	-10	-100.02@10MHz

* - Based on measurements, but back-calculated with help of simulations to refer back to VCO's core

** - Two quadrature VCOs

REFERENCES

- [1] L. M. Franca-Neto, R.E. Bishop, B.A. Bloechel, "64GHz and 100GHz VCOs in 90nm CMOS Using Optimum Pumping Method," ISSCC Dig. Tech. Papers, pp. 444-445, Feb., 2004.
- [2] F. Ellinger, T. Morf, G. Buren, "60GHz VCO with Wideband Tuning Range Fabricated on VLSI SOI CMOS Technology," IEEE Int. Microwave Symp. Dig. Papers, pp. 1329-1332, Jun., 2004.
- [3] Daeik D. Kim, Jonghae Kim1, Jean-Olivier Plouchart, "A 70GHz Manufacturable Complementary LC-VCO with 6.14GHz Tuning Range in 65nm SOI CMOS" ISSCC Dig. Tech. Papers, pp. 540-541, Feb., 2007.
- [4] C. Cao, K. K. O, "Millimeter-Wave Voltage Controlled Oscillators in $0.13\mu\text{m}$ CMOS Technology," IEEE J. Solid-State Circuits, vol. 41, pp. 1297- 1304, Jun., 2006.
- [5] M. Tiebout, H.-D. Wohlmuth, W. Simburger, "A 1V 51GHz Fully-Integrated VCO in $0.12\mu\text{m}$ CMOS," ISSCC Dig. Tech. Papers, pp. 300-301, Feb., 2002.
- [6] Daquan Huang, et. al. "A 60GHz CMOS VCO Using On-Chip Resonator with Embedded Artificial Dielectric for Size, Loss and Noise Reduction" ISSCC Dig. Tech. Papers, pp. 314-315, Feb 2006
- [7] K. Scheir, G. Vandersteen, Y. Rolain, P. Wambacq "A 57-to-66GHz Quadrature PLL in 45nm Digital CMOS" ISSCC 2009, Solid-state circuits conference - Digest of technical papers.
- [8] Kenneth K. O, M. C. Frank Chang, Michael Shur, and Wojciech Knap "Sub-Millimeter Wave Signal Generation and Detection in CMOS" Microwave Symposium Digest, 2009. MTT '09.