A Project Report on

DESIGN AND IMPLEMENTATION OF LOW RECOIL NOISE AND HIGH SPEED THREE STAGE COMPARATOR

Submitted in partial fulfillment of the requirements for the award of the Degree of

BACHELOR OF TECHNOLOGY

In

ELECTRONICS AND COMMUNICATION ENGINEERING

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SRI VASAVI ENGINEERING COLLEGE

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CERTIFICATE

This is to certify that the project report entitled "**DESIGN AND IMPLEMENTATION OF LOW RECOIL NOISE AND HIGH SPEED THREE STAGE COMPARATOR**" being submitted by the students **M. Chaitanya Ram (19A81A0429), B. Ganesh Sai (19A81A0404), Ch. Uma(19A81A0405), B. Rajesh (19A81A0402)** in partial fulfillment for award of the degree of **Bachelor of Technology** in **Electronics and Communication Engineering** for the academic year 2022-2023 from **Sri Vasavi Engineering College,** Tadepalligudem, affiliated to the **Jawaharlal Nehru Technological University, Kakinada (JNTUK),** Recognized by A.I.C.T.E, New Delhi, Accredited by NBA & NAAC with 'A' Grade is a record of bonafide work carried out by them under my guidance and supervision.

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We hereby declare that the project entitled "**DESIGN AND IMPLEMENTATION OF LOW RECOIL NOISE AND HIGH SPEED THREE STAGE COMPARATOR"** is submitted in partial fulfillment of the requirements for the award of Degree of **Bachelor of Technology** in **Electronics and Communication Engineering** under the esteemed supervision of Smt.Y.Sujatha, Sr. Assistant Professor, Department of ECE.

This is a record of work carried out by us and results embodied in this project report have not been submitted to any other **University** or **Institution** for the award of any **Degree** or **Diploma**.

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ABSTRACT

Nowadays fast analog to digital converters (ADC) are required to catch up with the speed of digital world. An ADC is used to convert an analog signal such as voltage to a digital form so it can be read and processed by a microcontroller. Analog to digital converters are used to allow digital computers to interact with the everyday signals. In order to get high performance ADC, the internal components of ADC must have better properties. Normally a comparator be the major component of ADC.

In this project a three-stage comparator with high speed and low recoil noise is designed. When validate with conventional comparators the designed comparator gives better results. When compared with the existing model in this model a voltage charge pump is introduced instead a preamplifier. Charge pump acts as an amplifier. This technique greatly reduces the number of transistors as well as recoil noise and increases the speed of comparator. Since it has a smaller number of transistors it occupies less space, and the power consumption also reduces greatly. It overcomes the major disadvantages of the existing models.

For easy comparison the existing models and the proposed model are designed in CMOS technology using Tanner EDA Tool.

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CHAPTER 1

INTRODUCTION

Comparators, as the name suggests compares an analog signal with another analog signal and outputs a binary signal based on the comparison. The comparator can be thought of as a decision-making circuit. The comparator is widely used in the process of converting analog signals to digital signals. Since comparators are generally used in open loop mode, they can have very high open-loop gain. Comparators are generally classified as open-loop comparators and regenerative comparators. Open-loop comparators are basically operational amplifiers without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals.

The comparator can be thought of as a decision-making circuit. If the positive input of the comparator is at a greater potential than the negative input, the output of the comparator is at logic 1, whereas if the positive input is at a potential less than the negative input, the output of the comparator is at logic 0. The circuit symbol of the comparator is shown below in figure1.

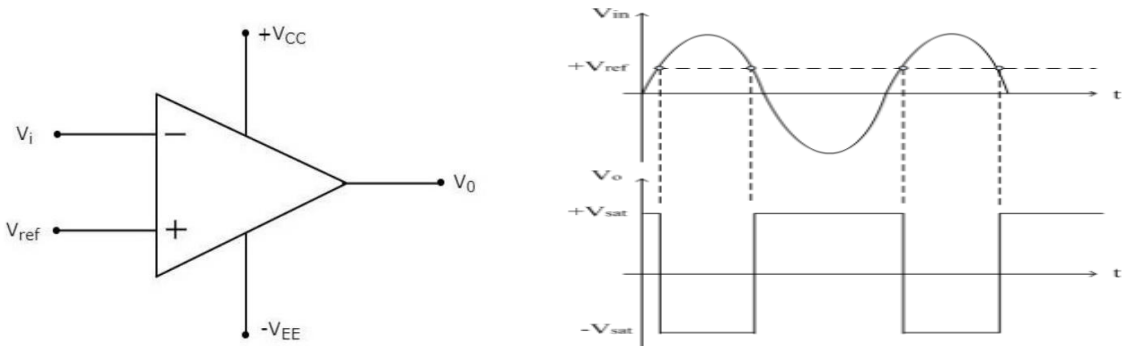

Figure 1.1. Basic comparator and its waveform

Comparators generally are designed to operate more optimally than op-amps in digital applications, in that comparator output voltages will go very close to the power supply voltage rails and their outputs will swing between these rails very fast, that is they have a very high slew rate.

1.1 Objective Of the Project

This project presents a high performance three stage comparator with high speed and low- recoil noise. By using a technique which can overcome the disadvantage of conventional models. The contribution of this project can be summarized as follows.

1. Three stage comparators are designed overcoming the disadvantages of two stage comparator.

2. A high speed three stage comparator is designed with less recoil noise.

3. A modified version of three stage comparator is designed with less area, delay and less power consumption.

A three-stage comparator is proposed with a technique that is used to increase the speed of latch stage. Simulation results can indicate that proposed model achieves low power, less area and high speed.

1.2 Organization of the Project

This project is organized into five chapters.

Chapter 1: It includes the introduction of the project.

Chapter 2: Consists of the background of comparators.

Chapter 3: Describes the High performance Three stage comparator with

low recoil noise, area and high speed.

Chapter 4: Gives the Simulation Results

Chapter 5: Advantages, disadvantages & Applications

Chapter 6: Discuss the Conclusion and Future Scope.

CHAPTER 2

LITERATURE SURVEY

Haoyu Zhuang , Wenzhen Cao, Xizhu Peng , and He Tang," A Three-Stage Comparator and Its Modified Version With Fast Speed and Low Kickback," IEEE transactions on very large scale integration (vlsi) systems, vol. 29, no. 7, July 2021

This brief presents a three-stage comparator and its modified version to improve the speed and reduce the kickback noise. Compared to the traditional two-stage comparators, the three-stage comparator in this work has an extra amplification stage, which enlarges the voltage gain and increases the speed. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. This greatly reduces the kickback noise by cancelling out the nMOS kickback through the pMOS kickback. It also adds an extra signal path in the regeneration stage, which helps increase the speed further.

H. Zhuang, H. Tang, and X. Liu, "Voltage comparator with 60% faster speed by using charge pump," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 2923–2927, Dec. 2020.

This brief proposes a novel comparator to greatly increase its comparison speed while not degrading its noise performance. This comparator is well suited for high-speed high-resolution SAR ADCs. Its structure is based on the classic Miyahara's two-stage comparator with the addition of only an extra charge pump. This simple modification greatly accelerates both the second-stage amplification phase and the regeneration phase, leading to significantly increased comparison speed. Meanwhile, the noise performance is not degraded, because the input pair transconductance of the second stage is increased while its integration time is decreased.

Jingqi Wang; Fan Ye; Junyan Ren "A Three-Stage Comparator with High Speed and Low Power", IEEE transactions on very large-scale integration (vlsi) systems, Vol. 28, Oct 2020

Three-stage comparator with two dynamic pre-amplifiers and a regenerative latch is proposed. The highlight of the proposed comparator is that a positive feedback pre-amplifier is added to the conventional two-stage comparator for higher gain and faster regenerative speed, which greatly suppresses the input-referred noise. In addition, the proposed comparator has almost no current flowing from the power supply to the ground, so it has extraordinary energy efficiency.

S vadivel and N S Nithya " Low power Two Stage Dynamic Comparator Circuit Design for Analog to Digital Converters", International Conference on Computer Communication and Informatics (ICCCI) 2018.

In this paper, a new structure is presented to realize a high-speed high-precision two-stage comparator. Positive feedback is employed in the first stage of the offered comparator to reduce the delay time. Furthermore, by using an NMOS transistor between the differential output nodes of each stage in the reset mode, the comparison speed is enhanced. Moreover, the second stage of the offered comparator is activated with a preset delay to improve the speed and accuracy of the comparison. Furthermore, by using intermediate transistors between the two stages of the comparator, the delay time and the comparison accuracy is also improved.

2.1 Comparator

A comparator detects whether its input is larger or smaller than the reference voltage. The output of the comparator is a digital signal ("1" or "0").

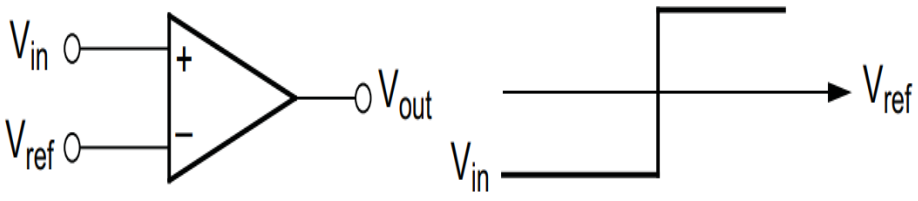

Figure 2.1: Comparator

If the input of comparator is driven with a voltage larger than the minimum voltage required to achieve the correct digital, the comparator is said to be overdriven.

Performance Characteristics:

1. Voltage Gain (A_v): Differential DC gain of a comparator, it is the derivative of the DC transfer curve.
2. Input Offset (V_{os}): Voltage that must be applied to the input to obtain a transition between the low and high state.
3. Response Time (t_r): Time interval between the instant when a step input is applied and the instant when the output reaches the corresponding logic level (depends on the input step amplitude).
4. Overdrive Recovery: Time interval required to recover from overdrive (the response time, for a given input step amplitude, depends on how much the comparator was previously overdriven
5. Recoil Noise: If design fail to provide perfect load at the output terminals some sort of disturbance will produce the latch circuit and feedbacks to comparator inputs. Therefore, the inputs will interfere with noise from output nodes and its actual inputs will vary because of these disturbances and this leads to give incorrect values as output.

2.2 Latched Comparators

In latched comparators, comparison is performed at given time instants (controlled by the latch signal) and the result is maintained until the next comparison is performed. Latched comparators are typically used in sampled data systems, for example data converters where the latch signal is the clock.

A latched comparator consists of a gain stage followed by a latch stage and eventually a set reset flip flop to hold the output signal while the latch is reset (latch bar signal).

The latch stage is based on a positive feedback loop ➜ Very fast response time.

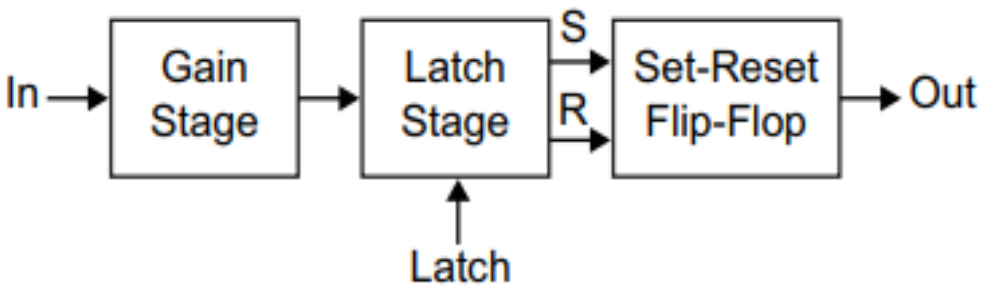

Figure 2.2: Block Diagram of Latched Comparator

During the latch phase the positive feedback is enabled, and the latch reaches a stable state. The state of latch depends on the logic level reached in the parasitic capacitances.

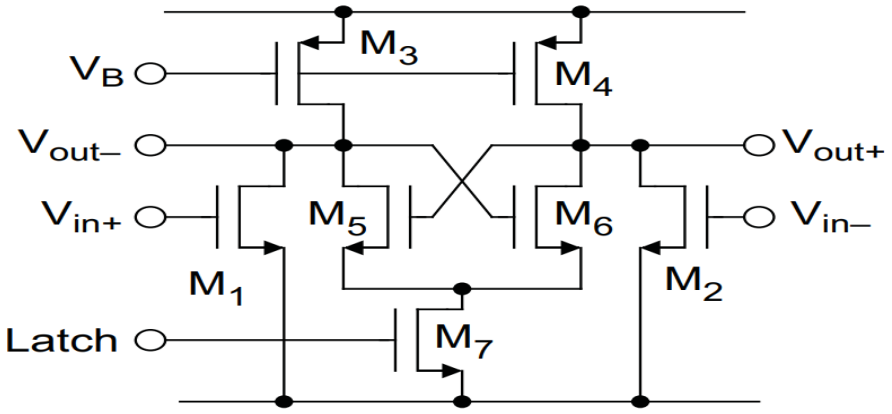

Fig 2.3: Simple Latched Comparator

During the reset phase (Latch) M1, M3 and M2, M4 form two inverters with active load. The parasitic capacitances at nodes Vout+ and Vout− are pre-charged to the desired logic signals.

During the latch phase (Latch) the positive feedback is enabled and the latch reaches a stable state The state of the latch depends on the logic level pre-charged in the parasitic capacitances Thanks to the regenerative behavior of the positive feedback loop the response time is very short even with small input signals The offset of the latch cannot be canceled with autozero or auxiliary stages To reduce the offset transistors M5 and M6 must have relatively large area (WL) ➜ Speed limitation Since the latch is reset before each comparison overdrive recovery is not an issue.

2.3 Two Stage comparator

There are many comparator structures reported in recent years. The Strong-Arm latch is a classic structure. It has several advantages: no static power, rail-to-rail outputs, and fast comparison due to the positive feedback. Nevertheless, it also has several limitations. First, its regeneration speed is limited by the small current source under the latch. Here, the current source is the input pair transistors. Because the input pair has a common-mode input of VDD/2, the current in the current source is limited, which limits the regeneration speed. Second, due to the several stacked transistors, a large power supply voltage is needed. Two-stage comparators do not have these issues. Take the Miyahara's two-stage comparator as an example . Its regeneration speed is no longer limited by the small current source. This is because its latch input pairs M6–M7 has a gate–source voltage of VDD, which is two times larger than the VDD/2 of the Strong-Arm latch. Another advantage is that the number of stacked transistors is reduced. This relaxes the requirement on the power supply voltage. Although the Miyahara's two-stage comparator increases the speed, its speed can be further improved in the following way. As can be seen in Fig. 2.4, its latch input pairs M6–7 is pMOS transistors, and the pMOS hole mobility is small (2–3 times smaller than the nMOS electron mobility), limiting the regeneration speed.

It's fascinating that the output (of ideal comparator) makes a spiky transition from Logic '0' to Logic '1', or the other way around, whenever the 2 input fast values cross one another. This means infinite gain analog differential electronic amplifier. However, usually a latch is employed because the deciding unit, which may accomplish a piercing, transition. The rise and fall time are set by the choice creating stage. The decision creating stage - a latch - changes its state once the trigger input exceeds the switch potential. This provides rise to input offset of the comparator.

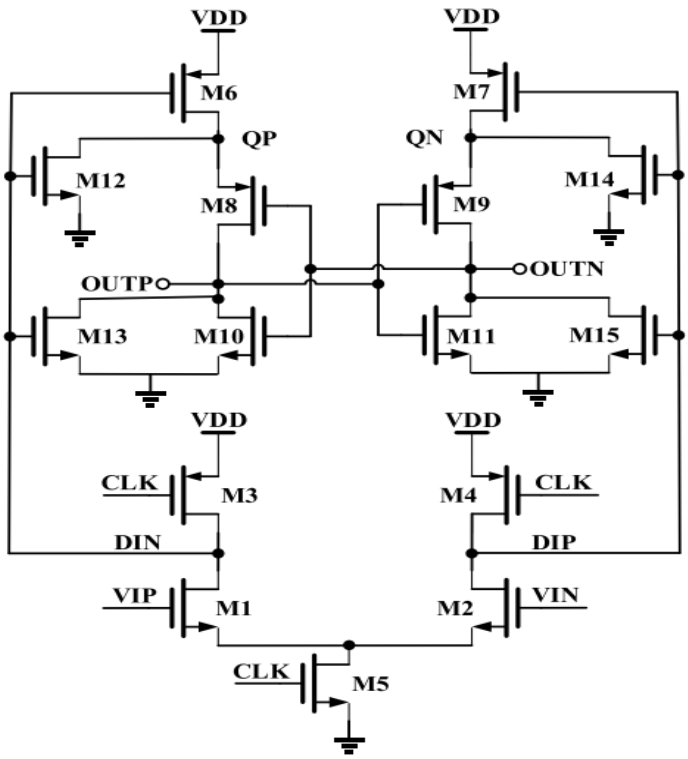

Figure 2.4: Two Stage Comparator

2.4 High performance comparator

A block diagram of a high-performance comparator is shown in figure 2.5 below. The comparator consists of three stages.

1. Input preamplifier stage
2. Positive feedback or decision stage
3. An output buffer stage

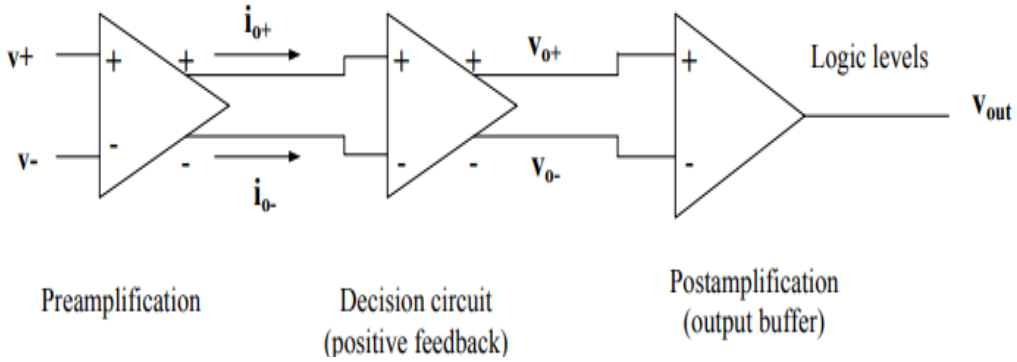

Figure 2.5: Block diagram of high-performance comparator

Preamplification stage: The preamp stage amplifies the input signal to improve the comparator sensitivity. i.e., increases the minimum input signal with which the

comparator can make a decision and isolates the input of the comparator from switching noise coming from the positive feedback stage. The schematic of the preamplification stage of the comparator. It consists of a differential amplifier with active loads.

Decision stage: The decision stage is the heart of this comparator and is used to determine which of the input signals is larger. The schematic of the decision stage of the comparator. This circuit uses positive feedback from the cross-gate connection to increase the gain of the decision element.

Output buffer stage: This stage is also called post-amplifier stage. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal.

2.5 Three Stage Comparator

Excessive-speed analog to-digital converters (ADCs) digitize the signal on the front-give up acquire channels in modem verbal exchange structures as the link among digital processors and the analogue global. As a result, the conversion speed and precision of ADCs are decided with the aid of the overall performance of comparators. A digital latch circuit with an infinite advantage, preamplifier makes up a super latched comparator. Comparators can combine high-quality feedback to acquire almost unlimited advantage due to the fact the amplifiers employed in them no longer need to be linear or closed loop. Due to less gain in the implementation of the preamplifier layout, the real latched comparators use a finite benefit amplifier circuit and an advantageous remarks dynamic latched circuit. A latched comparator's operation may be damaged into tiers because of its precise architecture, monitoring, and latching. The following dynamic latch circuit is grown to become off inside the monitoring level, and the preamplifier amplifies the input analogue differential voltages.

The instant currents of transistors are associated with the inputs of the comparators via parasitic gate-supply and gate-drain capacitances, rendering the disturbances undesirable. It is a phenomenon where the kickback noise has an impact on. The mixture of adjustments from regeneration nodes in flash ADCs wherein an excessive wide variety of comparators are becoming on or off at the identical time would possibly come to be enormously great, resulting in wrong quantization code output. However, to lower the offset voltage, these solutions require a high voltage gain, which loses effectiveness when the drain resistance decreases owing to technology scaling.

Furthermore, achieving a broad bandwidth amplifier necessitates a high-power consumption amplifier.

A dynamic comparator with an offset compensation function, on the other hand, was presented. On this method, every comparator's input sign is brought in flash type ADC because the reference voltage, and the weight capacitances of the comparator's output node are digitally regulated so that the comparator's output reaches the suitable fee. But, as the ADC's resolution is improved, the calibration time increases dramatically.

By adding an extra preamplifier stage, the nMOS input pairs can be used for both the latch-stage and the first-stage preamplifier, thus improving the regeneration speed. Besides, these input pairs work in the saturation region at the beginning of comparison, thus ensuring a small input referred noise. The extra stage of preamplifier also provides voltage gain, which helps further increase the regeneration speed and suppress the input referred offset and noise. The three stages are connected one after another. Compared with the Miyahara's comparator, the major difference is that one extra preamplifier (the second stage) is added.

This extra preamplifier acts as an inverter and makes the latch stage able to use nMOS input pair M11–12 instead of pMOS input pair, which leads to increased speed. The extra preamplifier also provides voltage gain, thus improving the regeneration speed and suppressing the input referred offset and noise. Although the extra preamplifier helps increase the speed, this extra stage itself incurs extra delay, because the amplified signal has to go through two stages, rather than one stage, before arriving at the latch stage. By adding three extra stages we can control the regeneration of the regenerative stage at lower current, thus the disadvantage of the two-stage comparator can be overcome.

Thus, it is necessary to discuss whether this extra delay overwhelms the benefit it brings about. As can be seen in Fig. 2, after the first-stage amplification, its outputs FP and FN fall to GND. This makes the second-stage input pair M8–9 have a large gate–source voltage equal to VDD. As a result, the current on M8–9 is large enough for quickly pulling up RP and RN. This means that the extra delay incurred by the second stage is small (about 20 ps in post-layout simulation) compared to the large delay of the latch stage (about 200 ps in post-layout simulation).

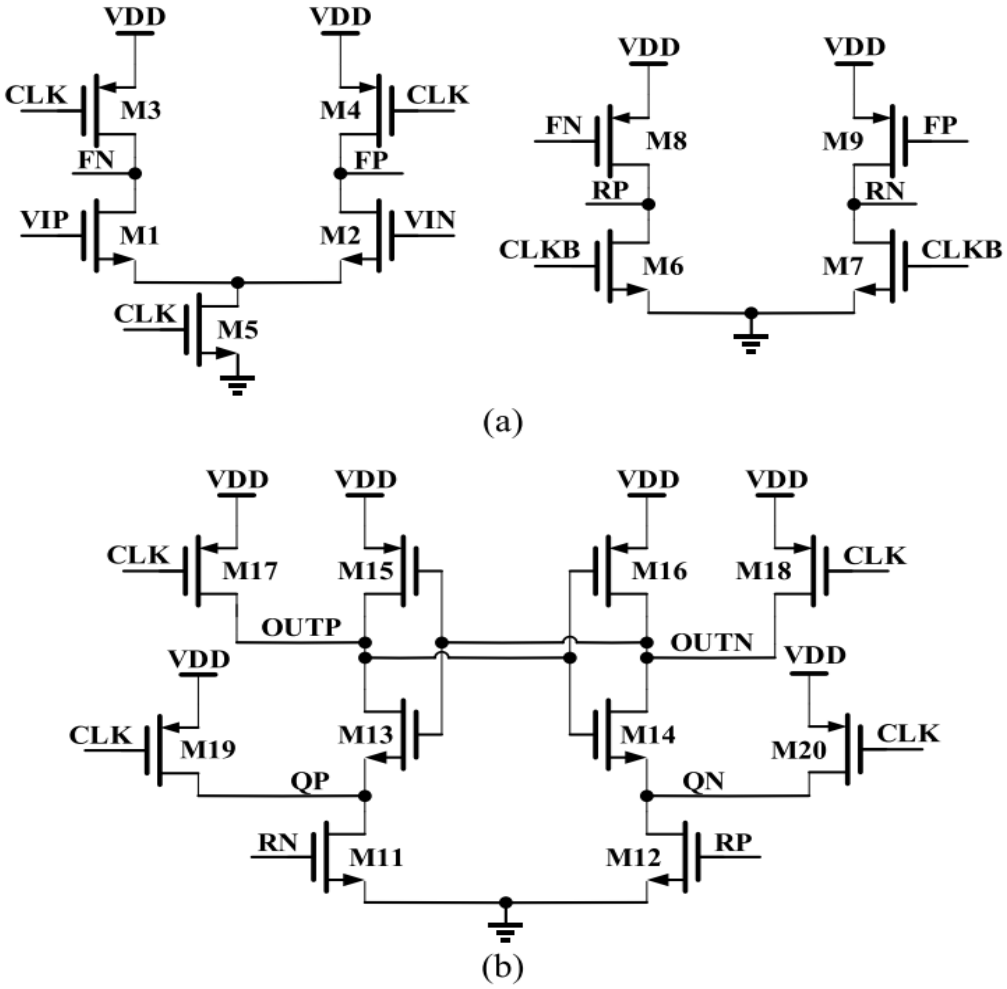

Figure 2.6: Three-stage comparator: (a) preamplifiers (stage 1 & 2) (b) Latch stage (stage 3)

This makes sense because the second stage is a dynamic inverter which does not incur much delay. Furthermore, compared to the first-stage output load in the Miyahara's comparator (M6–7 and M12–15 in Fig. 1), the first-stage output load in the three-stage comparator is only M8–9 in Fig. 2. The output load is reduced by several times, improving the amplification speeds of the transient simulation comparison between the Miyahara's comparator and the three-stage comparator. As can be seen, the first-stage output of the three-stage comparator settles faster than the Miyahara's first-stage output by 60 ps, due to the decreased output load. Even if the extra delay of the second stage is considered, the second-stage output of the three-stage comparator still settles faster than the Miyahara's first-stage output by 40 ps, considering 90% settling. Furthermore, the regeneration time of the latch stage is also reduced by 76 ps due to the nMOS input pair.

The three-stage comparator has so many advantages. First, the gate of M6–7 in Fig. 2 is connected to CLKB, rather than to the first-stage output. This reduces the parasitic capacitance at the first-stage output. Second, the gate of M17–20 is connected to CLK, rather than to the second-stage output. This reduces the parasitic capacitance at the second-stage output. Third, the clocked cascode nMOS on top of M1–2 is deleted. This reduces the parasitic capacitance in the first stage. More importantly, it helps ensure that the drain of M1–2 is at VDD at the beginning of comparison. This is important because the saturation region of input pair helps reduce the input referred noise. Overall, post-layout simulated results show that the input referred noise is reduced by 15% due to the guaranteed saturation region of input pair, and the speed is increased by 6% due to the less parasitic capacitances.

2.6 Three stage Comparator using Lector Technique

The comparator is a critical constructing block for all excessive pace ADC's, unbiased architecture, and it influences the general overall performance of records converters to a wonderful extent. It carries records which include the most sampling rate, a chunk resolution, and standard strength intake. Comparators are perhaps the maximum underappreciated and underused monolithic linear component. This is regrettable due to the fact comparators are some of the maximum adaptable and extensively used additives available. The IC op amp, whose adaptability lets it dominate the analogue layout arena, is in charge for a huge a part of the shortage of awareness. Comparators are normally notion of as 1-bit A/D converters that poorly specific analogue records in virtual shape. In a strict sense, this factor of view is correct. It additionally has a wastefully restrictive viewpoint. Comparators do not "without a doubt compare, "simply as op amps do not "simply amplify." Comparators, especially excessive pace comparators, may be applied to assemble linear circuit capabilities as state-of the-art as any op amp-primarily totally based circuit. Getting excessive overall performance effects calls for appropriate use of a quick comparator and op amps. Op-amp primarily totally based circuits, in general, employ their cap potential to exactly near a remarks loop. In a super world, such loops might be maintained indefinitely. Comparator circuits, on the opposite hand, often depend on pace and function a time-various output.

While every approach has advantages, combining the 2 produces the best circuits. Figure four depicts the 3-level comparator. The predominant alternate from the Miyazawa comparator is the addition of a 2nd preamplifier (the second one level).

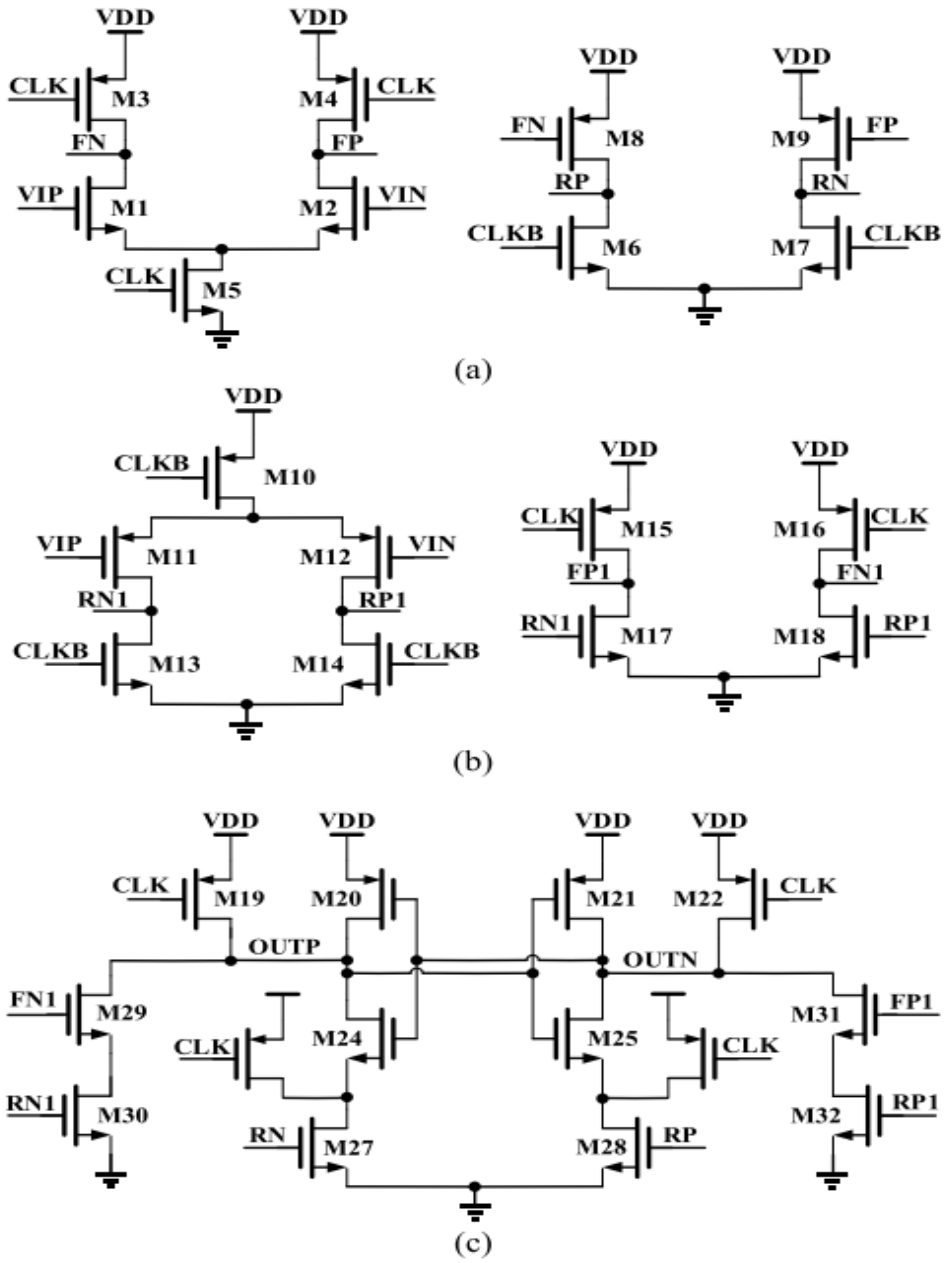

Figure 2.7: Three-stage comparator with lector technique. (a) First two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

In order to reduce the kickback noise and further improve the speed, this brief proposes a modified version of a three-stage comparator, as shown in Fig. 4. Compared to the

original version in the previous section, the only difference is that the modified version has the extra first two stages. The extra first two stages use pMOS input pair M11–12 to cancel out the nMOS input pair M1–2 kickback noise. Besides, the extra paths M29–32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further, and the input referred offset and noise are suppressed further. The operation of these extra circuits is as follows. In the reset phase, CLK is 0 and CLKB is 1. The RP1 and RN1 in Fig. 4(b) are reset to GND, while FP1 and FN1 are reset to VDD. This turns off M30 and M32 in Fig. 4(c),ensuring that there is no static current in the extra path M29–32.

In the amplification phase, CLK rises to 1 and CLKB falls to 0. RP1 and RN1 in Fig. 4(b) rise to VDD (R stands for rise). Then, FP1 and FN1 fall to GND (F stands for fall). Because the rising of RP1 and RN1 occurs before the falling of FP1 and FN1, the extra paths in Fig. 4(c) are turned on for a limited time, drawing a differential current from the latching nodes OUTP and OUTN.

This generates a differential voltage at OUTP and OUTN, which helps speed up the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths in Fig. 4(c) are turned off again to prevent the static current. Overall, the modified version of the three-stage comparator has the advantages of faster speed, lower input referred offset and noise, lower kickback noise. It is suitable for high-speed high-resolution SAR ADCs.

An extra preamplifier is a major difference between three stage comparator and three stage comparators with Lector technique. Usually, Lector technique means adding a preamplifier to the conventional three stage model. That is why this comparator has two stages of preamplifiers. This makes the usage of pMOS topology to give inputs. Adding a preamplifier leads to adding of transistors in latch stage in order to increase path. Due to this extra path the power consumption will increase.

CHAPTER 3

Three Stage Comparator with Voltage Charge Pump

3.1 Three Stage Comparator with Voltage Charge Pump

To overcome the disadvantage of three stage comparator such as area, power consumption and delay instead of using Lector technique a charge pump is used here. Both the techniques are used for the same purpose, but the architecture is different. Compared to Lector technique the charge pump occupies less area and there is no need for an extra path thus it reduces the power consumption.

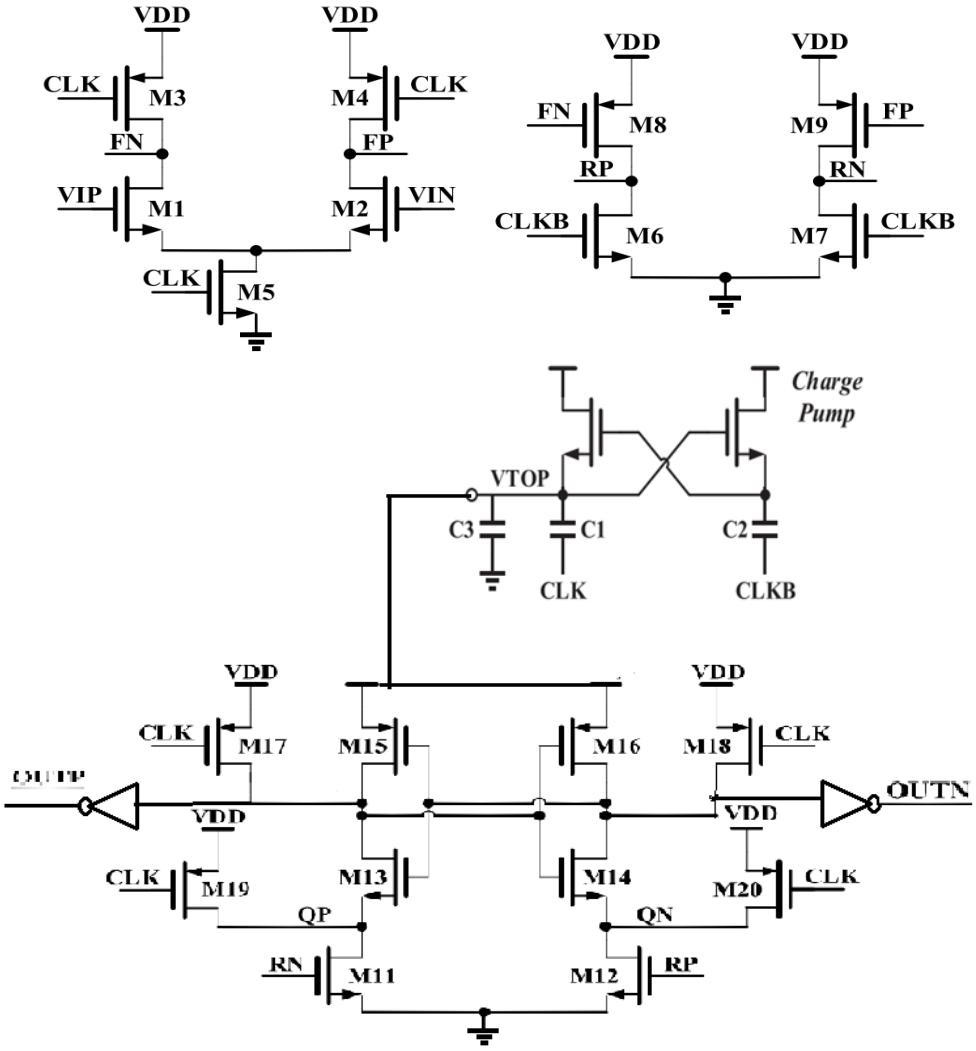

Figure 3.1: Three stage comparator with voltage charge pump. First two stages (preamplifiers) and Third stage with charge pump

3.1.1 FUNCTIONAL DESCRIPTION

A three-stage comparator is an electronic circuit that compares two analog signals and produces an output based on the comparison. The circuit uses three stages of operational amplifiers (op-amps) to amplify and compare the signals.
The working procedure of a three-stage comparator can be broken down into the following steps:

- **Signal Amplification:** The input signals are first amplified by the first stage preamplifier. The gain of this stage is usually set by the feedback loop. The amplified signals are then fed to the second stage.
- **Level Shifting:** The second stage is configured as a level shifter. It shifts the amplified signals to a reference voltage level. The shifted signals are then fed to the third stage.
- **Decision making:** The third stage is configured as a decision-making stage. It compares the shifted signals and produces an output based on the comparison.
- **Latch Stage:** The output of the comparator is typically a binary signal, either high or low, indicating which signal is higher or lower than the other.

The high-performance comparator obtained by pumping the voltage higher the VDD to the latch stage. This can be resolved by using a voltage charge pump which is used for obtaining higher voltage for given voltage. In order to speed up the comparison of inputs the latch must work with high speed. So, connecting output of voltage charge pump to the sources of pMOS transistors in latch stage results in high regeneration speed of inputs, high speed signal comparison and fast pumping of outputs nodes.

Thus, it is necessary to discuss whether this extra delay overwhelms the benefit it brings about. As can be seen in Fig. 3.1, after the first-stage amplification, its outputs FP and FN fall to GND. This makes the second-stage input pair M8–9 have a large gate–source voltage equal to VDD. As a result, the current on M8–9 is large enough for quickly pulling up RP and RN. This means that the extra delay incurred by the second stage is small (about 20 ps in post-layout simulation) compared to the large delay of the latch stage (about 200 ps in post-layout simulation). This makes sense because the second stage is a dynamic inverter which does not incur much delay. Furthermore, compared to the first-stage output load in the Miyahara's comparator (M6–7 and M12–15 in Fig.

1), the first-stage output load in the three-stage comparator is only M8–9 in Fig. 3.1.

The output load is reduced by several times, improving the amplification speeds of the transient simulation comparison between the Miyahara's comparator and the three-stage comparator. As can be seen, the first-stage output of the three-stage comparator settles faster than the Miyahara's first-stage output by 60 ps, due to the decreased output load. Even if the extra delay of the second stage is considered, the second-stage output of the three-stage comparator still settles faster than the Miyahara's first-stage output by 40 ps, considering 90% settling.

Furthermore, the regeneration time of the latch stage is also reduced by 76 ps due to the nMOS input pair. The three-stage comparator has so many advantages. First, the gate of M6–7 in Fig. 3.1 is connected to CLKB, rather than to the first-stage output. This reduces the parasitic capacitance at the first-stage output. Second, the gate of M17–20 is connected to CLK, rather than to the second-stage output. This reduces the parasitic capacitance at the second-stage output.

Third, the clocked cascode nMOS on top of M1–M2 is deleted. This reduces the parasitic capacitance in the first stage. More importantly, it helps ensure that the drain of M1–2 is at VDD at the beginning of comparison. This is important because the saturation region of input pair helps reduce the input referred noise. Overall, post-layout simulated results show that the input referred noise is reduced by 15% due to the guaranteed saturation region of input pair, and the speed is increased by 6% due to the less parasitic capacitances.

3.3 Voltage Charge Pump

The architecture of the charge pump is based on continues current pumping technique. In general, a charge pump is required to provide load current all the time. The input power supply should deliver enough charge during each clock cycle to fulfill the load current requirement.

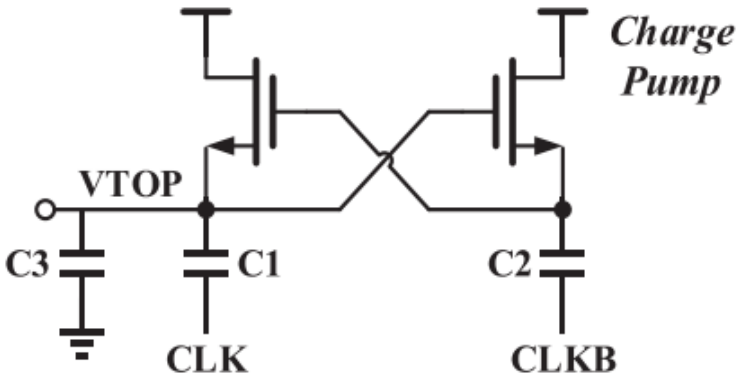

Figure 3.3: Voltage Charge Pump

A typical charge pump has two clocking phases:

1) **Charge phase** – during which the charge is transferred to the load capacitor.

2**) Discharge phase** during which the charge pump stops pumping charge.

The load current is provided by discharging the load capacitor during the discharge phase. In the proposed architecture the energy required to be delivered to the load is continuously provided by either the top half or the bottom half of the charge pump to the load capacitor. During a full cycle of the clock signal, there is no phase for the load capacitor. However, the load capacitor discharges a small amount of charge to current requirement during each half cycle which results in the output ripple voltage.

Here the charge pump is designed with cross coupled nMOS transistors and with three capacitors C1, C2 and C3. The charge pump is used to amplify the given input voltage. The sources of first nMOS transistors is connected to C1 and the source of second nMOS transistor is connected to C2.

- When CLK=1 and CLKB=0,

In this condition the capacitor C1 is charged to VDD and the capacitor C2 remains same. This can switch on the second nMOS transistor and short the first nMOS transistor. This can rise the given VDD to the voltage greater than VDD and stored in capacitor C3. The output of the voltage charge pump is VTOP.

- When CLK=0 and CLKB=1,

In this condition the capacitor C2 is charged to VDD and the capacitor C1 remains

same. This can switch on the first nMOS transistor and short the second nMOS transistor. This can rise the given VDD to the voltage greater than VDD and stored in capacitor C3. The output of the voltage charge pump is VTOP.

In both conditions the VTOP becomes greater than VDD simultaneously. In a charge pump, the output voltage has a linear dependence with respect to the load current, exhibiting an equivalent output resistance. In most applications, the output voltage should be kept constant under different load current. To achieve this, the regulated charge pump is used.

While the three stage comparator is interfacing with voltage charge pump, it decreases the usage of power consumption due to the amplifying nature of the charge pump. The voltage charge gives output nearly equivalent to 1.49 times of VDD i.e., 1.49VDD but while using this it is up to 2.84 volts for the given voltage of 2.5 volts. It means the settling voltage is 1.2 VDD but with a peak of 1.49 VDD. So, by using charge pump the output of this circuit never fall beyond given voltage.

CHAPTER 4

SIMULATION RESULTS

In this project, Two Stage Comparator, Three Stage Comparator, Three Stage Comparator with Lector technique are used for comparison. We have studied the proposed designs and compared them with the CMOS based accurate and performed simulations using 125nm technology in Tanner Tool. The Modified Three Stage comparator has a lower power consumption and low recoil noise compared to the conventional model. Compared to the Three Stage Comparator with Lector technique the proposed model occupies less area and give more accurate outputs.

4.1 Three Stage Comparator with Voltage Charge pump

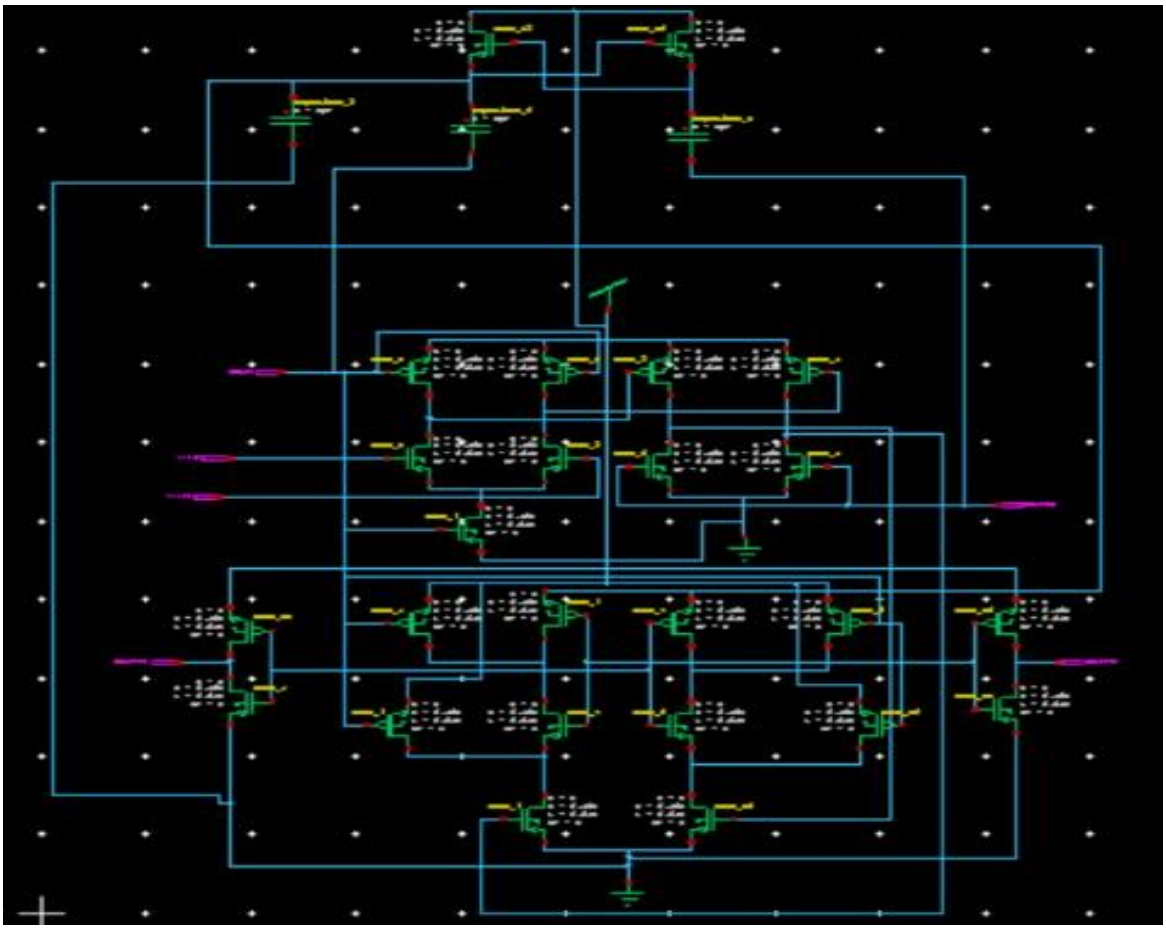

Figure 4.1: Schematic of Three Stage Comparator with Voltage Charge Pump

Table4.1

Truth Table for Three Stage Comparator with Voltage Charge Pump

CLK	INPUTS		OUTPUTS	
	VIP	VIN	OUTP	OUTN
0	X	X	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

4.1.1 Waveforms

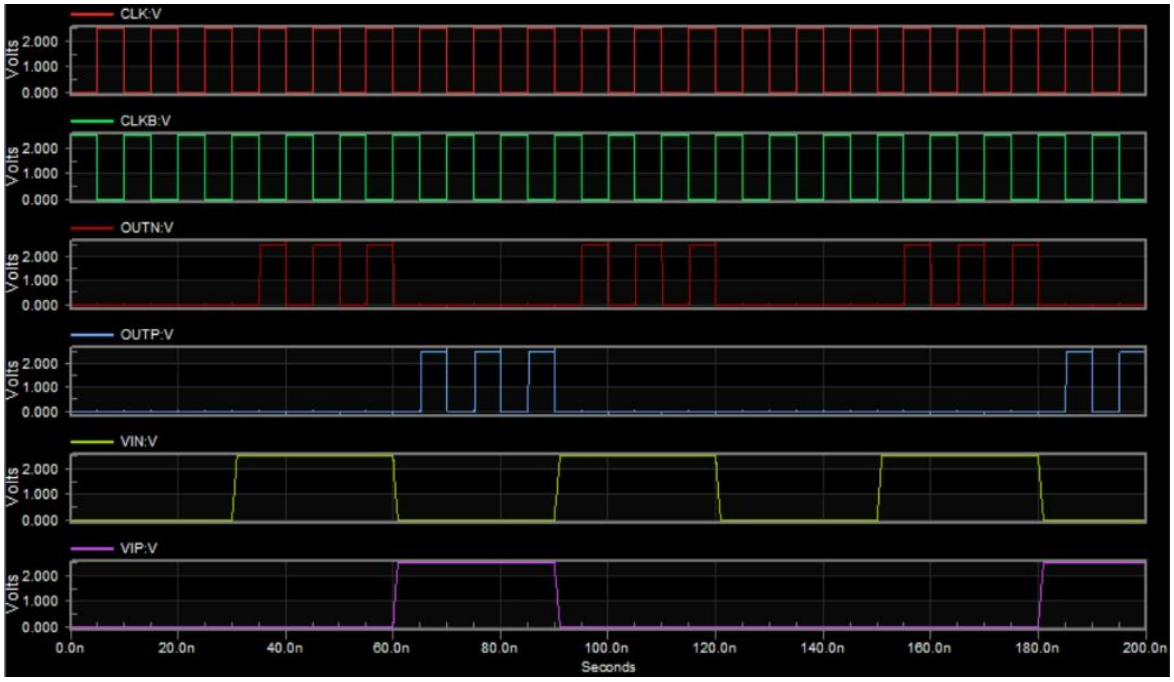

Figure 4.2: Waveforms of Three Stage Comparator with Voltage Charge Pump.

Here mainly the comparison of inputs takes place and the output will pass on the node which input is high from the waveform, the output will pass whenever the CLK is high.

For VIP=1, VIN=0 the output will pass on the node OUTP i.e., OUTP=CLK

For VIP=0, VIN=1 the output will pass on the node OUTN i.e., OUTN=CLK

If both inputs VIP=VIN=0 the. both OUTP=OUTN=0

4.1.2 Power result

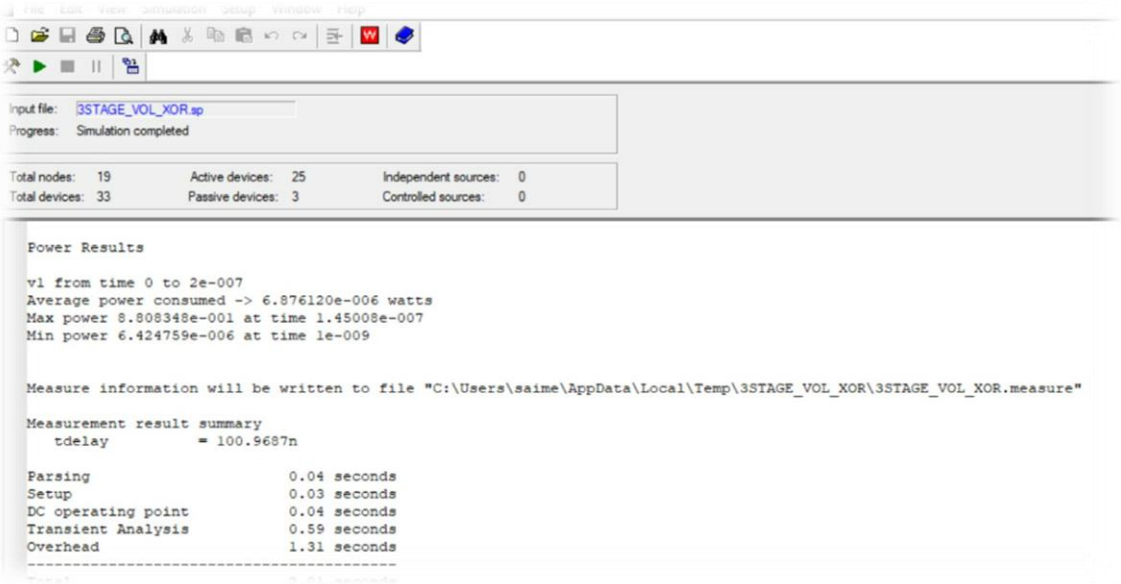

Figure 4.3: Power result of Three Stage Comparator with Voltage Charge Pump.

4.2 Voltage Charge Pump

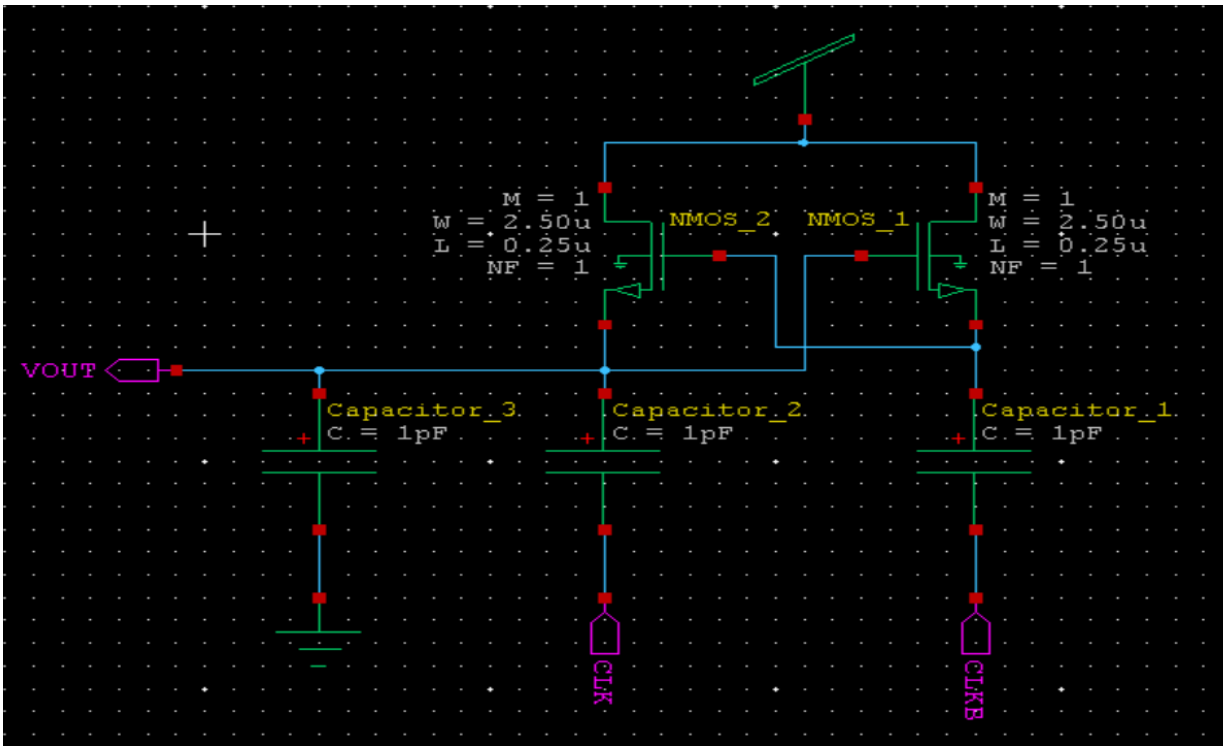

Figure 4.4: Schematic of Voltage Charge Pump

4.2.1 Waveforms

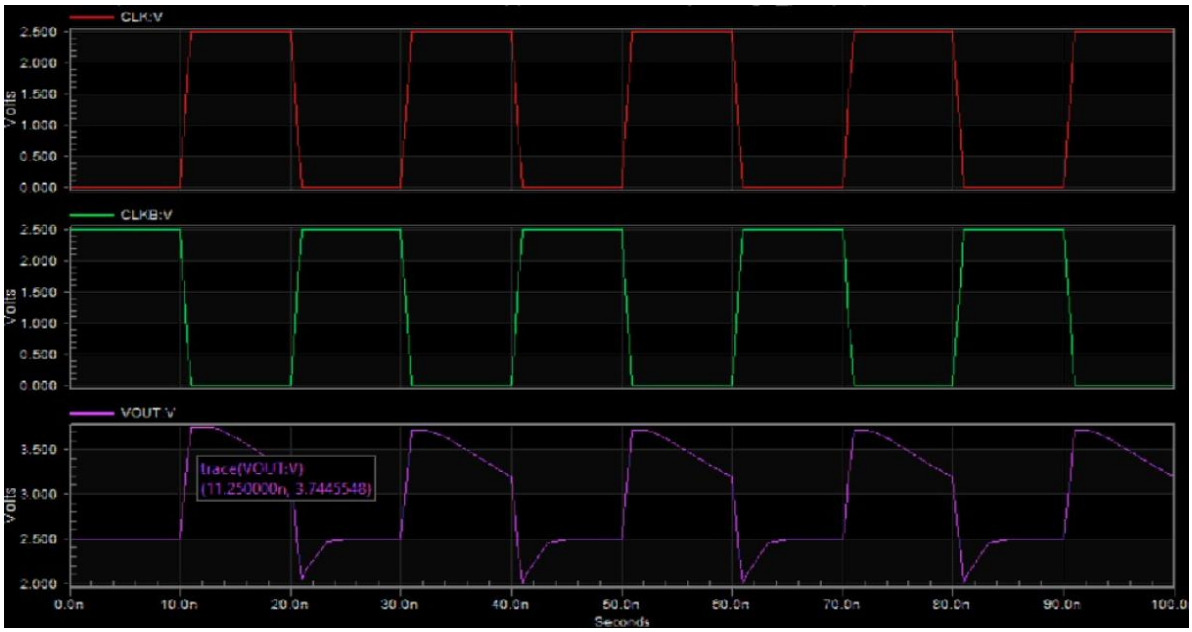

Figure 4.5: Waveforms of Voltage Charge Pump.

The voltage charge pump is used for getting higher voltage for given voltage.

From the waveform, here the VDD is about 2.5V .Hence the output node VOUT be representing the peak voltage of 3.74V i.e., it nearly equivalent to 1.49VDD

4.3 Three stage comparator with Lector technique

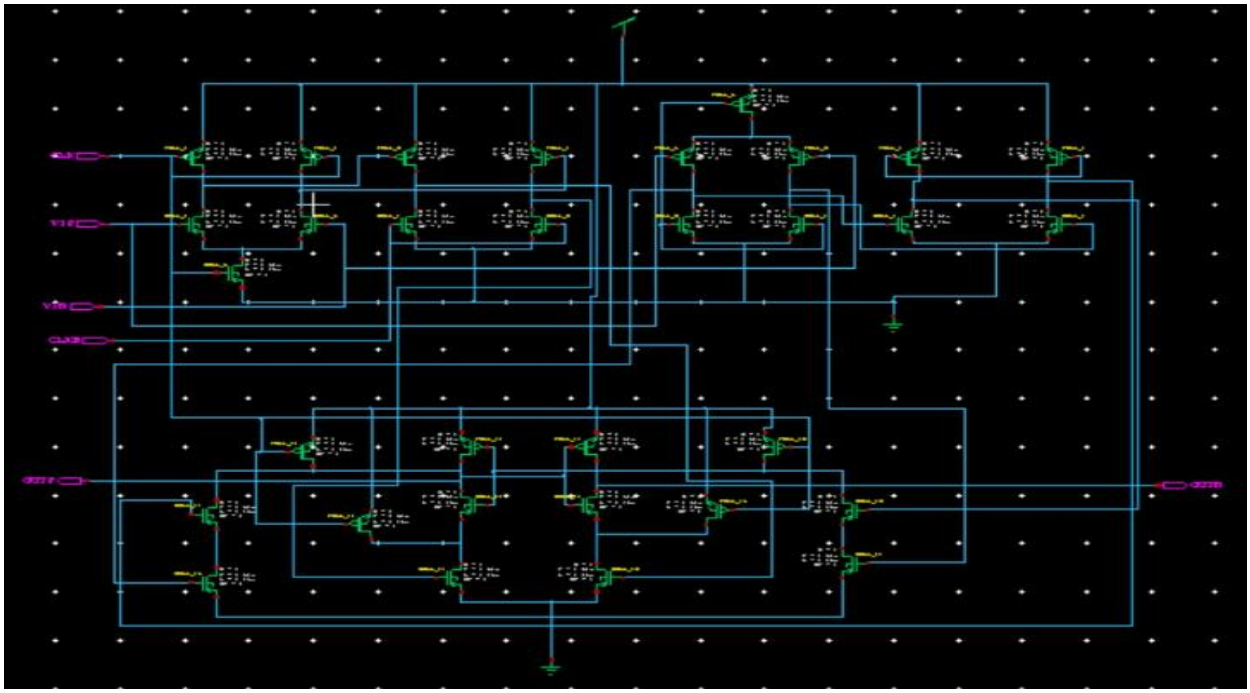

Figure 4.6: Schematic of Three Stage comparator using Lector technique

Table4.2

Truth Table for Three Stage Comparator with Lector technique

CLK	INPUTS		OUTPUTS	
	VIP	VIN	OUTP	OUTN
0	X	X	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

4.3.1 Waveforms

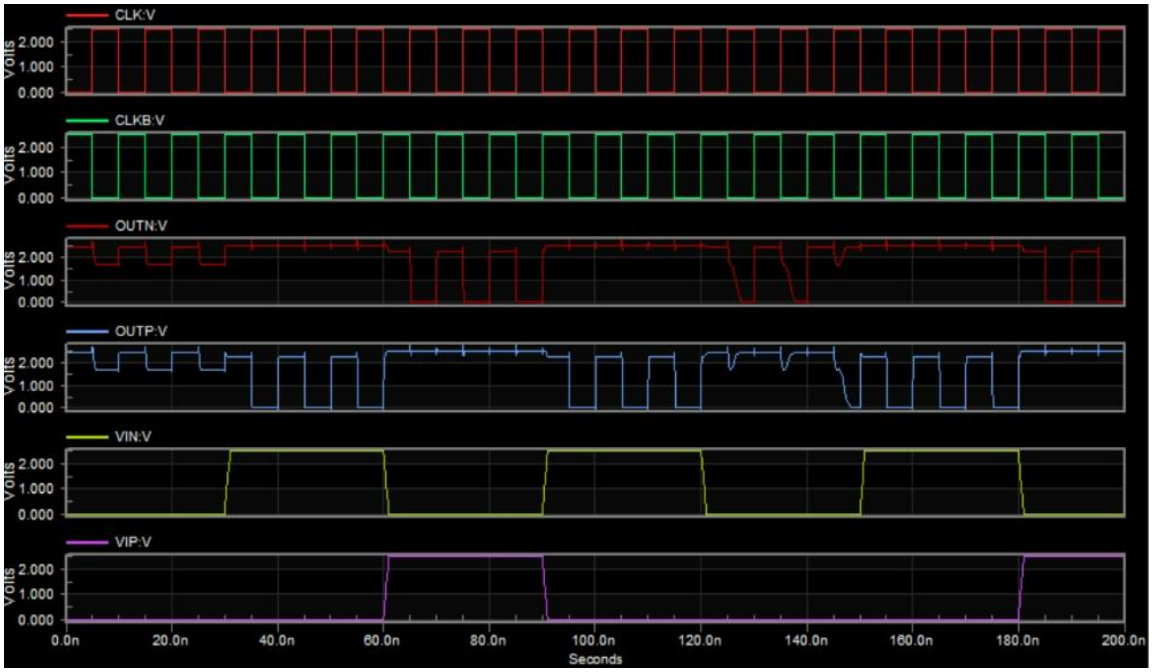

Figure 4.7: Waveforms of Three stage comparator using Lector technique.

For this comparator, the recoil noise is existed, and it is the main disadvantage of it. From the waveform, due to imperfection in the load at output stage the feedback is

existed and it can variates the given inputs.so the outputs are not clear for the given inputs due to feedback loop.

4.3.2 Power result

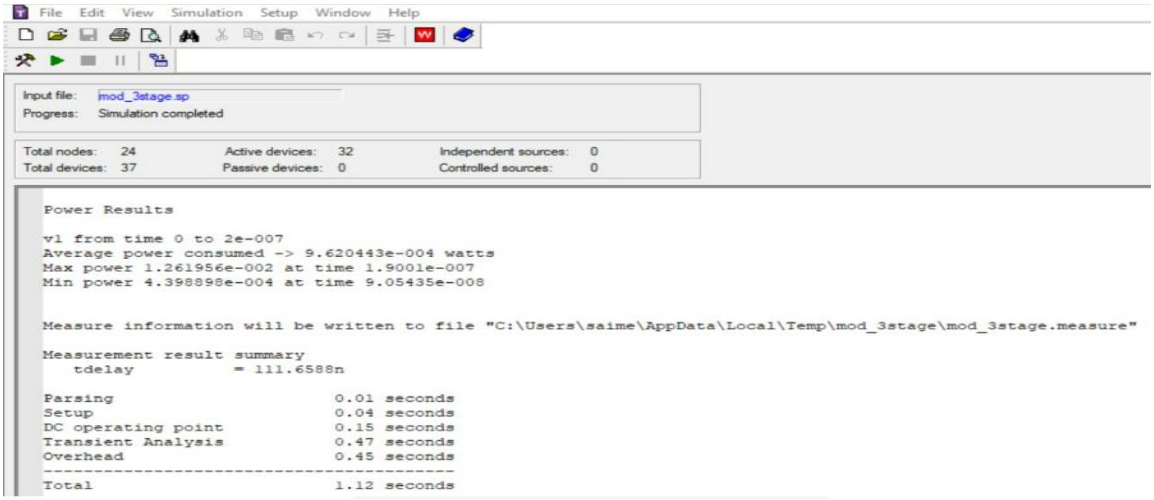

Figure 4.8: Power result of Three Stage Comparator using Lector technique.

4.4 Three Stage Comparator

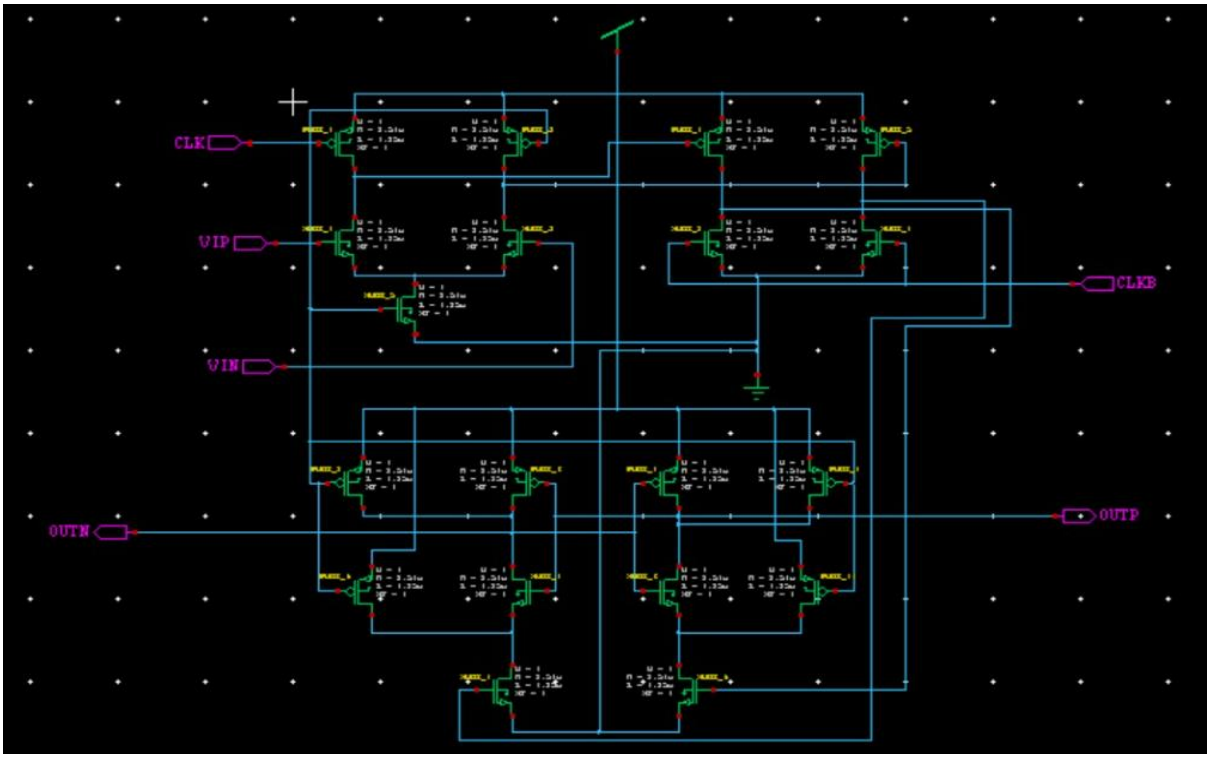

Figure 4.9: Schematic of Three Stage Comparator

Table4.3

Truth Table for Three Stage Comparator

CLK	INPUTS		OUTPUTS	
	VIP	VIN	OUTP	OUTN
0	X	X	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

4.4.1 Waveforms

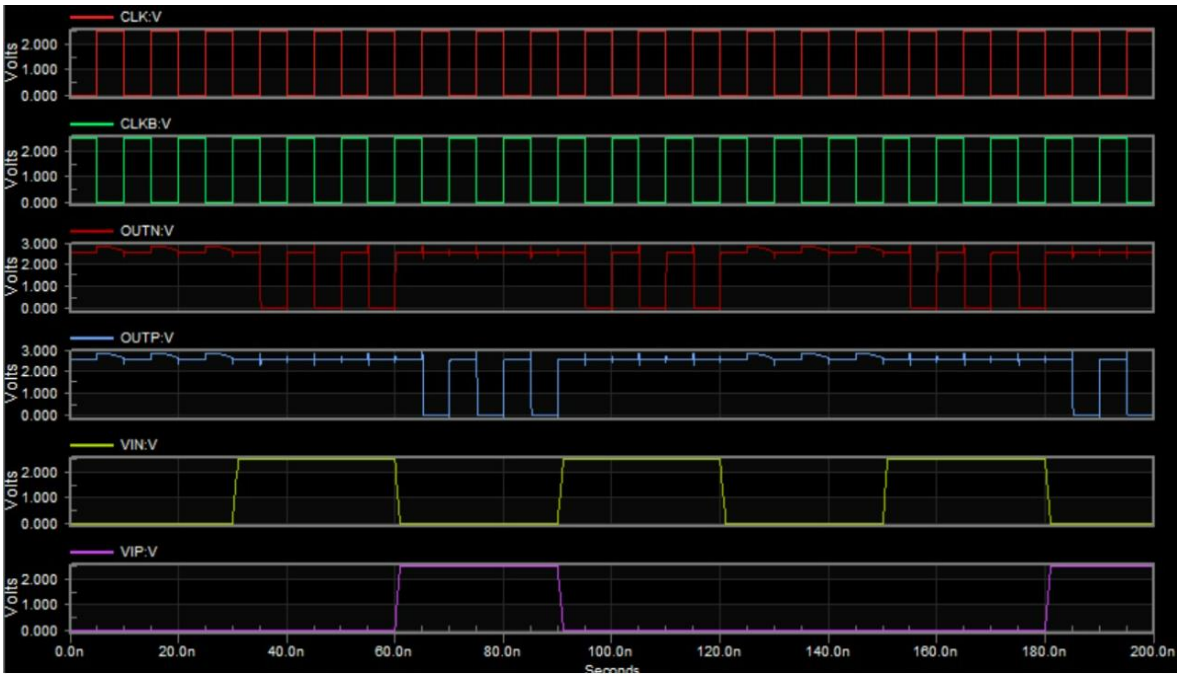

Figure 4.10: Waveforms of Three Stage Comparator

Here mainly the comparison takes place between the inputs and the output will pass on the output node which input is high.

Due to feedback of the latch stage, the recoil noise exists, and it can reduce the input

values, so the outputs are not given correctly.

4.4.2 Power result

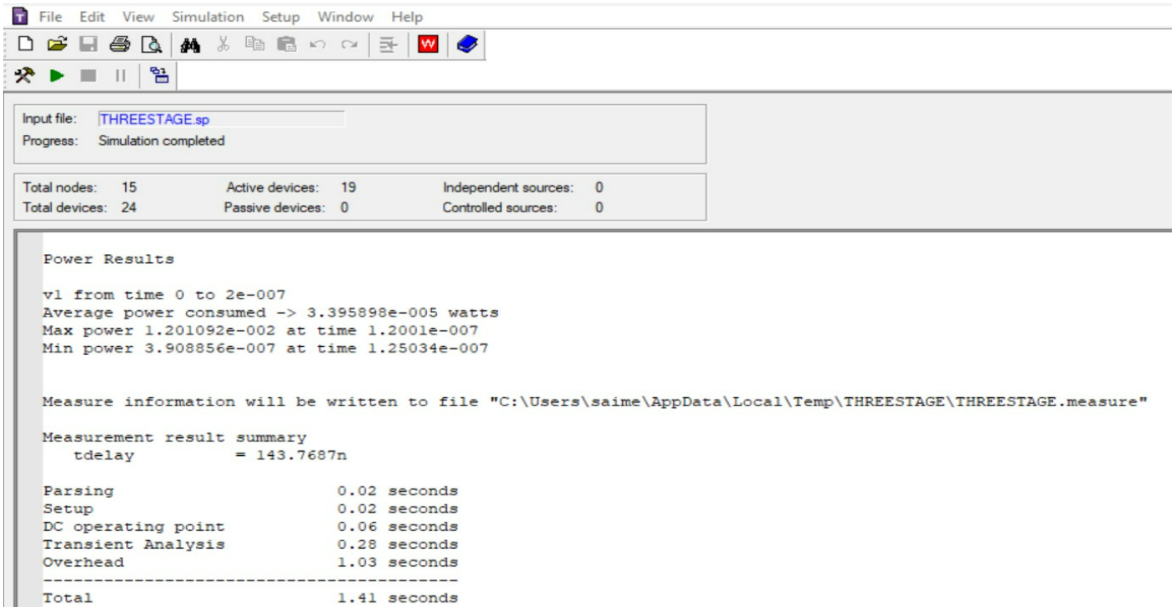

Figure 4.11: Power result of Three Stage Comparator

4.5 Two Stage Comparator

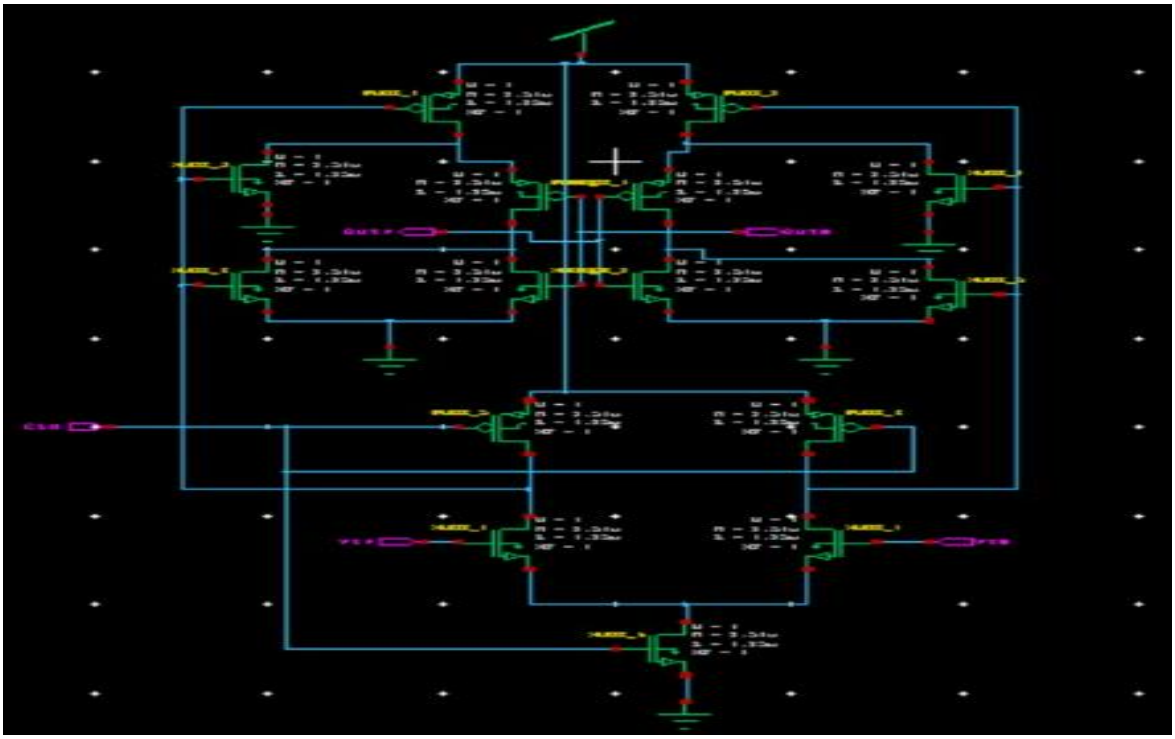

Figure 4.12: Schematic of Two Stage Comparator

Table4.4

Truth Table of Two Stage Comparator

CLK	INPUTS		OUTPUTS	
	VIP	VIN	OUTP	OUTN
0	X	X	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

4.5.1 Waveforms

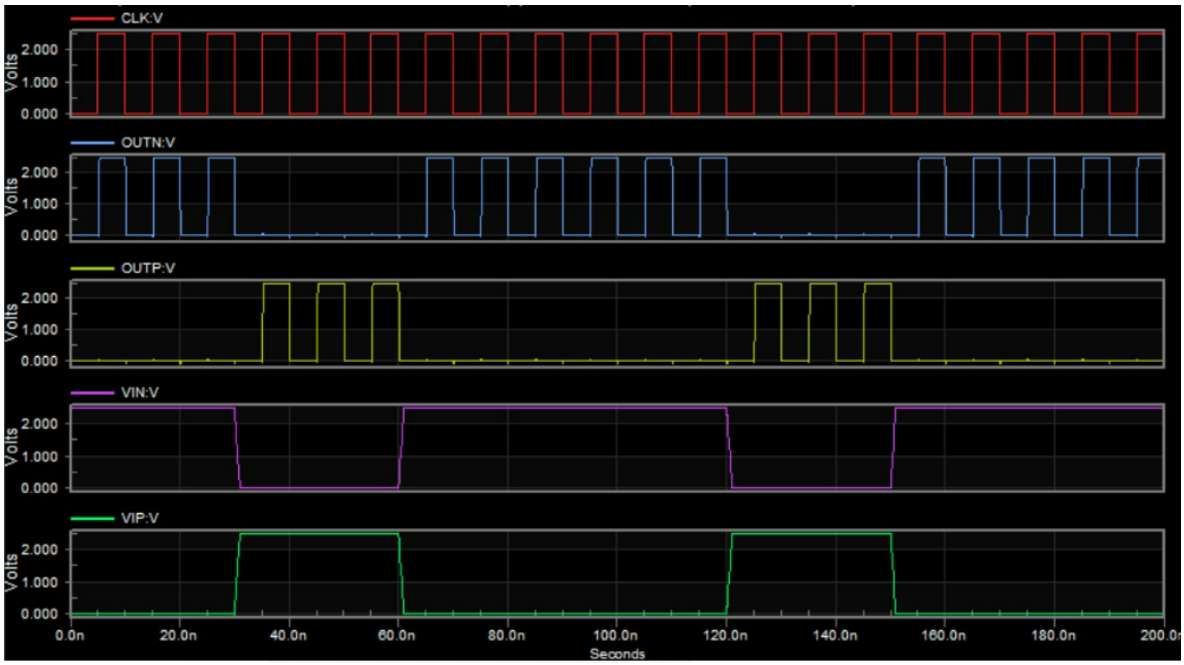

Figure 4.13: Waveforms of Two Stage Comparator

Here mainly the comparison takes place between the inputs and the output will pass on the output node which input is high.

Due to feedback of the latch stage, the recoil noise is existed and it can reduce the input values, so the outputs are not given correctly.

4.5.2 Power result

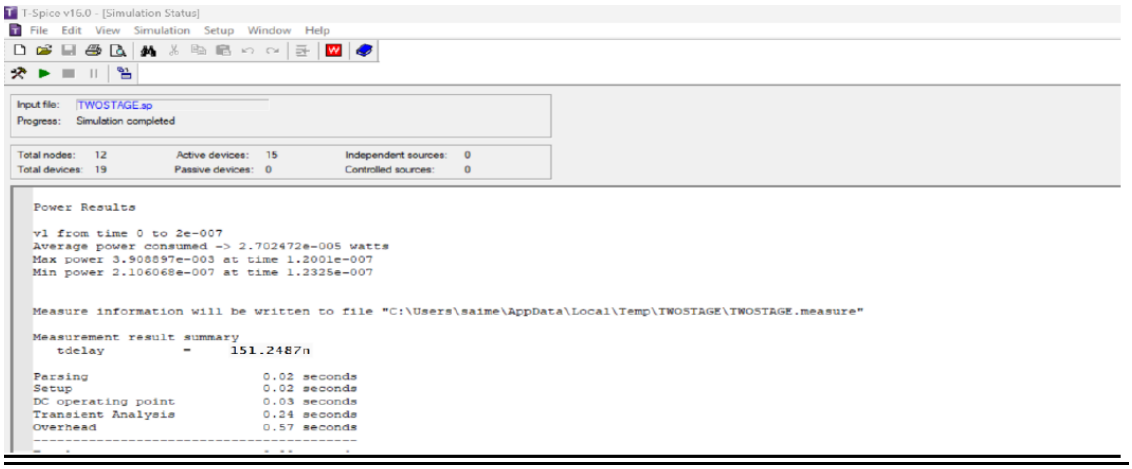

Figure 4.14: Power result of Two stage comparator

4.6 Performance Analysis

For comparison purposes, the two-stage comparator, Three Stage Comparator, Three Stage Comparator using Lector technique and the proposed model of Three Stage comparator are designed and implemented in 125nm technology. The proposed designs are evaluated in terms of power, delay, and Transistor count. Here, the speed comparison of given inputs is taken in terms of delay as delay is inversely proportional to speed. The area of the design can be observed based on the transistor count.

4.6.1 Transistor Count

The transistor count of the two-stage comparator, Three Stage Comparator, Three Stage Comparator using Lector technique and the proposed model of Three Stage comparator transistors are shown in the below Table 4.5.

The modified version of the Three Stage Comparator i.e. With Voltage Charge Pump is designed with 22% a smaller number of transistors than the three-stage comparator with lector technique.

Table 4.5: Transistor Count

	PMOS	NMOS	Total
Two Stage Comparator	6	9	15
Three Stage Comparator	10	9	19
Three Stage comparator with lector technique	15	17	32
Three Stage comparator with voltage charge pump	12	13	25

4.6.2 Power Consumption

Power consumption is the amount of energy used per unit time. It has great importance in digital systems. It is measured along the path it covers from input node to output node.

Three Stage Comparator with voltage charge pump consumes less power than conventional three stage comparator due to absence of extra path indulged by the pMOS input pairs.

Table 4.6 Power Consumption

Type of Circuit	**Average Power Consumed (uW)**
Two Stage Comparator	83.3
Three Stage Comparator	33.9
Three Stage Comparator with Lector Technique	96.2
Three Stage Comparator with voltage charge pump	6.87

4.6.3 Time delay

It is measured as the time required for the circuit to give the output. As time delay is inversely proportional to speed, the proposed model takes less delay hence it is faster than the three-stage comparator with Lector technique.

Table 4.7 Time delay

Type of Circuit	Time delay (ns)
Two Stage Comparator	164.78
Three Stage Comparator	143.76
Three Stage Comparator with Lector Technique	111.65
Three Stage Comparator with voltage charge pump	100.96

The Graphical representation of the power consumption and time delays for the three models are represented in the below graph Figure 4.14, for better understanding.

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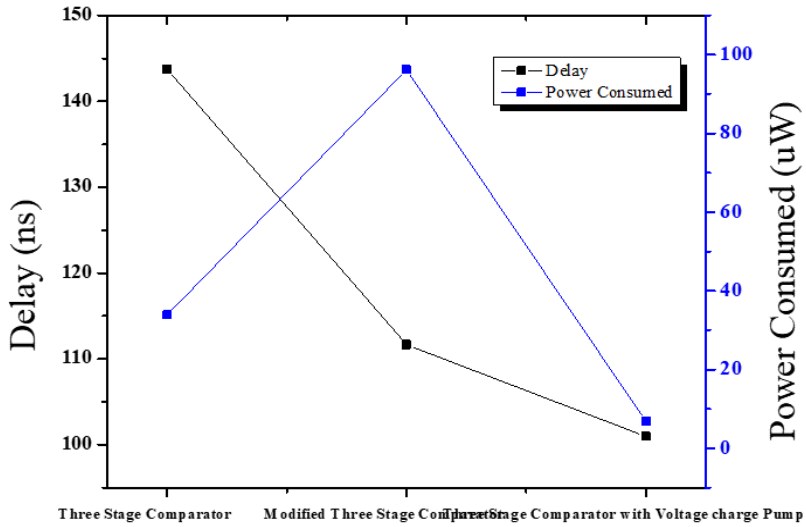

Figure 4.15: Graphical representation of power consumption and delay

CHAPTER 5

ADVANTAGES, DISADVANTAGES &APPLICATIONS

5.1 ADVANTAGES

- High precision: Three stage comparator have a correction stage which can improve the precision of the output signal making them suitable for high resolution applications.
- High linearity: Three stage competitors have a correctional stage which can improve the linearity of the output signal making them suitable for applications where the input signal needs to be converted to a different format.
- Low Recoil Noise
- High speed: The proposed model has high speed due to absence of the extra path that is present in the conventional three stage model.
- Low power consumption
- Less area

5.2 DISADVANTAGES

- Fabrication is expensive.
- If one component in an integrated circuit fails, it means the whole circuit has to be replaced.
- It can be handled only a limited amount of power.

5.3 APPLICATIONS

- High resolution analog to digital converters (ADC)
- High Precision digital to analog converters (DAC)
- High linearity signal processing
- Low immunity to noise communication systems
- Successive approximation analog to digital converters
- Comparator null detector
- Zero crossing detector
- Level shifter

CHAPTER 6

CONCLUSION & FUTURE SCOPE

In this project, significant contributions are made towards the comparator to offer high speed with low recoil noise.

The two-stage comparator does not have control over the regeneration speed at small current source, so the delay is more. A Three stage comparator is designed to overcome the limitation of two stage comparator, and it can control the regeneration speed but the recoil noise in the latch stage is more. So, to overcome these disadvantages using Lector technique another three-stage comparator is designed, this comparator achieves a high-speed characteristic, but the transistor count increased drastically resulting in increasing the area and recoil noise is quite similar.

The speed and recoil noise are the main aims of the proposed model. To increase the speed voltage charge pump is used to drive the latch more than voltage VDD. To reduce recoil noise inverters are used at output nodes. This achieves better results. Power consumption was also reduced due to the absence of extra path which was presented in conventional model.

This type of comparator can be a better component in ADC's. As it has high-speed characteristics it can give the result faster than any other comparator. Many electronic industries rely on comparators to produce ADCs, so our comparator might be a better choice where high speed and low power consumptions are required. This can bring advancement in ADC technology.

CHAPTER 7

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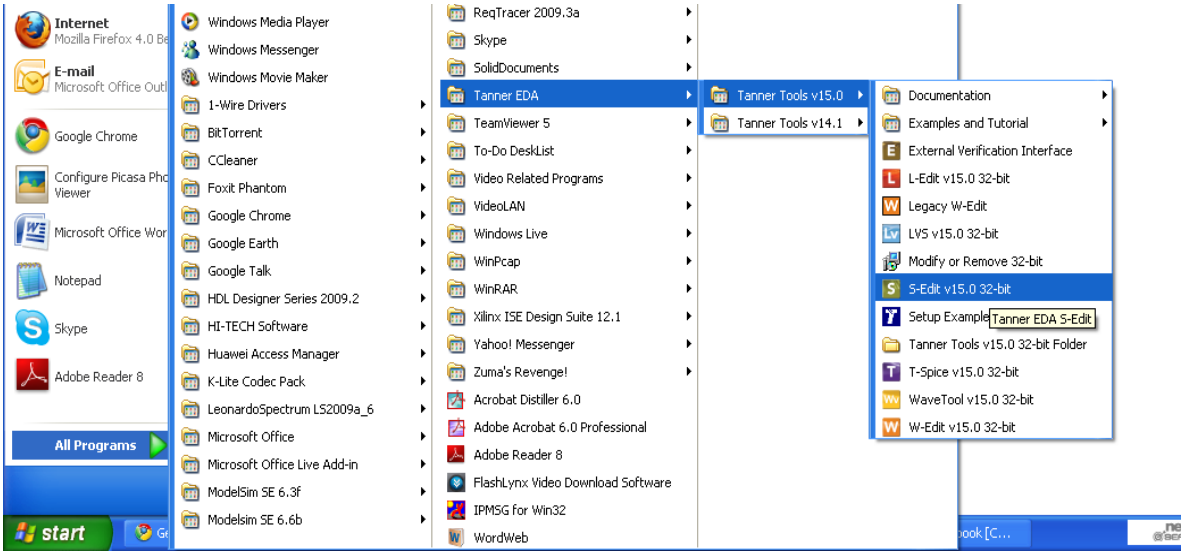
Appendix-1

Tanner tool V16 Tutorial

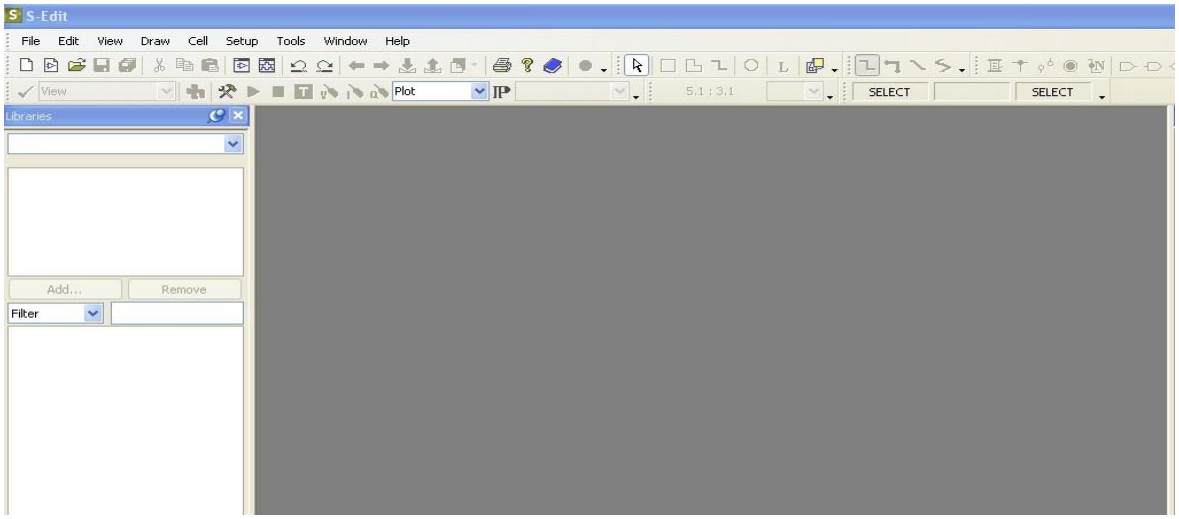
S-EDIT

The following is the path for opening S-Edit tool:

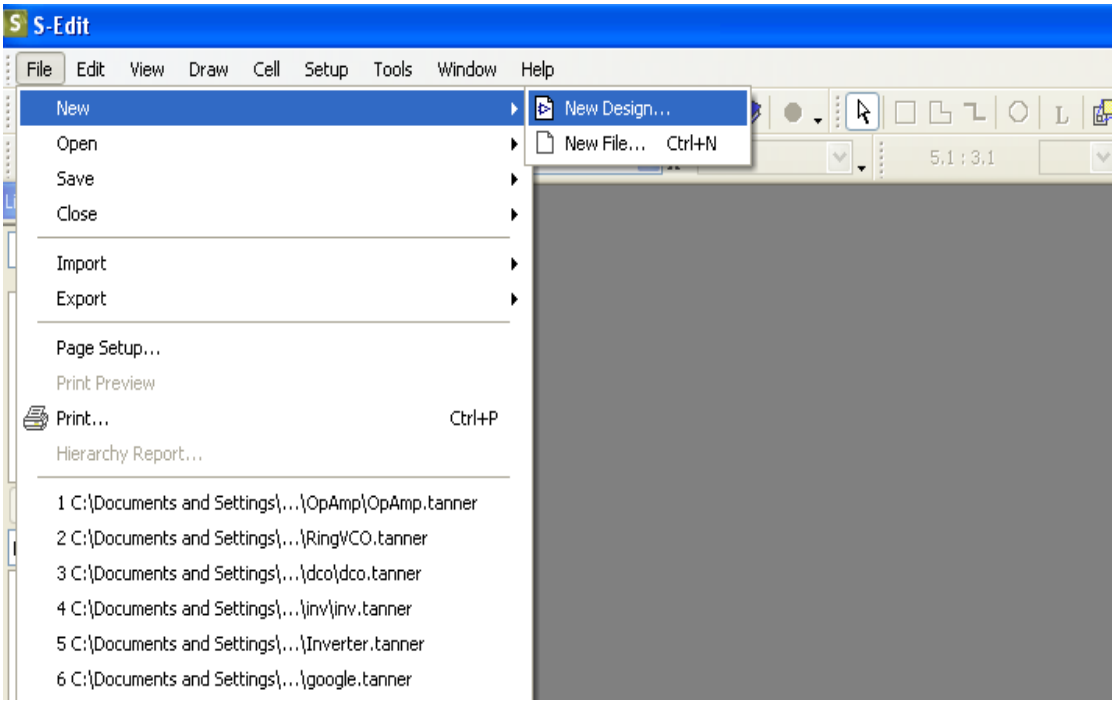
Start -> All Programs -> Tanner EDA -> Tanner V 16 -> S-Edit V16.0 64 Bit



To do schematic entry, run S-Edit tool



To create a new design: File -> New Design

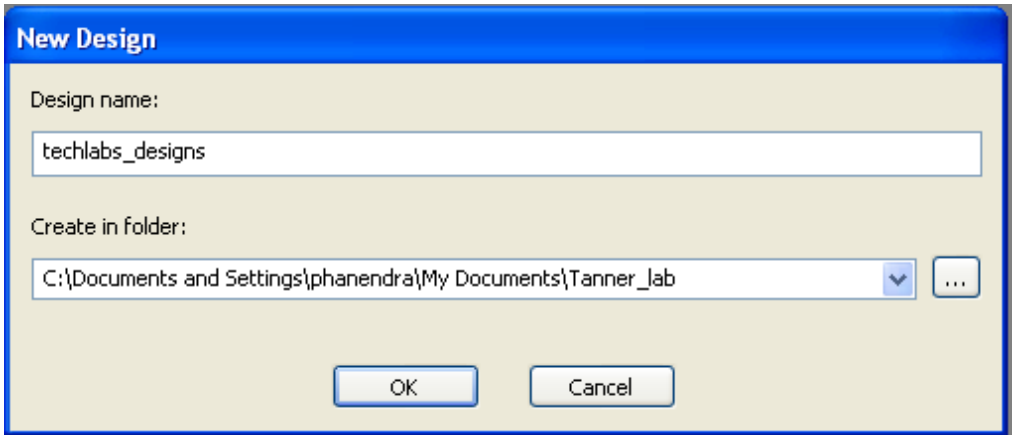


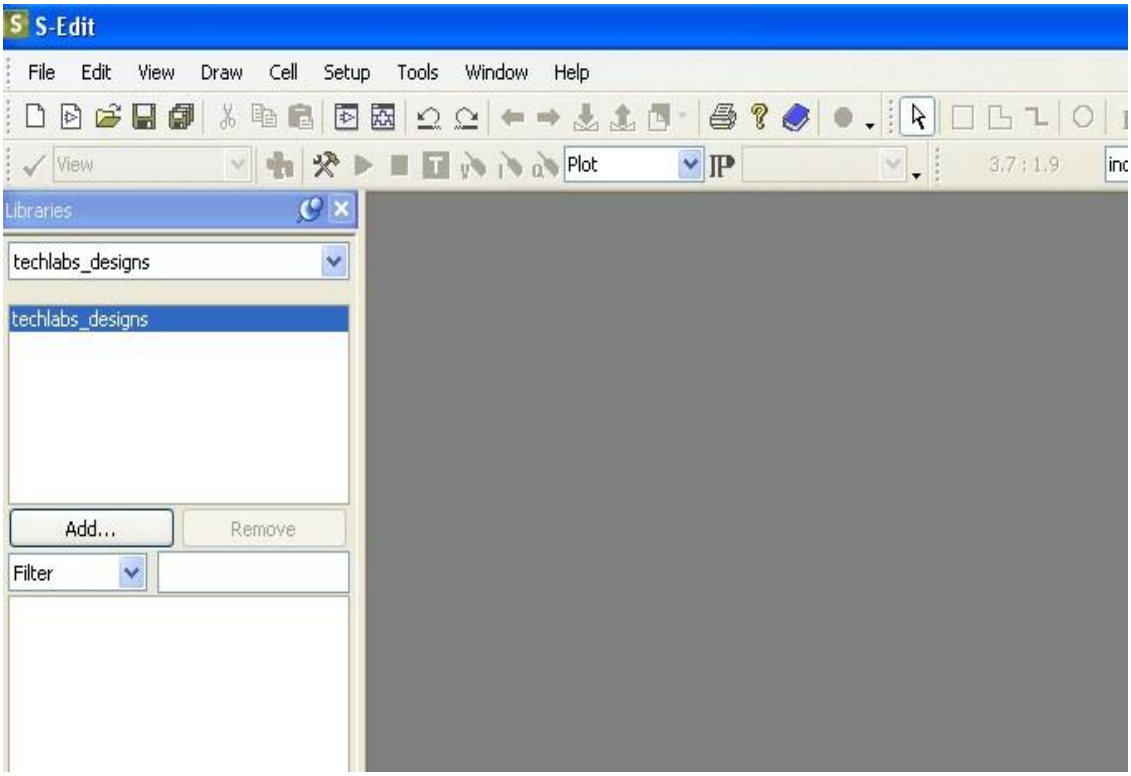
Enter the design name and give the path where it should

be saved.Example: techlabs_designs is the design

folder

C:\Documents and Settings\phanendra\My Documents\Tanner_lab is the targetlocation of design folder



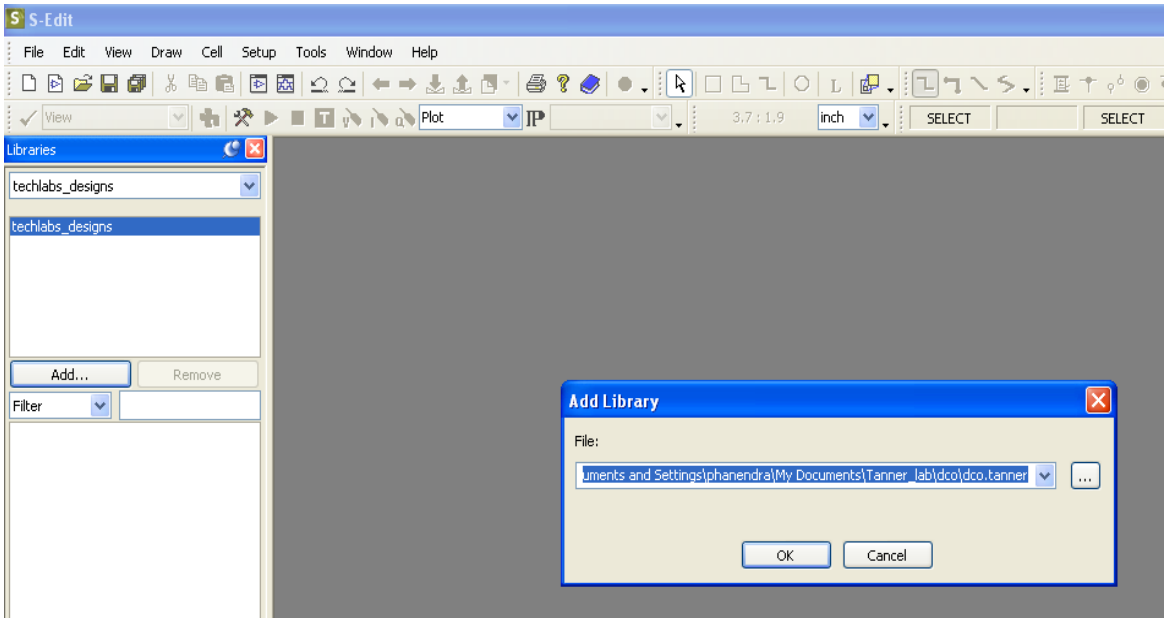


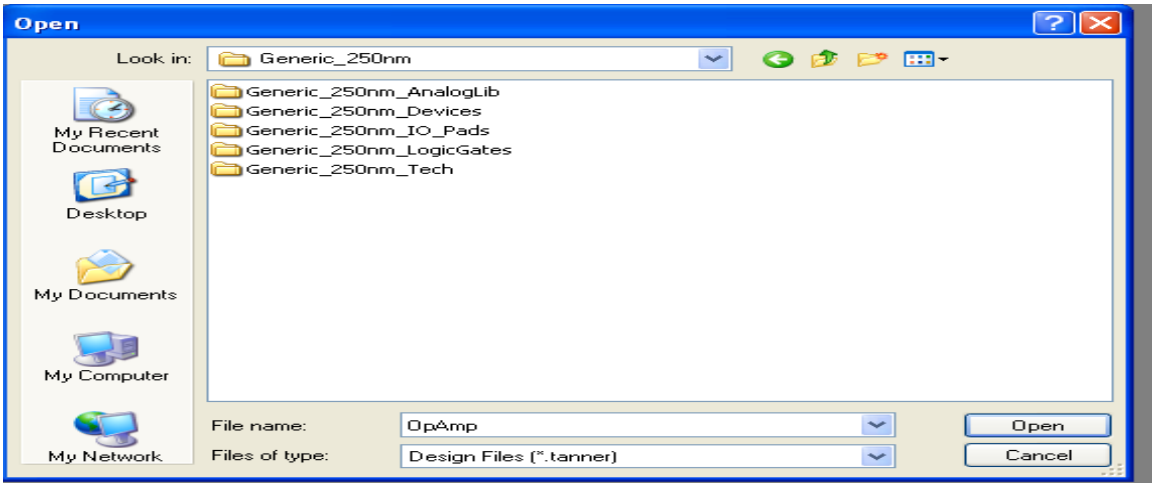
Add component libraries. The path for component libraries

is given below.My Documents\Tanner EDA\Tanner Tools

v15.0\Process\Generic_250nm

Click add in S-Edit window for adding the libraries and follow the path of processfolder.

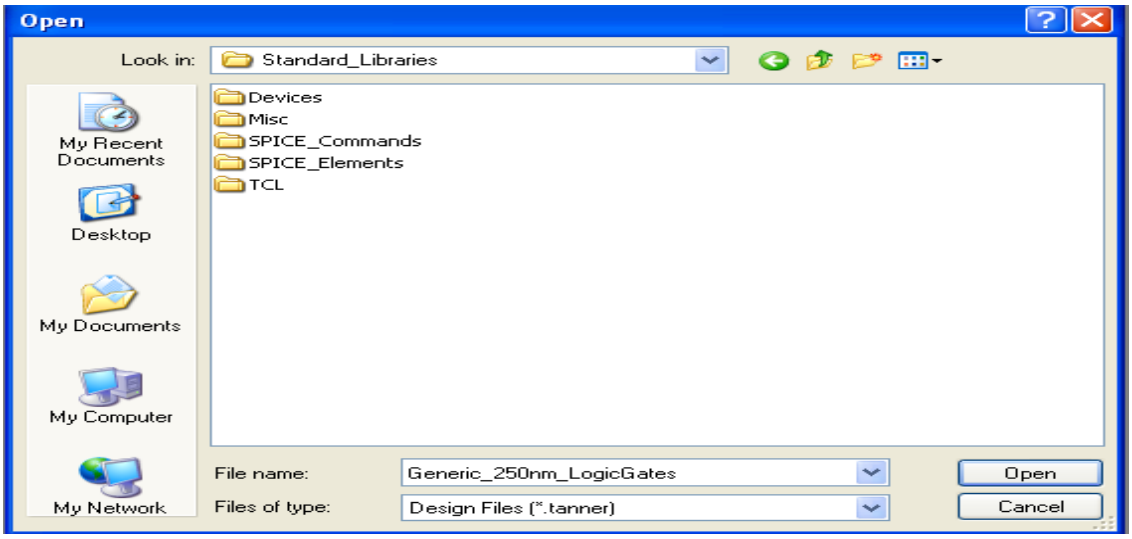




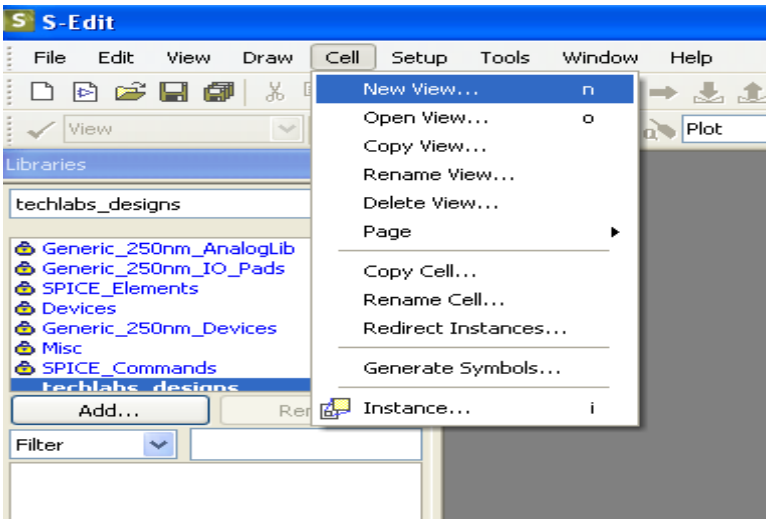
Double click all the component libraries under Generic_250nm and add all tannerdatabase files (.tdb).

To add Spice commands and Spice Elements for setting spic e simulation follow thepath.

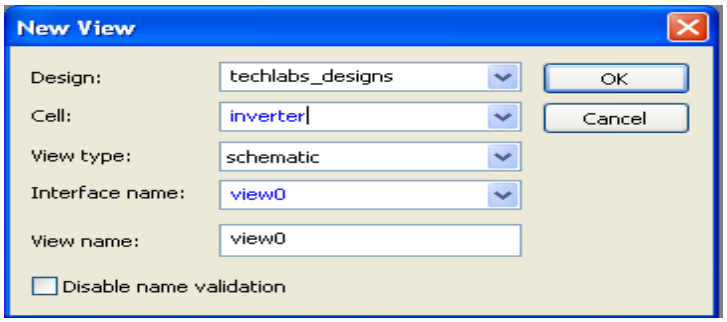
My Documents\Tanner EDA\Tanner Tools v16.0\Process\Standard Libraries

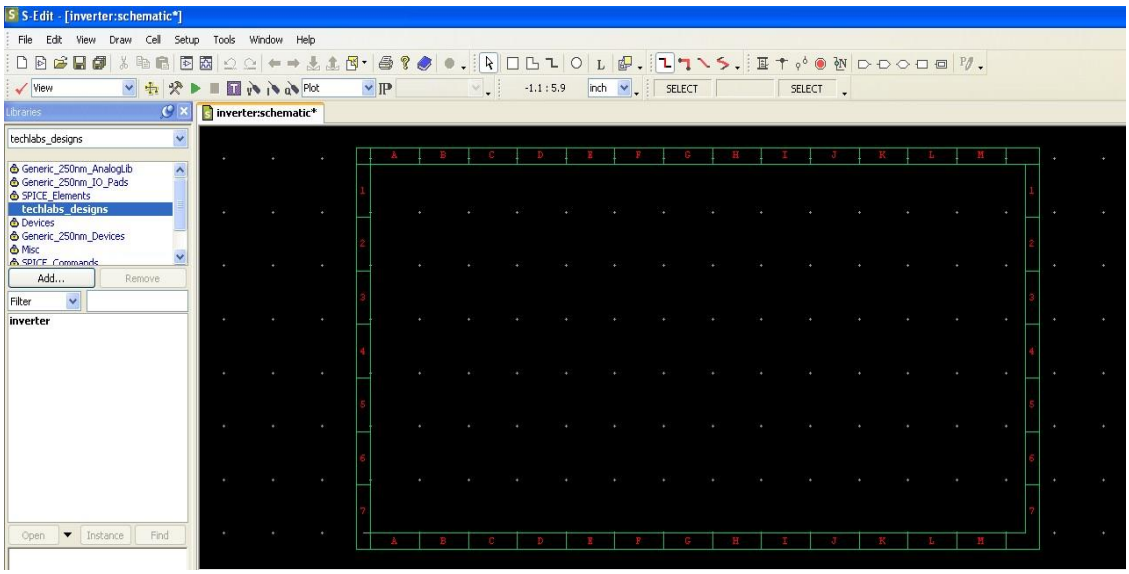


Now, we need to create a new cell.



Give a new name for cell

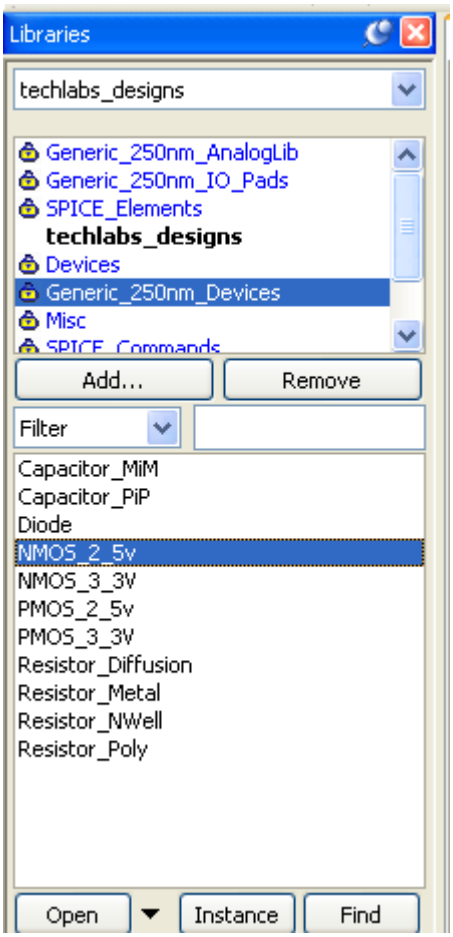




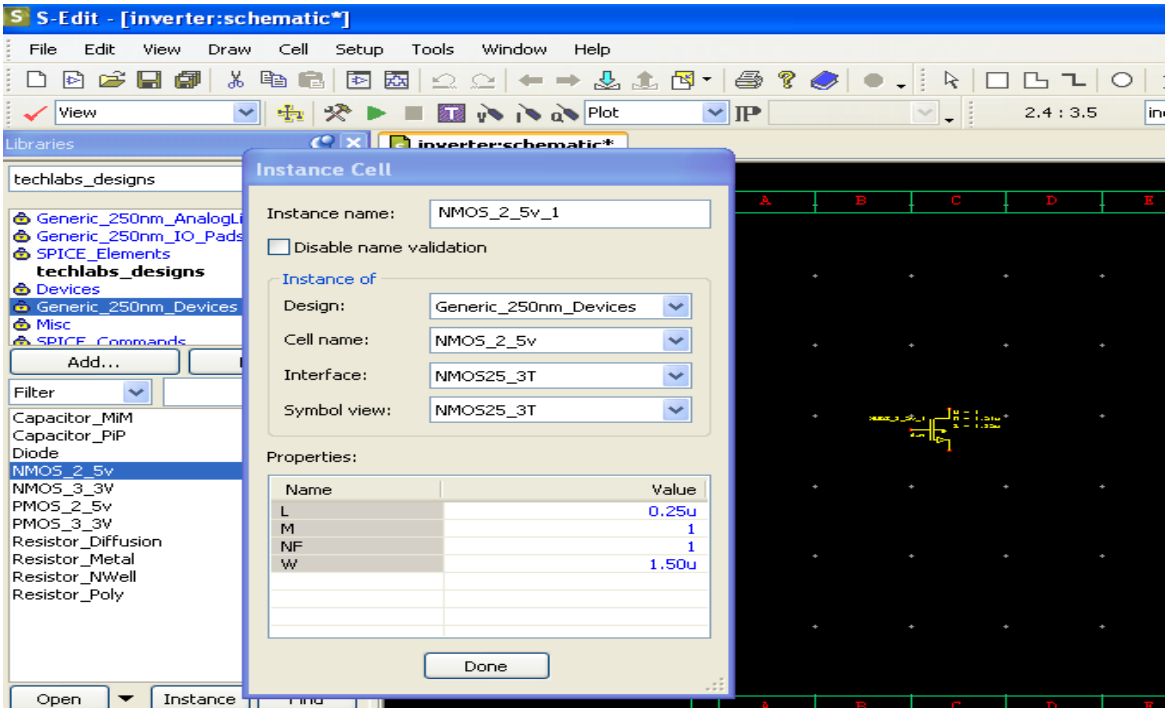
Scroll mouse for Zoom in and Zoom Out. And to view entire

design press homebutton on keyboard.

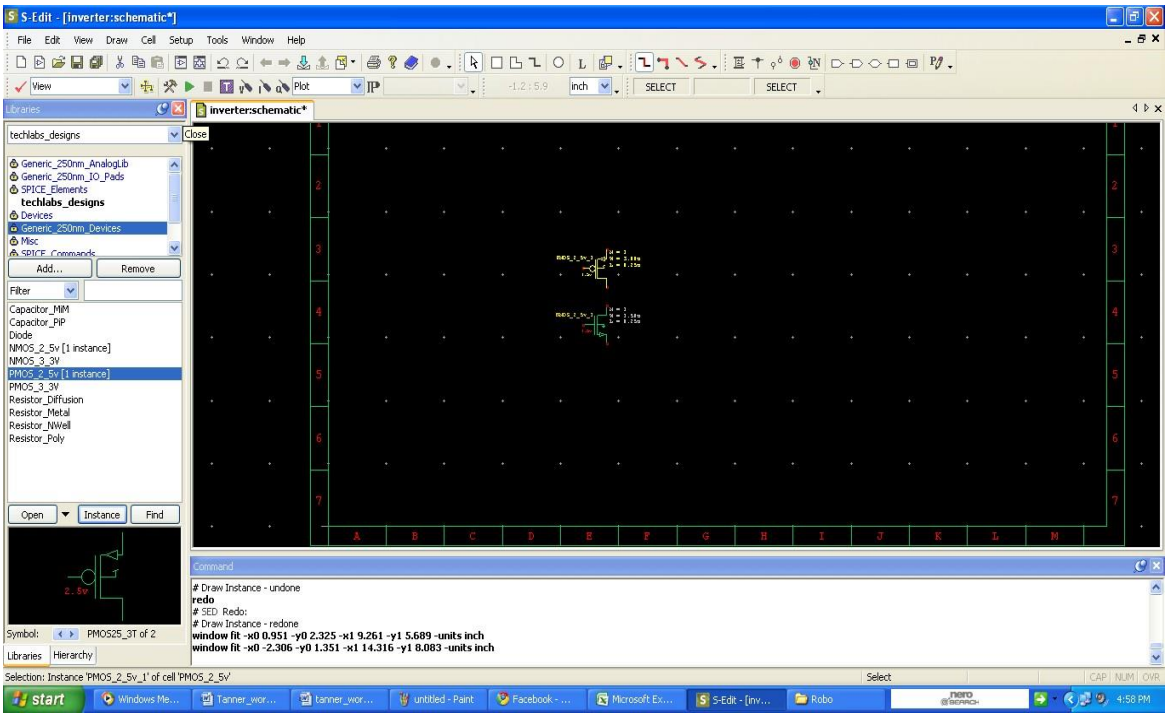
Click on Generic_250nm_Devices folder on libraries



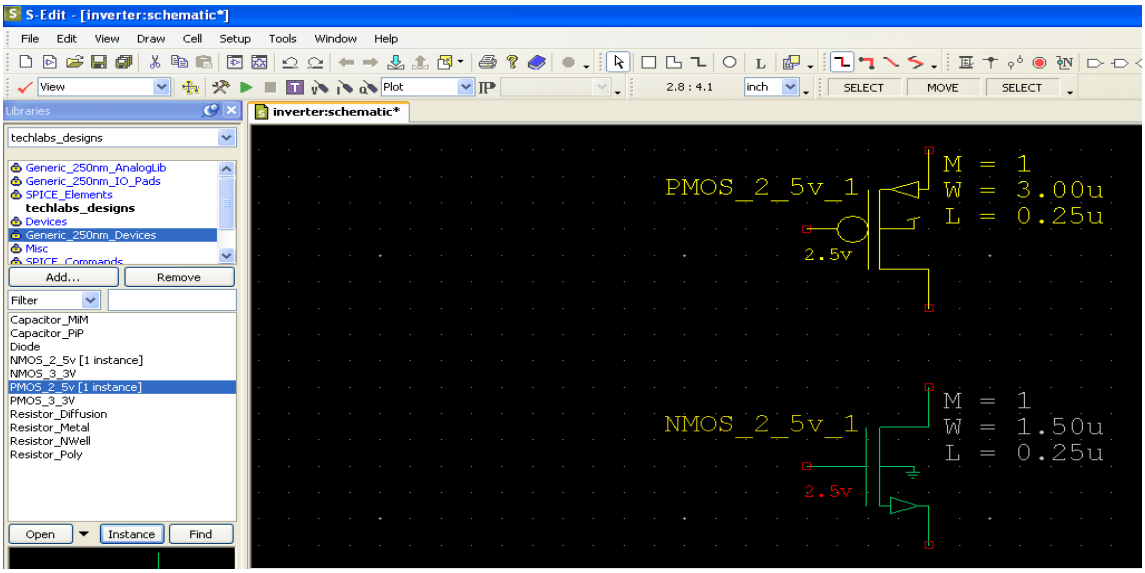
To add any component either drag the component on to the design area (black region with grids) or click Instance, then Instance Cell pops up where a user can change the properties. Keeping the icon on the design area, components icon can be placed N number of times. Either press ESC buttonon keyboard or Done on Instance Cell window to stop placing of cells.



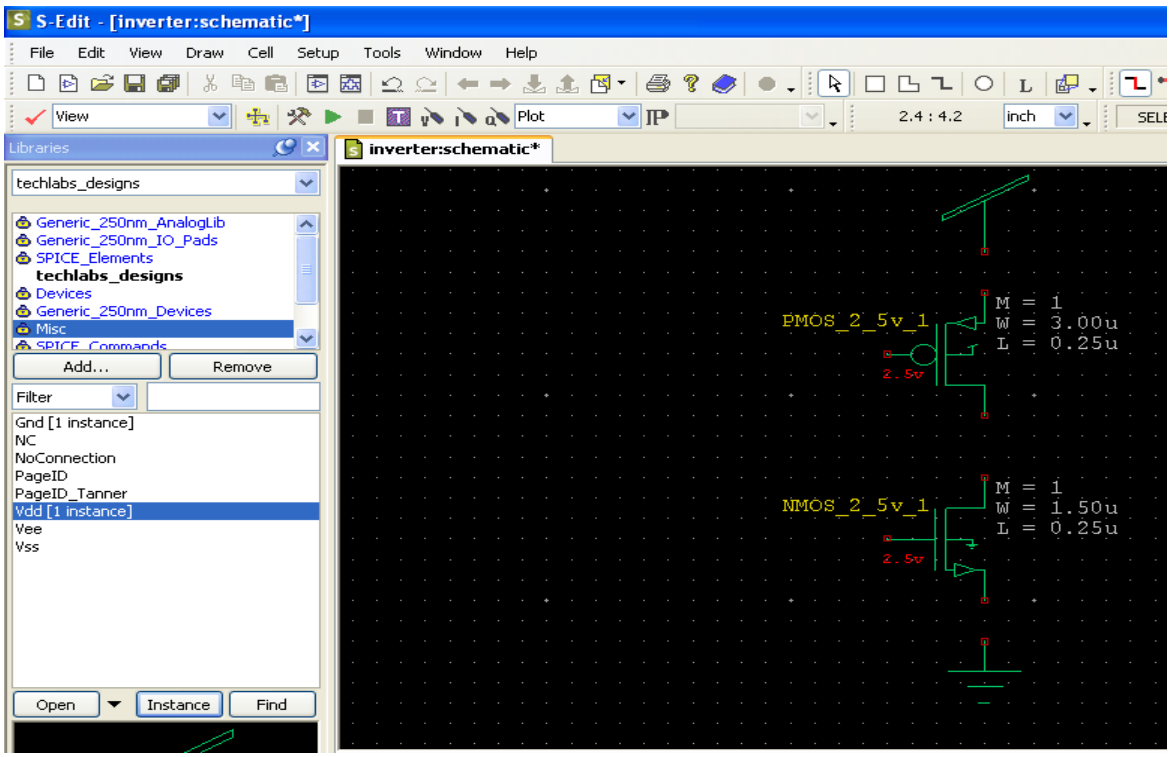
In the same way place PMOS component on the design area.



To Zoom the design area, scroll the mouse or press home button on keyboard.

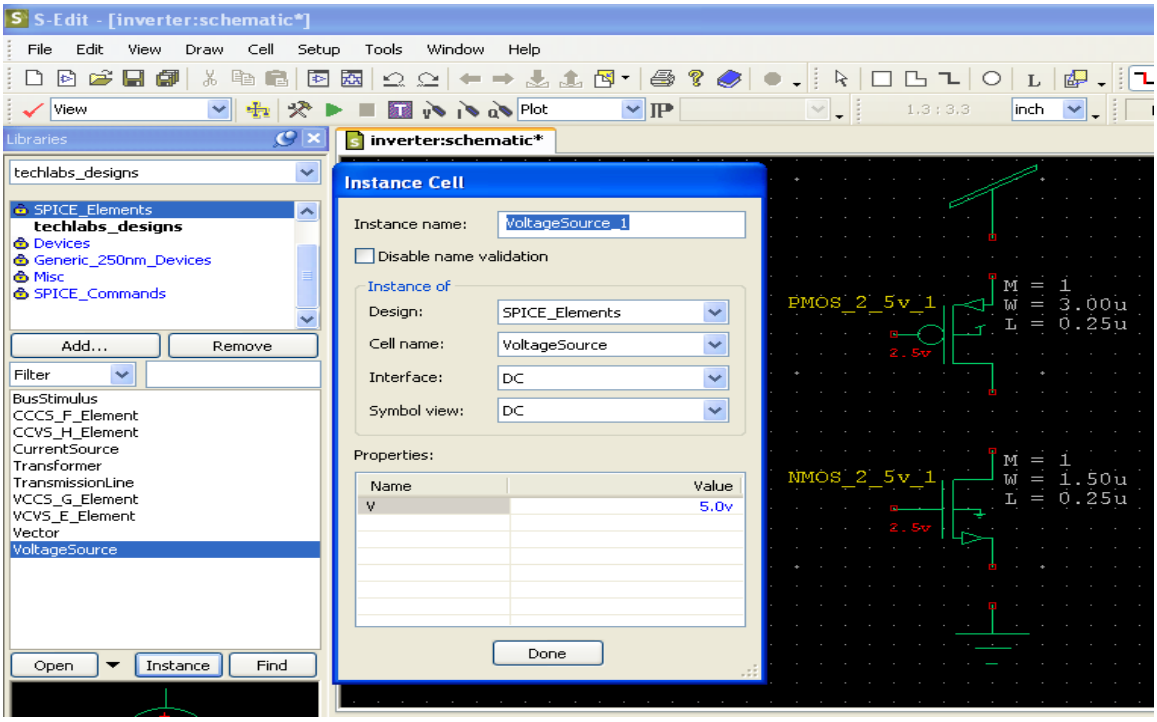


Now place Vdd and Gnd Instances from the Misc folder under Library.



Now place a DC Voltage and Pulse Voltage source from the Spice Elements folderunder Library.

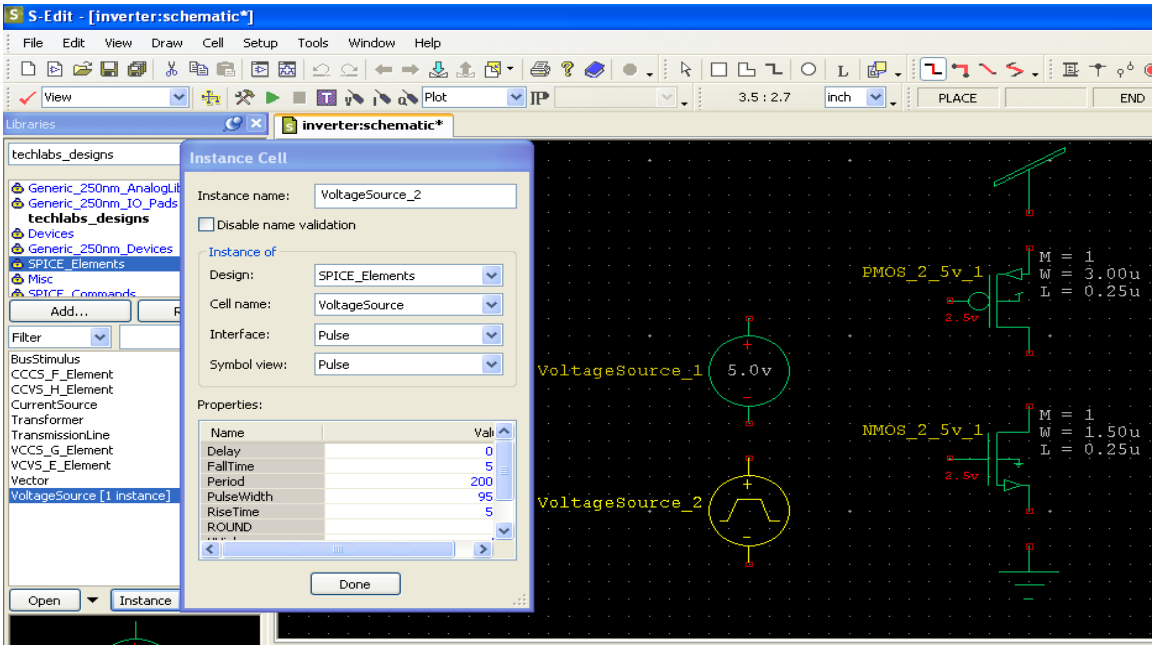
To place a Voltage Source, Click Spice Elements, Under Spice Elements ClickVoltage Source and then Instance.



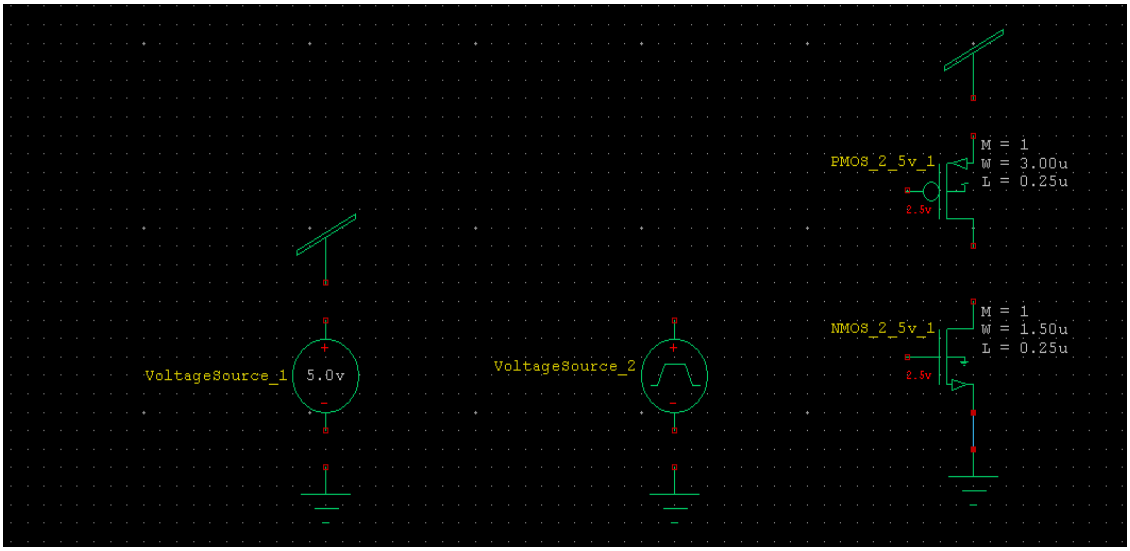
To place a DC voltage source, change the interface to DC and edit the voltage value

Click done only after placing the voltage source on design area.

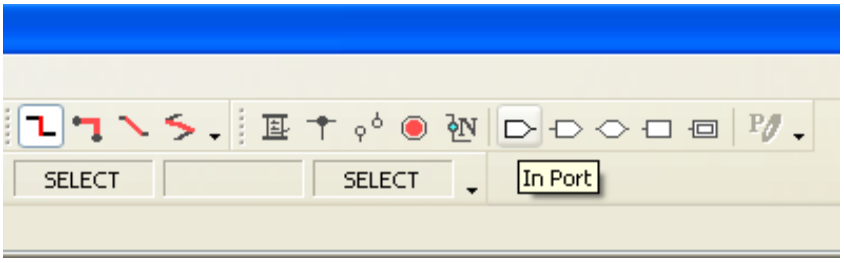
To place a Pulse voltage source, change the interface to DC and edit the voltagevalue. Click done only after placing the voltage source on design area.

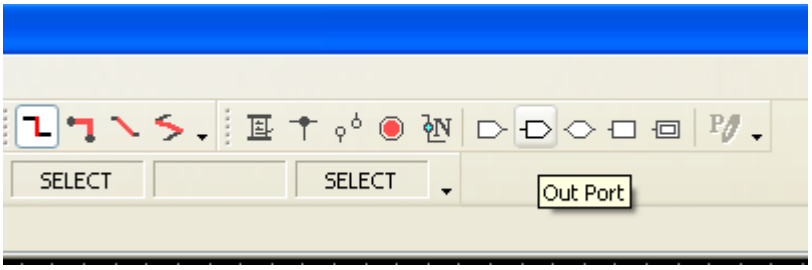


Place Vdd and Gnd even for the voltage sources as shown.

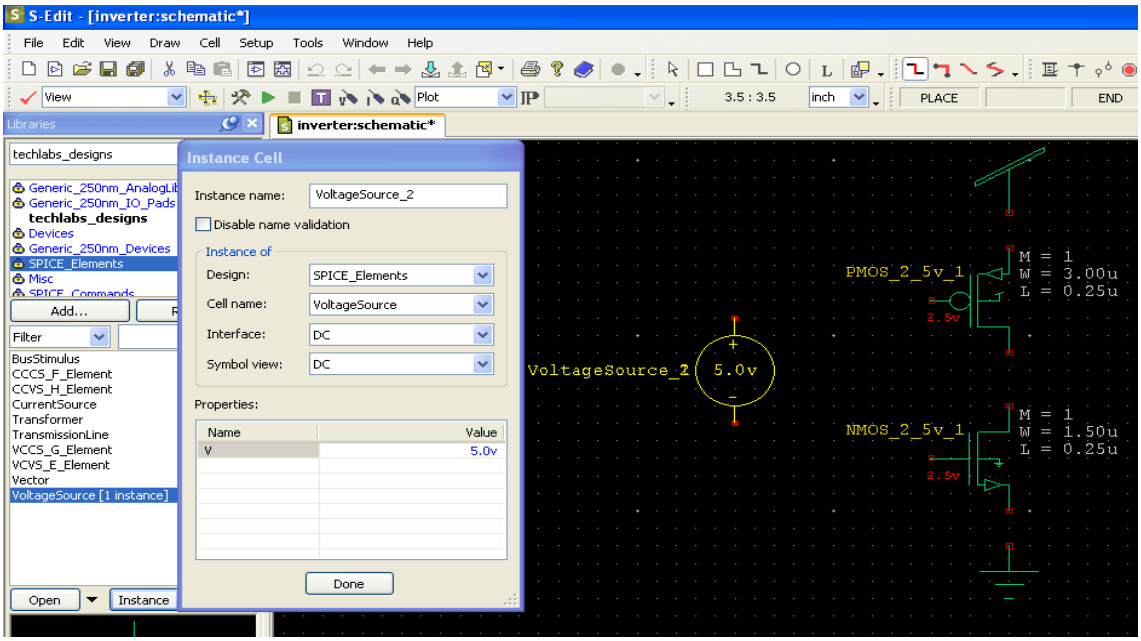


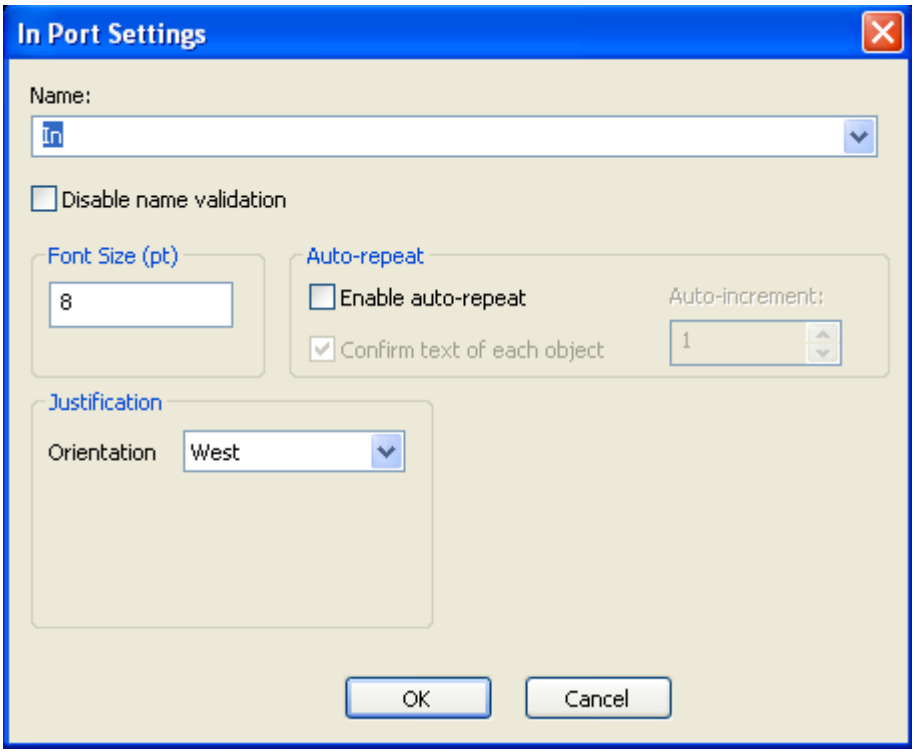
Now place Input and Output ports.



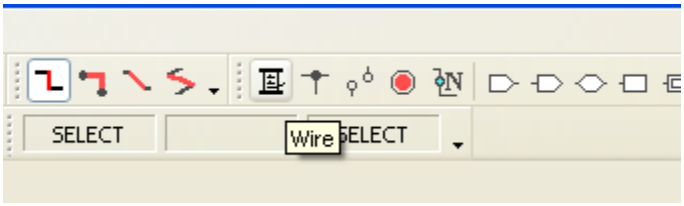


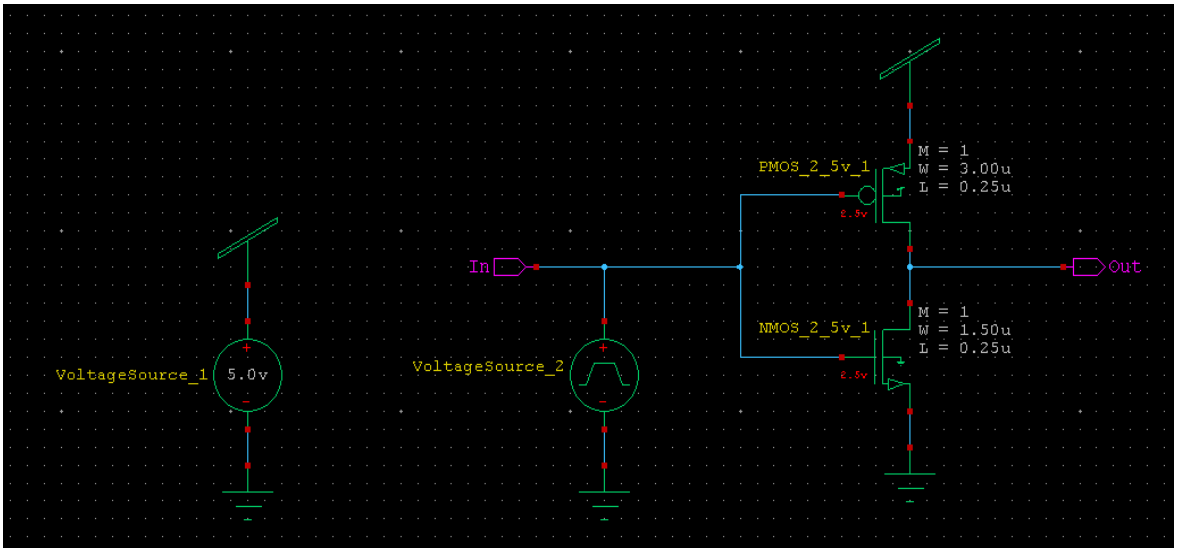
When an input port is placed, in port window pops up where we can edit the portname, font size and orientation. Even the port orientation can be changed by pressing r button on key board.



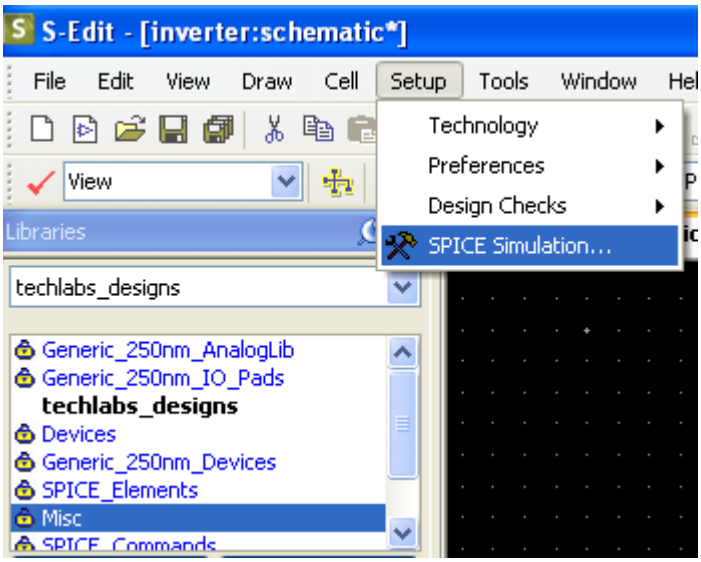


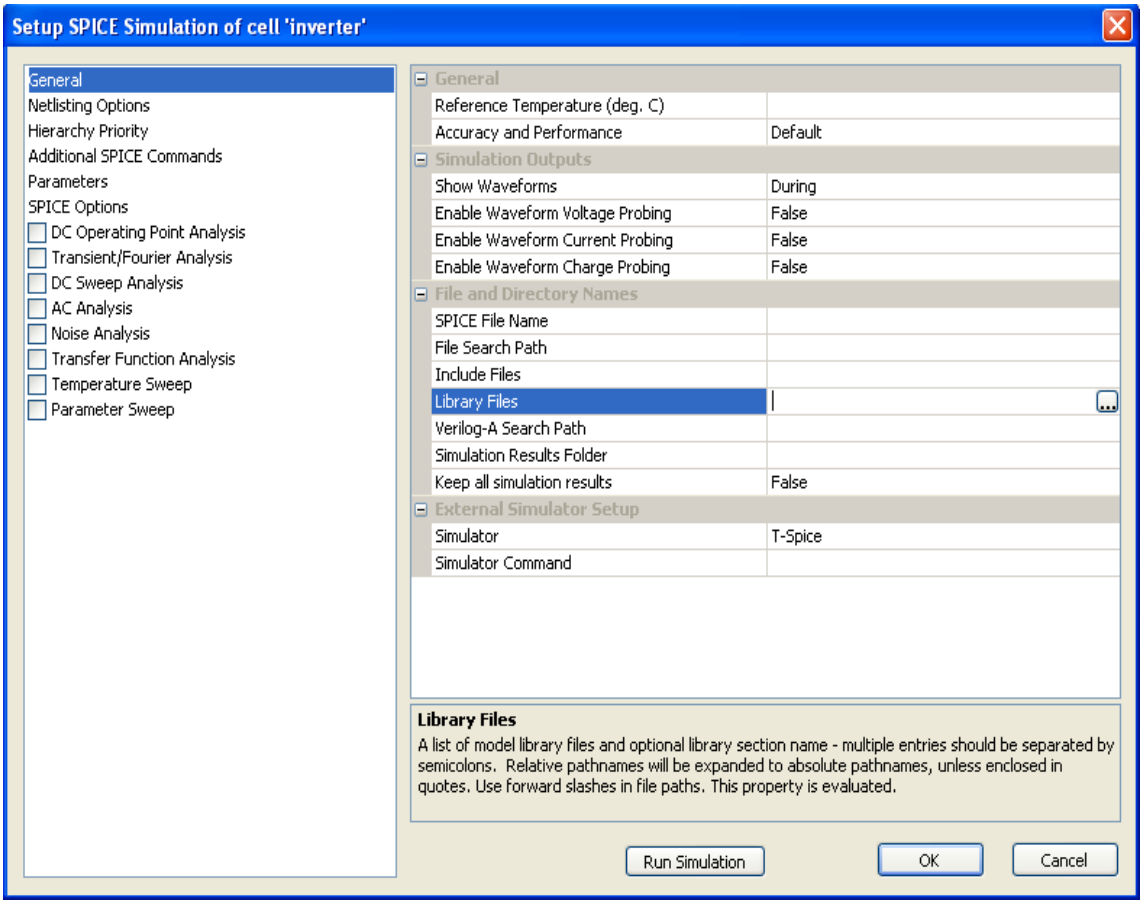
Now we have placed all the components on the design window. And connections aremade using the wire as shown below





Now we need to set up simulation.





Now, give the path of library file.

My Documents\Tanner EDA\Tanner Tools v16.0\Process\Generic_250nm\ Generic_250nm_Tech \Generic_250nm.lib
After giving the path of Generic_250nm.lib, add TT as shown below.

My Documents\Tanner EDA\Tanner Tools v16.0\Process\Generic_250nm\ Generic_250nm_Tech \Generic_250nm.lib TT
TT is the corner model used. There are different types of Corner models in .lib file

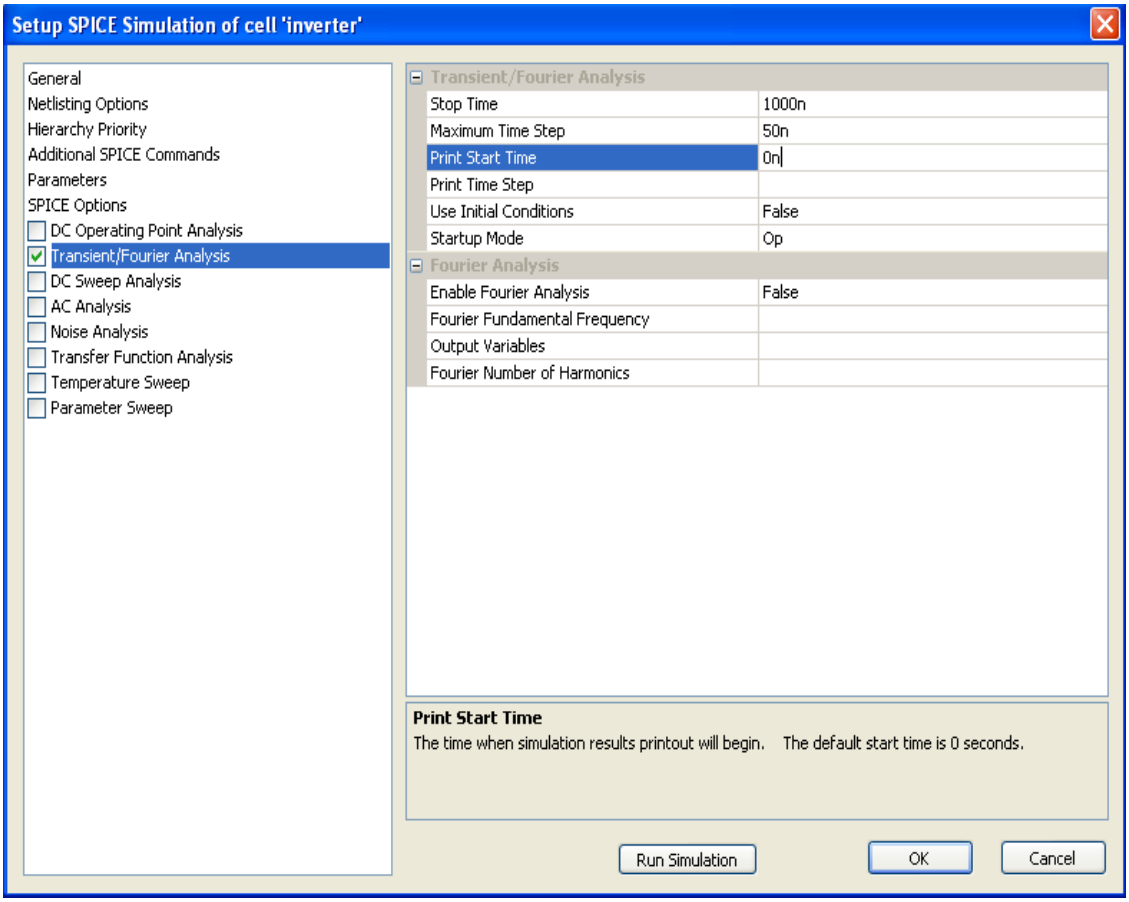
TT: Typical model for NMOS & PMOS

SS: Slow NMOS Slow PMOS model

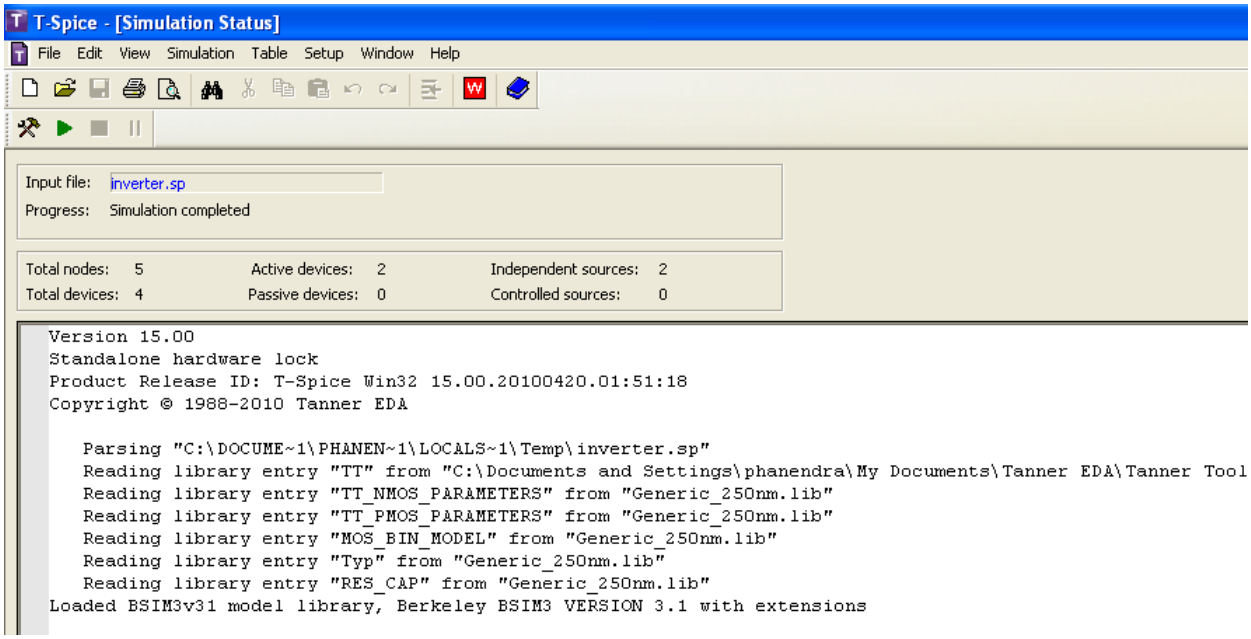
FF: Fast NMOS Fast PMOS model

SF: Slow NMOS Fast PMOS model

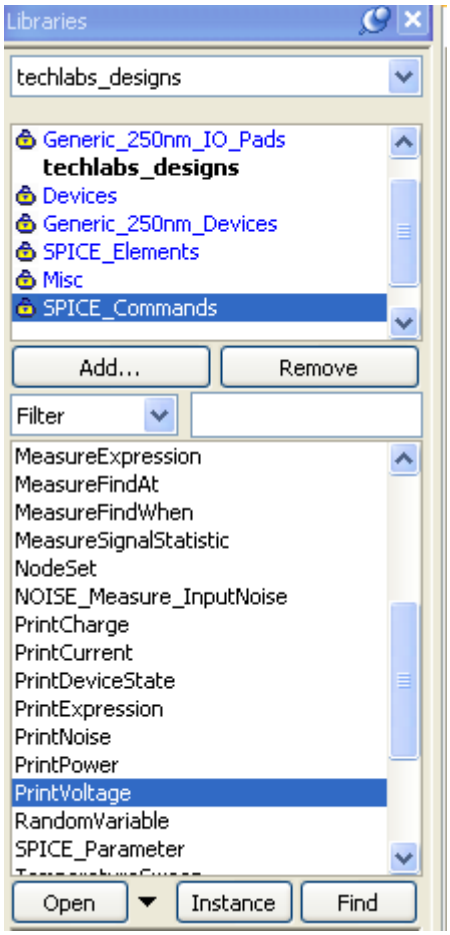
Set Transient Analysis as shown below.

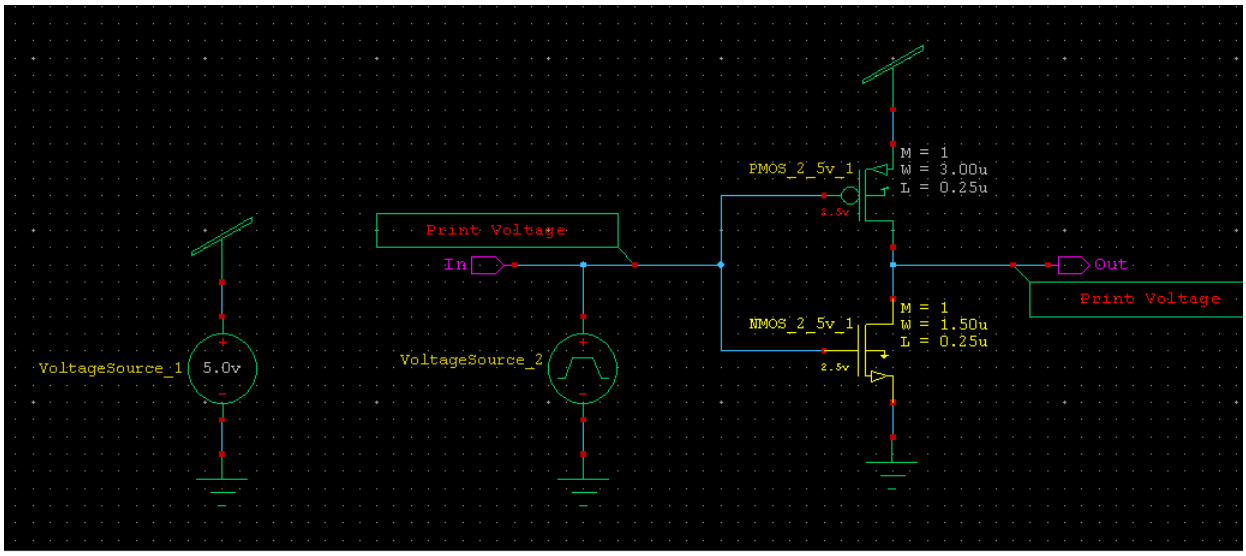


Run Simulation.



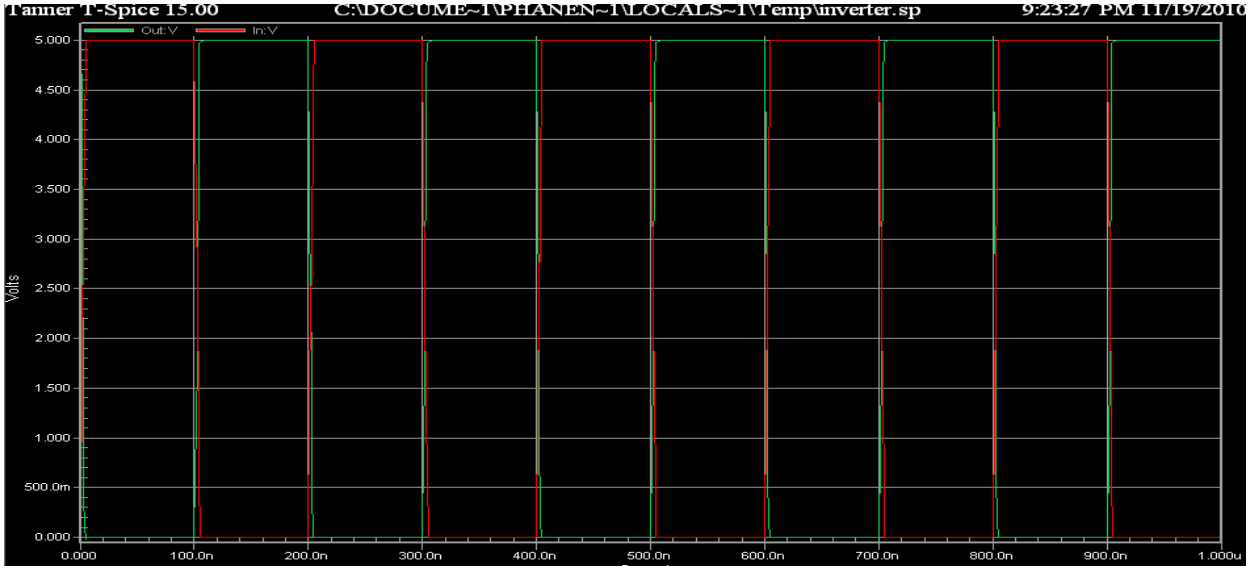
To view waveforms, place Print Voltage from Spice Commands library.



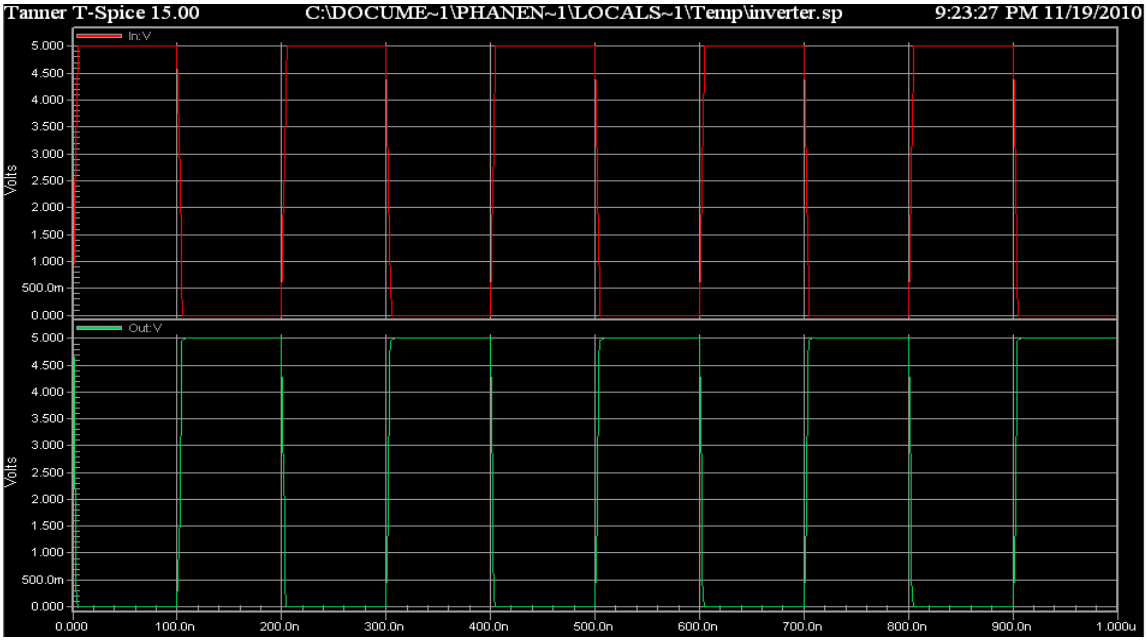


Now, Run Simulation.

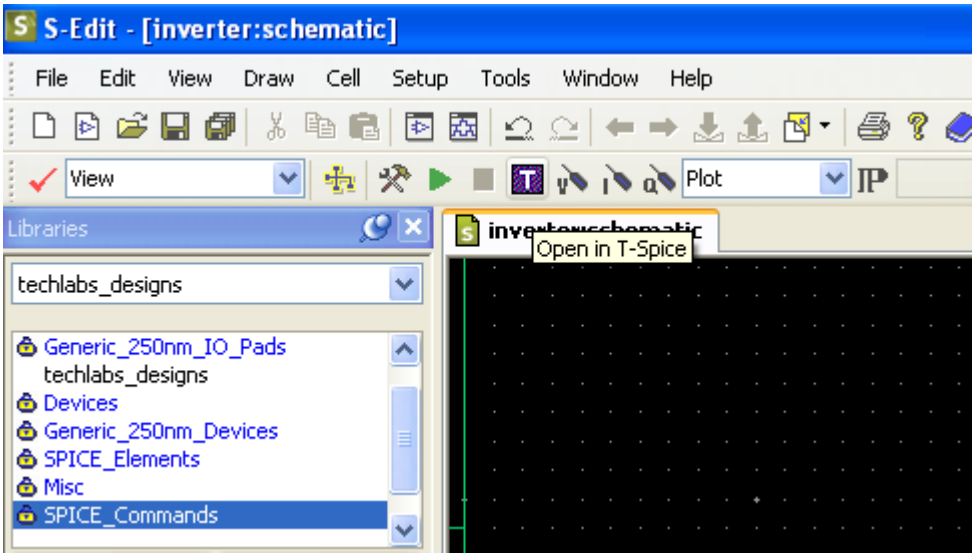
Waveforms can be viewed on W-Edit tool once Simulation is Run again.



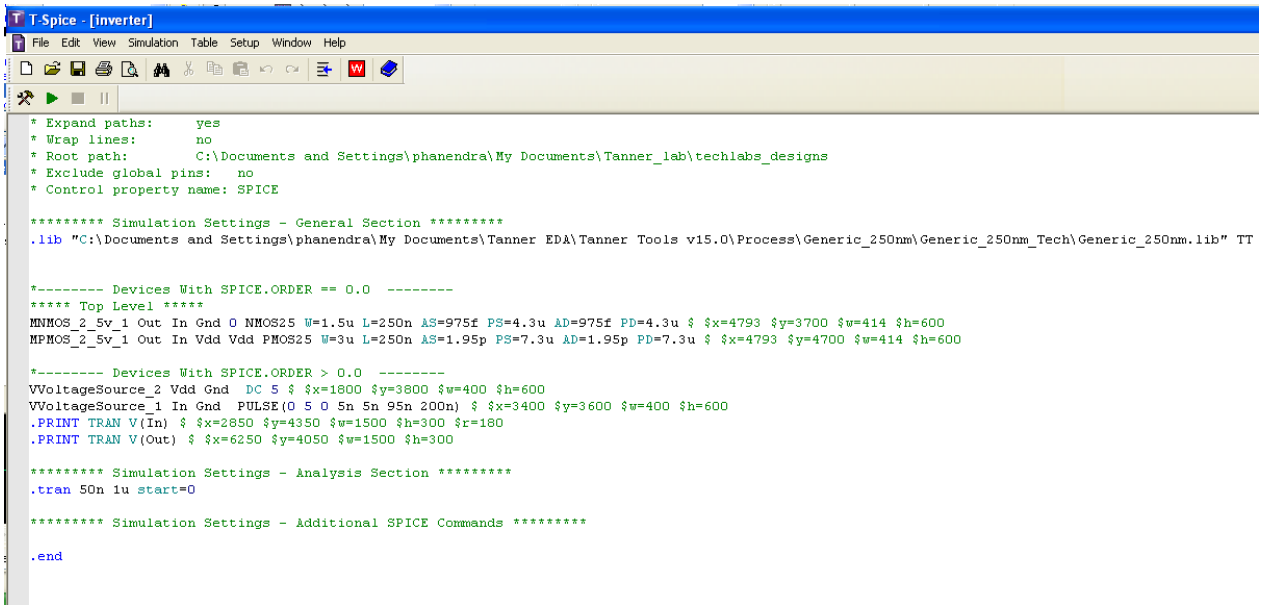
Waveforms can be expanded by clicking Chart ◊ Expand Traces on W-Edit window.



To extract the spice netlist from schematic, go to S-Edit and click the T-Spice option.



The following spice netlist is extracted from the schematic which contains the information of the circuit connections across its nodes, analysis setup, voltagesapplied and type of library used for simulation.



Save the netlist as inverter_sch. sp

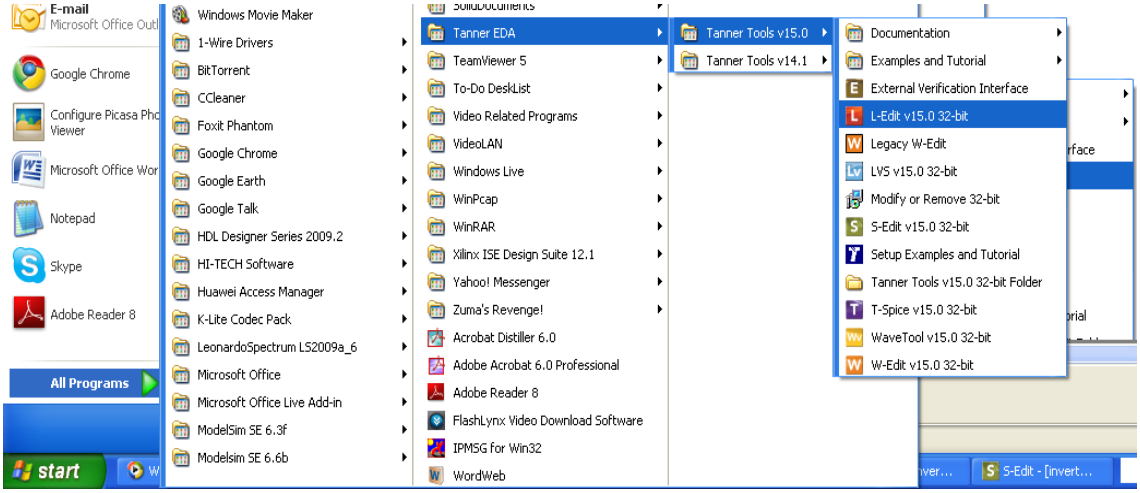
********* Simulation Settings - General Section *********
.lib "C:\Documents and Settings\phanendra\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT
*-------- Devices With SPICE.ORDER == 0.0 --------
***** Top Level *****

MNMOS_2_5v_1 Out in Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975fPD=4.3u $ $x=4793 $y=3700 $w=414 $h=600
MPMOS_2_5v_1 Out in Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3uAD=1.95p PD=7.3u $ $x=4793 $y=4700 $w=414 $h=600
*-------- Devices With SPICE.ORDER > 0.0 --------
VVoltageSource_2 Vdd Gnd DC 5 $ $x=1800 $y=3800 $w=400 $h=600 VVoltageSource_1 In Gnd PULSE (0 5 0 5n 5n 95n 200n) $ $x=3400 $y=3600 $w=400 $h=600
.PRINT TRAN V(In) $ $x=2850 $y=4350 $w=1500 $h=300 $r=180
.PRINT TRAN V(Out) $ $x=6250 $y=4050 $w=1500 $h=300
********* Simulation Settings - Analysis Section *********
. tran 50n 1u start=0
********* Simulation Settings - Additional SPICE Commands *********
. end

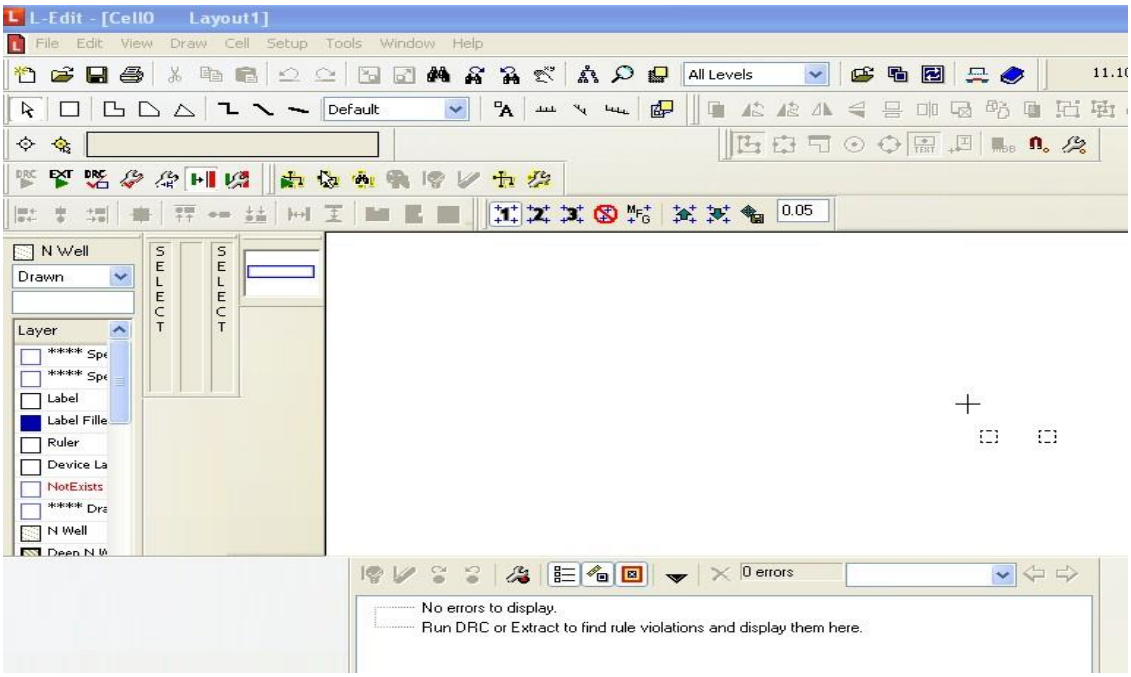
L-EDIT

The following is the path for opening L-Edit tool:

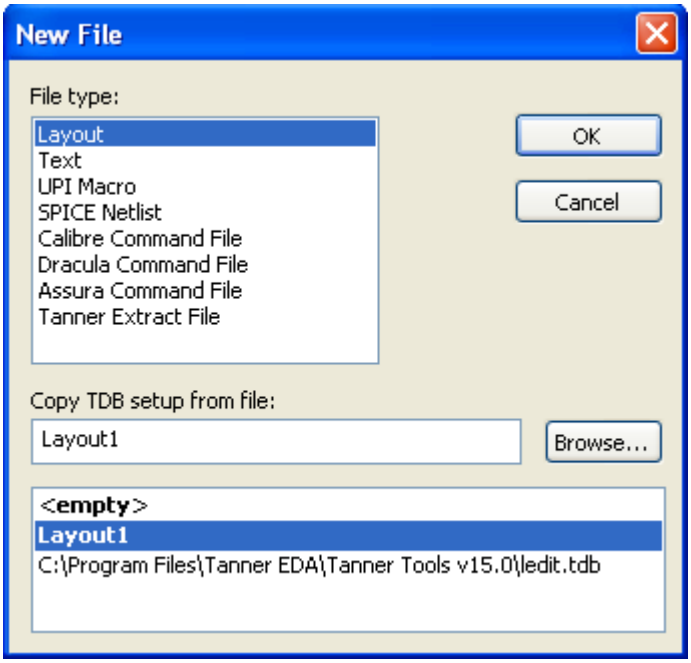
Start -> All Programs -> Tanner EDA -> Tanner V16 -> L-Edit V16.0 64 Bit



To do Layout, run L-Edit tool. Follow window pops up.

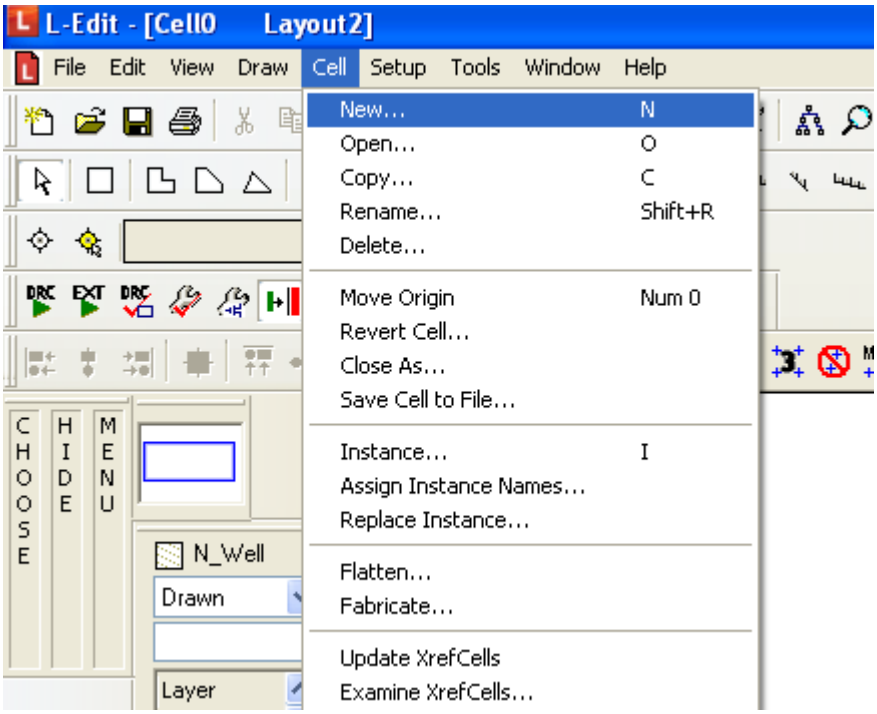


Go to File —> New

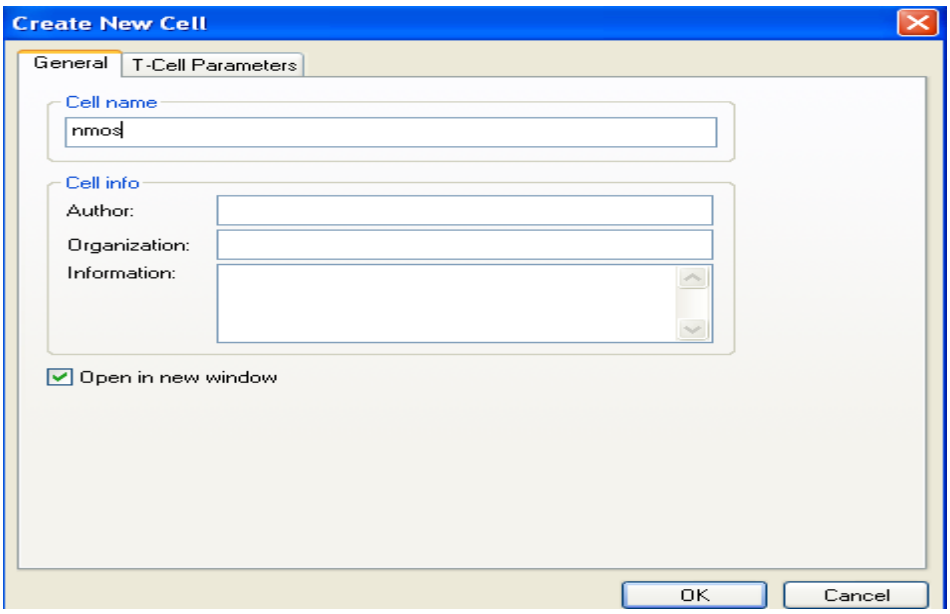


Click Browse –> My Documents\Tanner EDA\Tanner Tools v15.0 \Process
\Generic_250nm \Generic_250nm_Tech and add Generic_250nm_TechSetup.tdb fileand click ok.

Go to Cell —> New



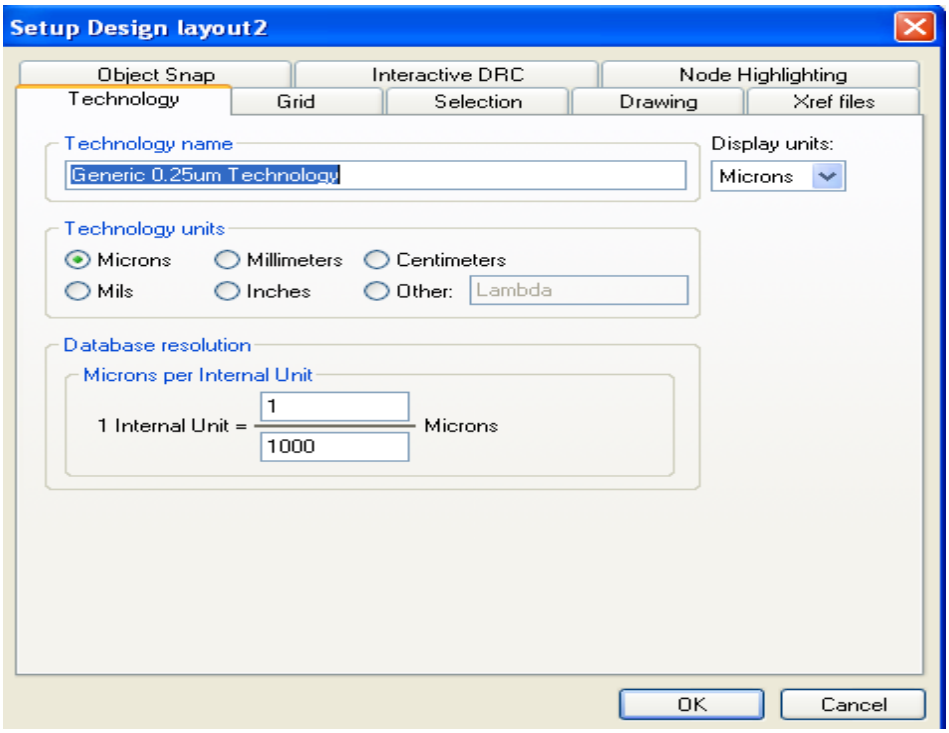
Name the Cell



Grids spacing can be minimized or

maximized using – or + signto change the

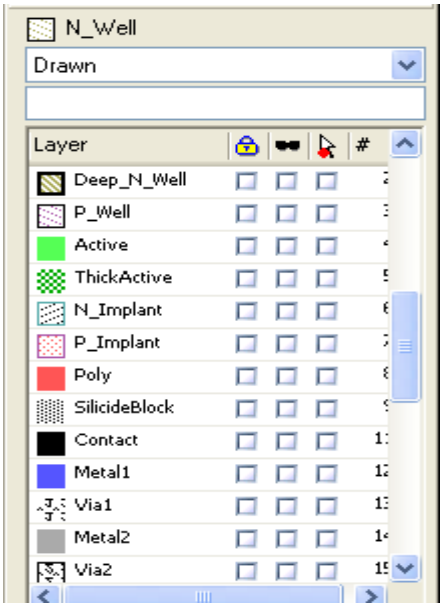
technology Goto setup-> Design



Select Lambda or microns accordingly and click ok

Before designing layout, we need to remember following equations

N Diffusion = N Implant and Active – (1)P Diffusion = P Implant and Active - (2)
From layer palette, we can select layer then for drawing layer we need to switch atDrawing boxes as follows

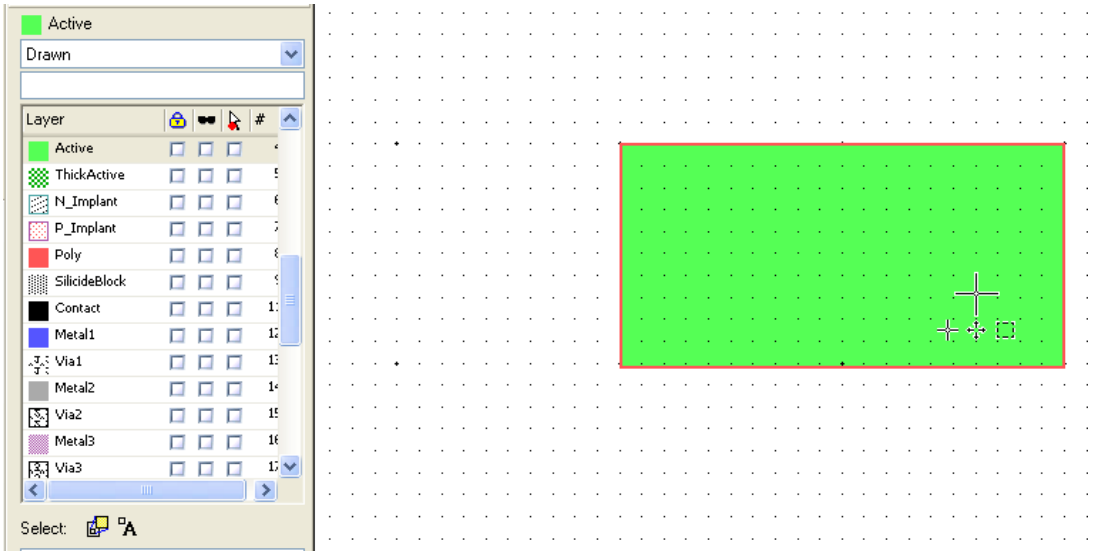


Now we can start layout designing. We are Taking Example of

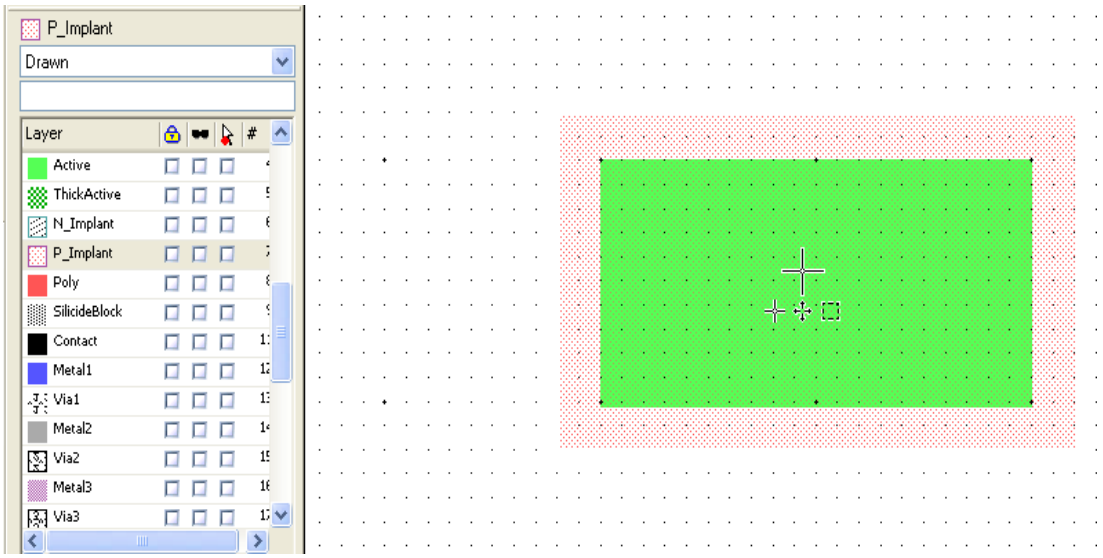
CMOS Layout designBackground of L-Edit is P-Substrate by

default

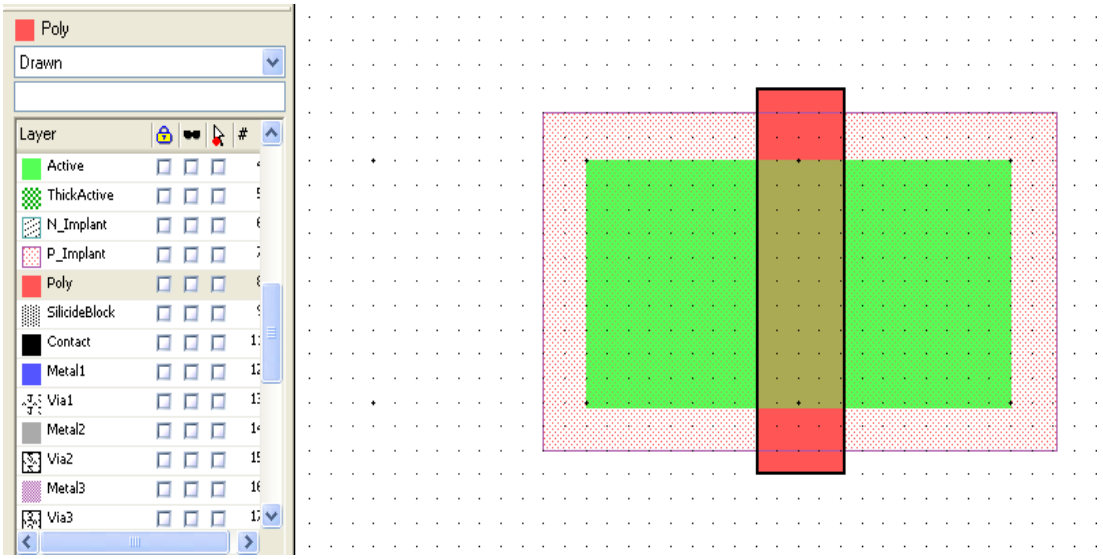
We need to design PMOS, First draw active



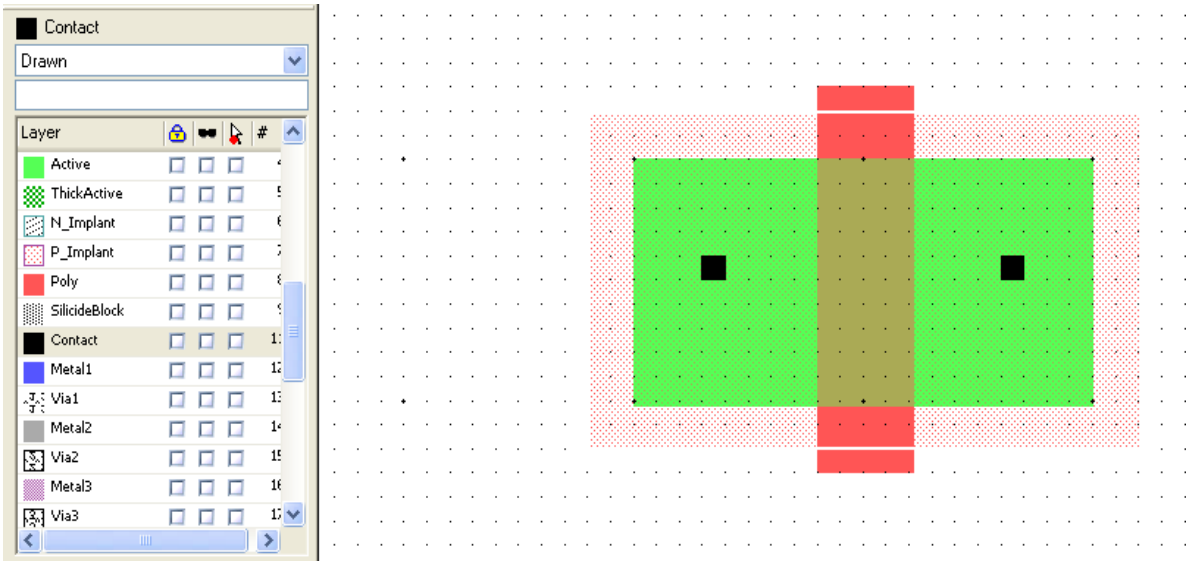
Now draw P Implant over Active with keeping in mind Lambda based design rules



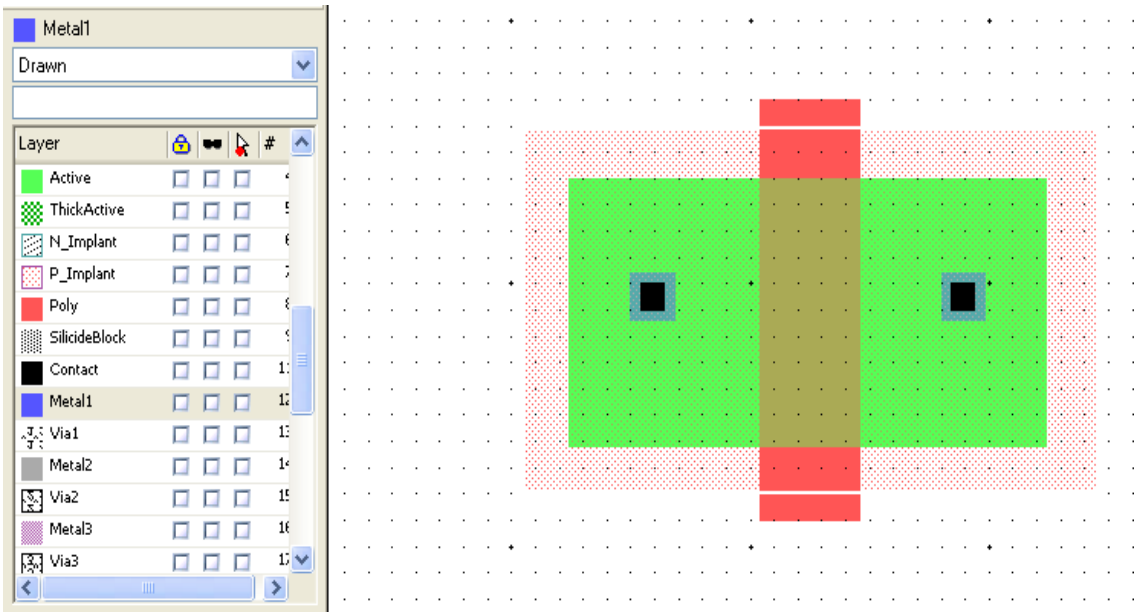
Now draw poly over it accordingly



Now draw Contact for Active region

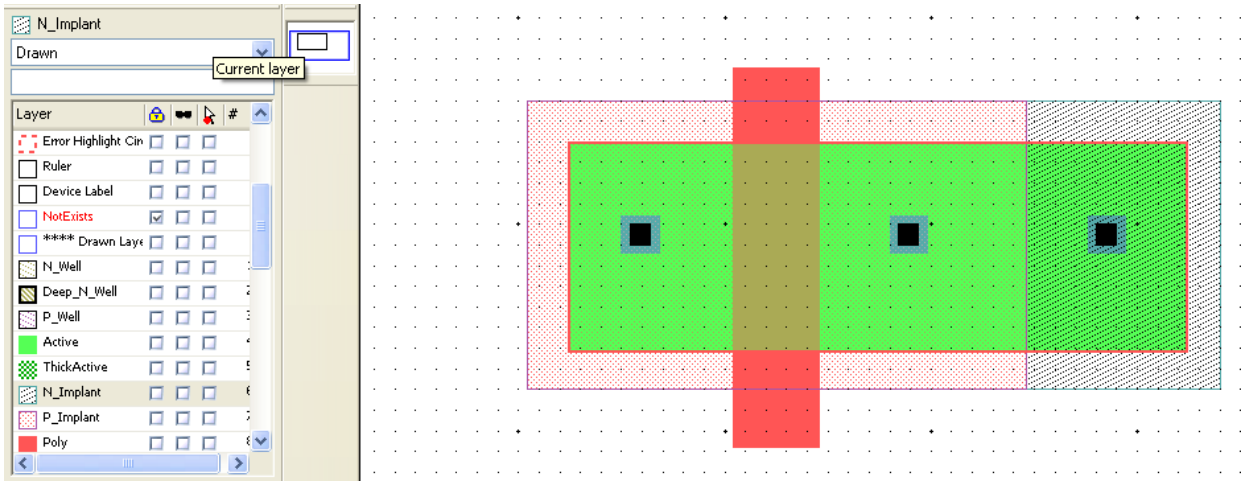


Now draw metal1 around Contact

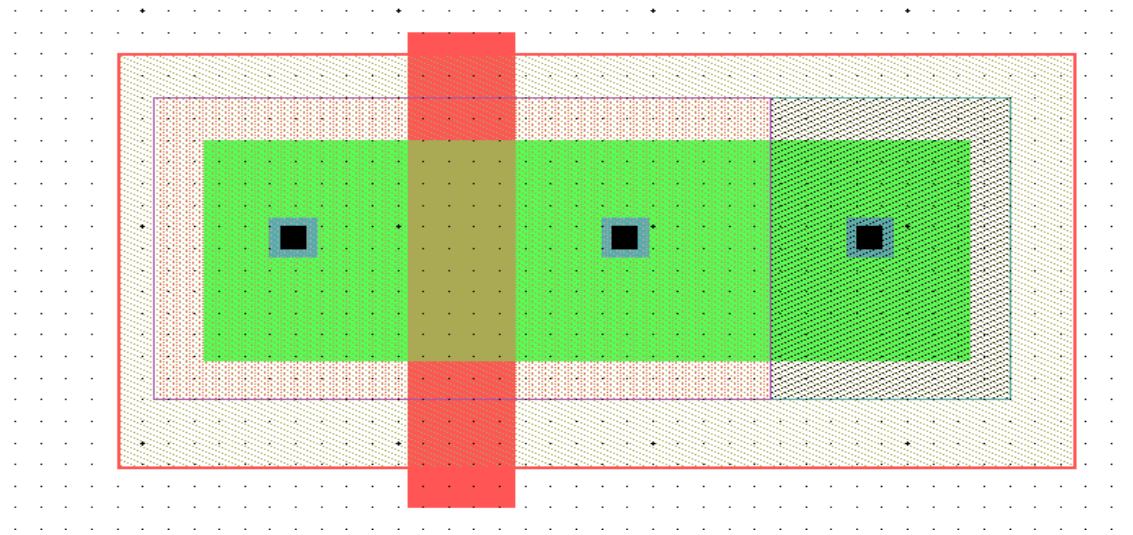


We have designed source, gate and drain.

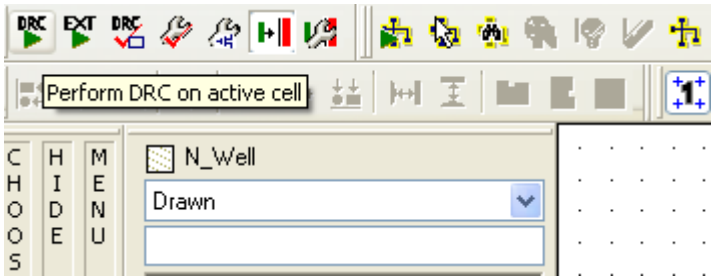
Now we have to design bulk by creating a N+ diffusion



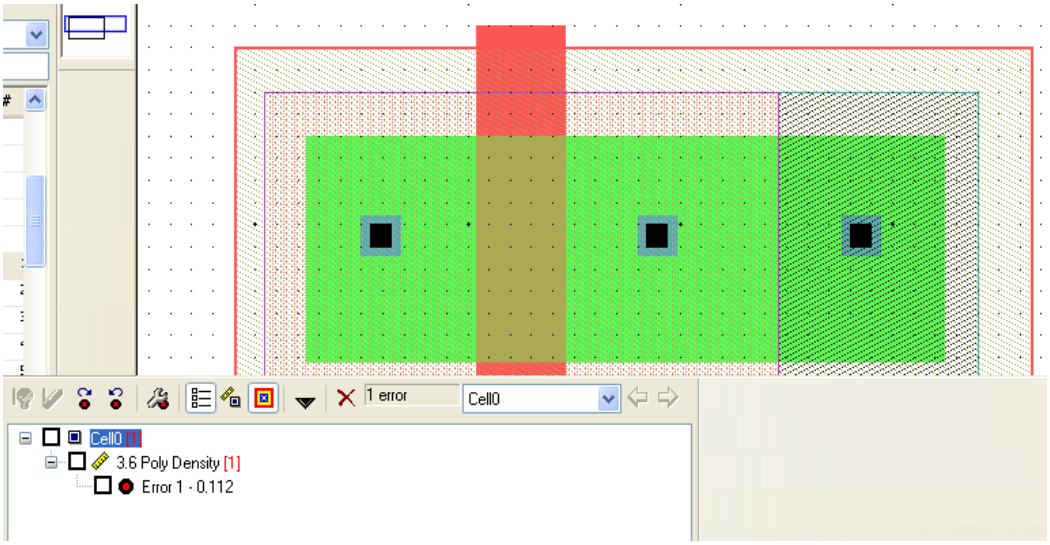
Now we need to put this in N-Well



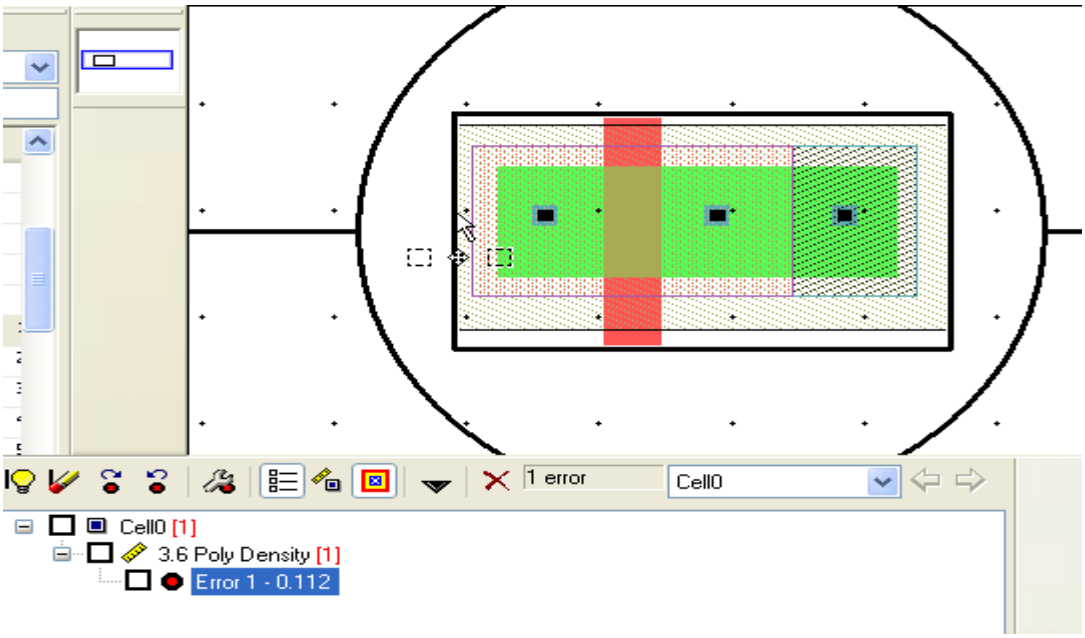
We can perform DRC (Design Rule Check) at every stage



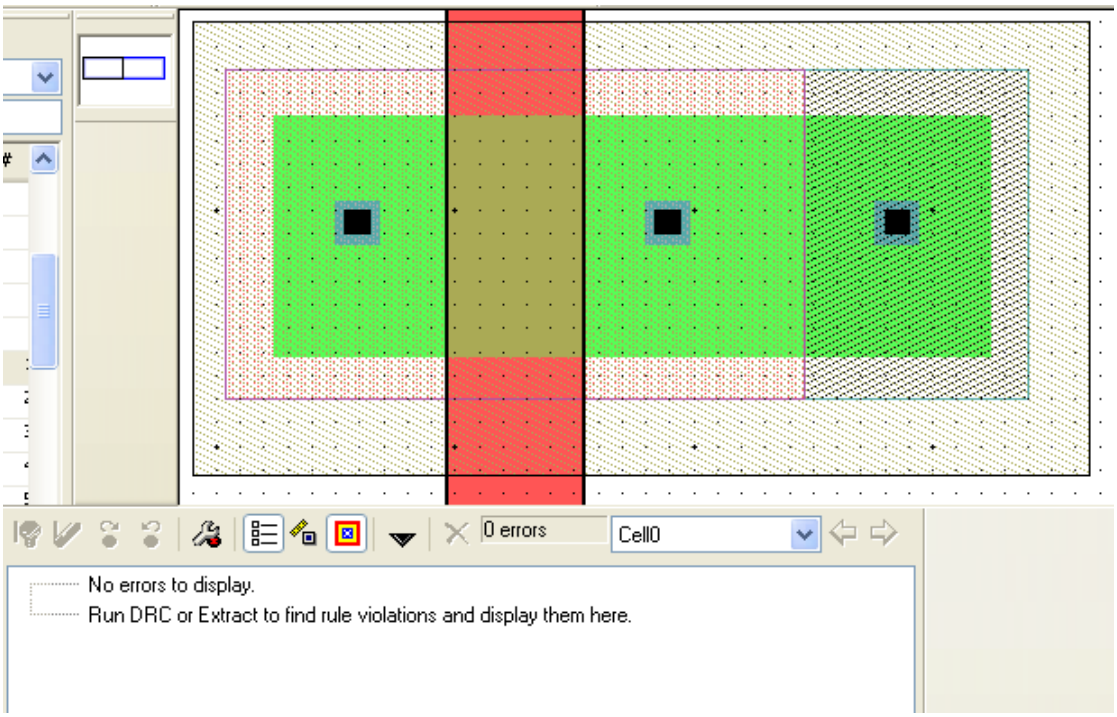
If we are violating any Design rule then it will be shown in Error verificationnavigator



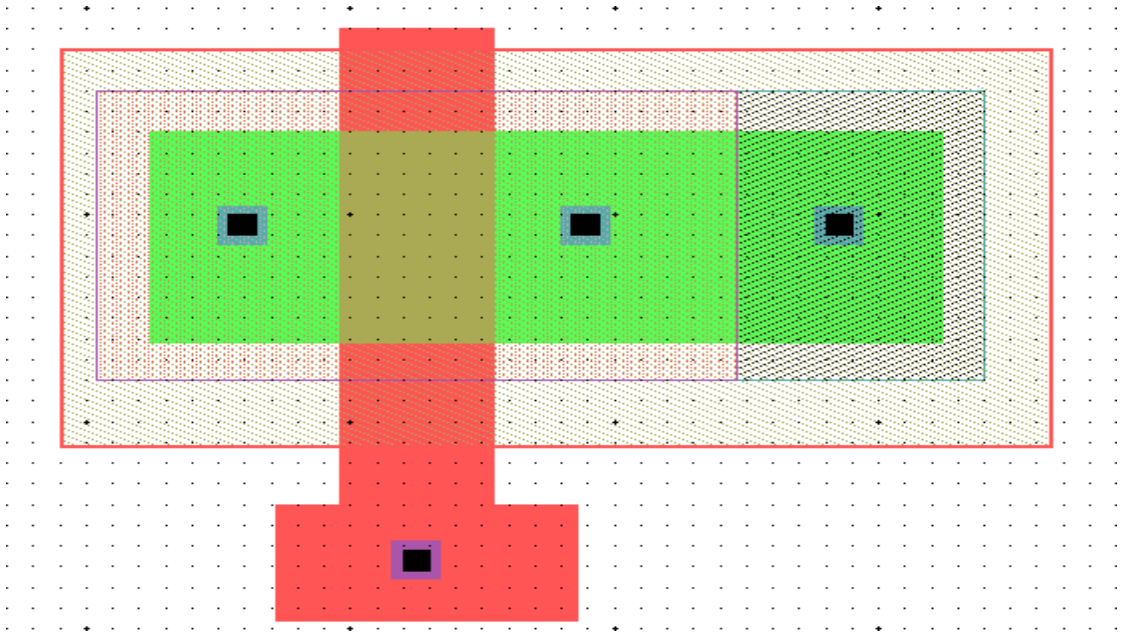
By clicking on the error, the tool points to the error that occur on layout.



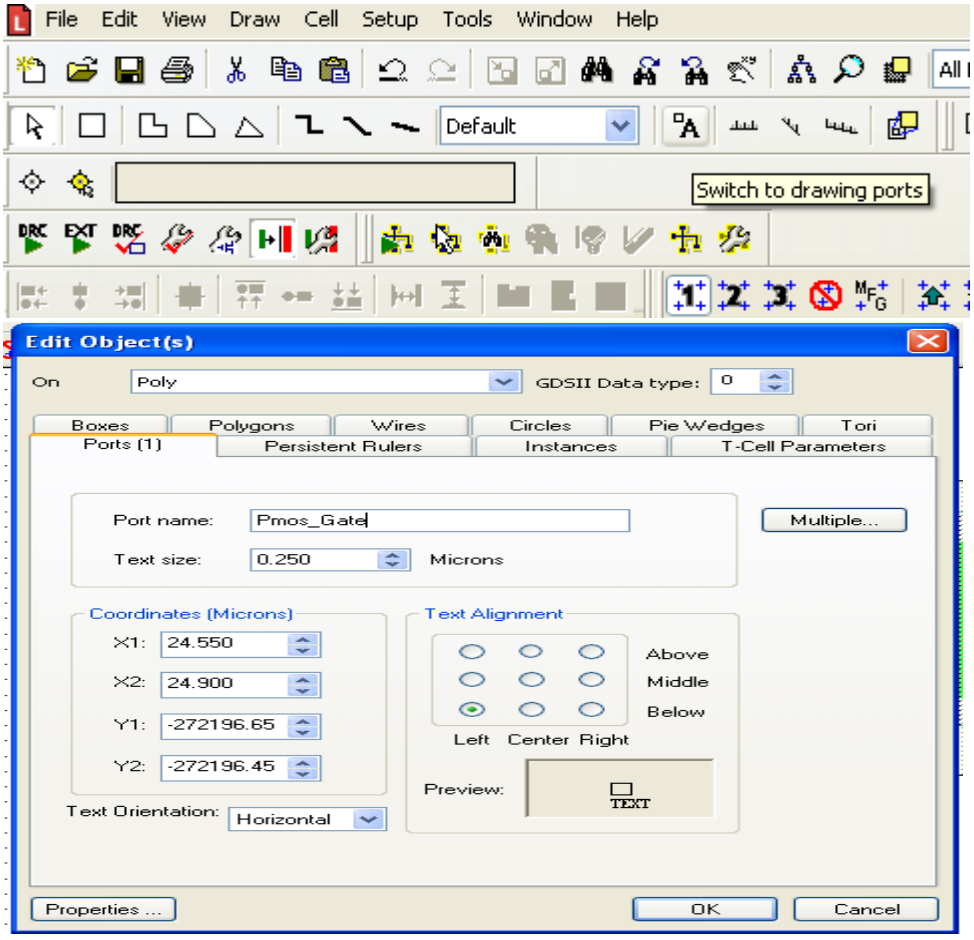
By increasing the poly density area in the layout, we can minimize that error. Andagain, run DRC check.



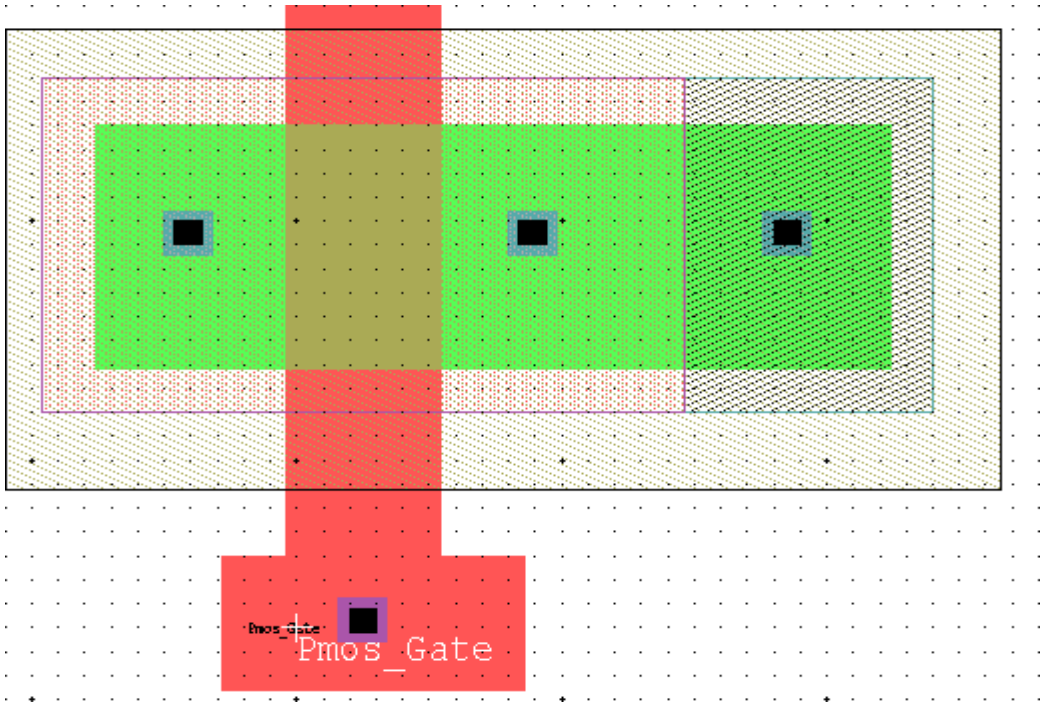
We need to design Gate contact.



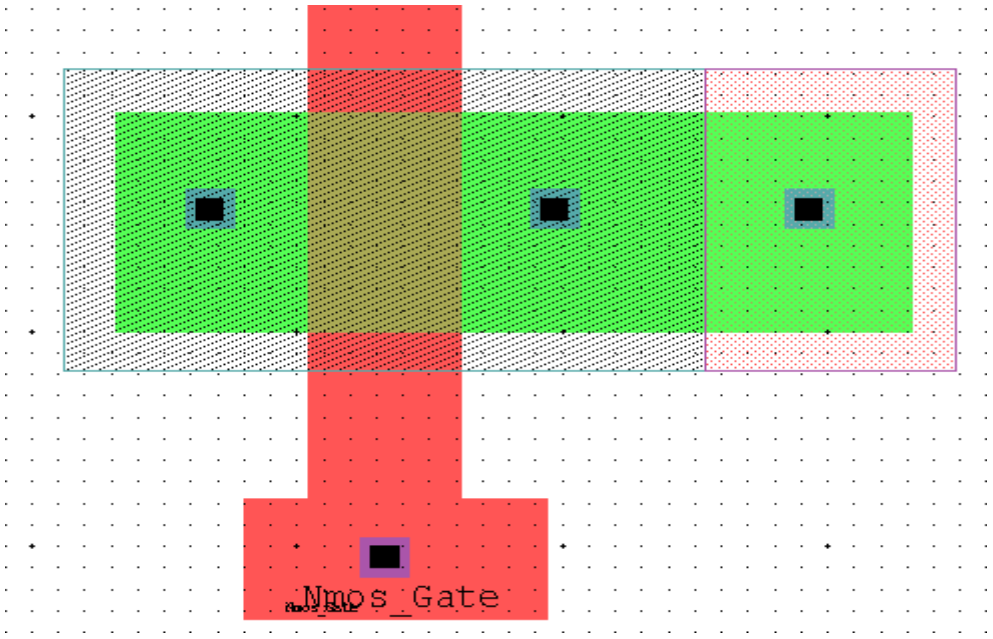
To define port, go to (A)



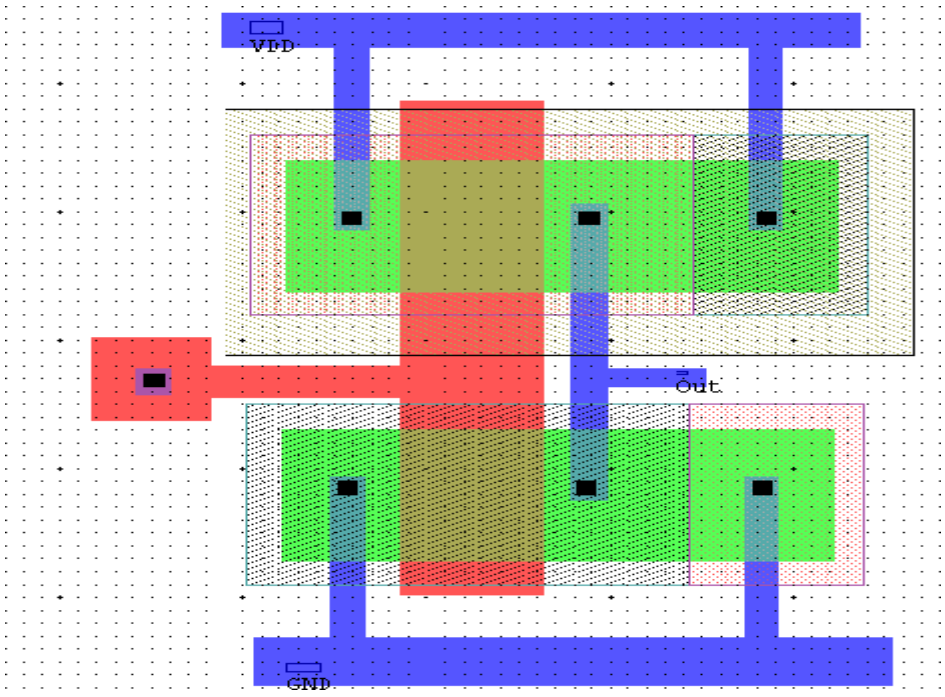
We can now find the port name added to gate.



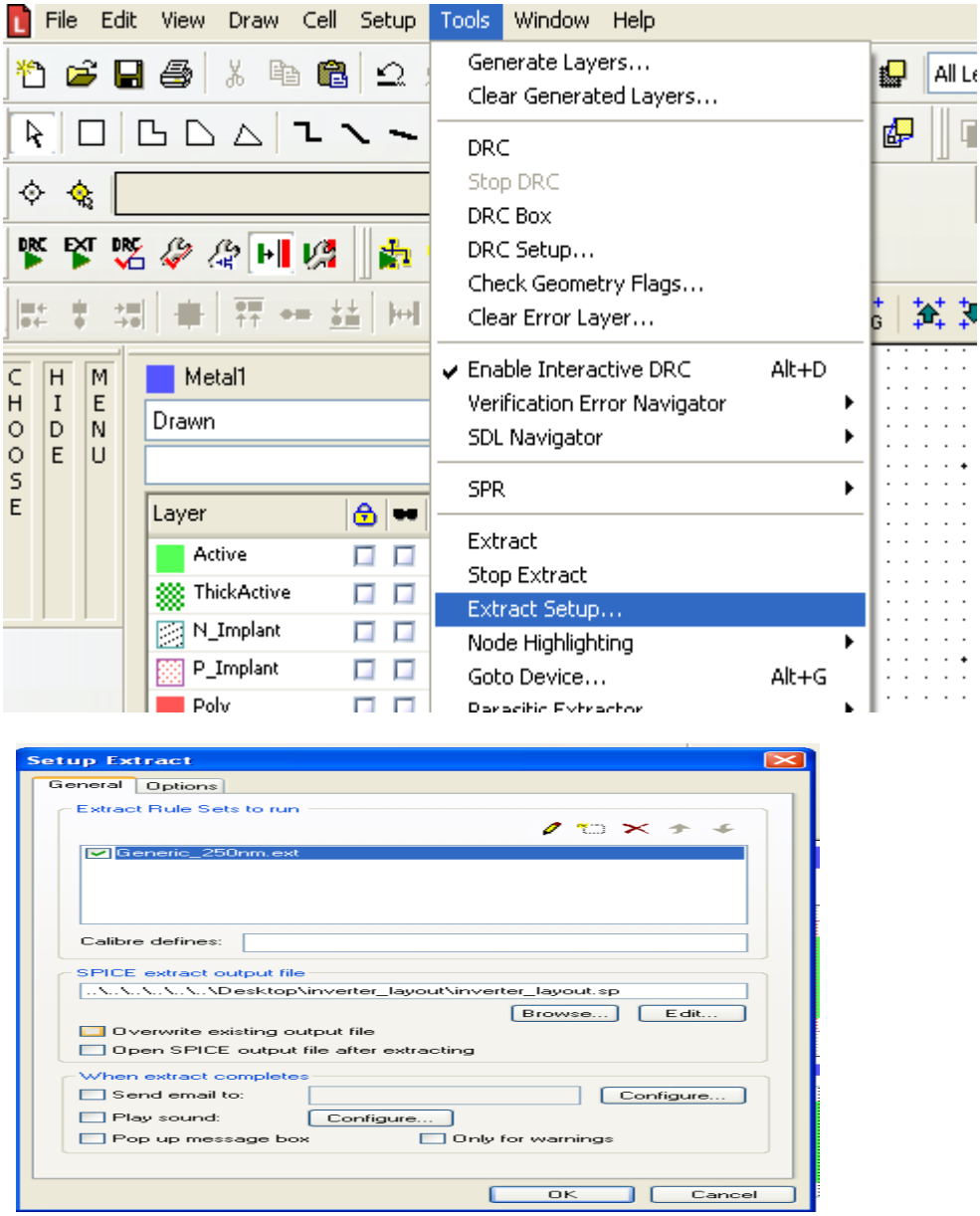
Similarly, we do NMOS layout.



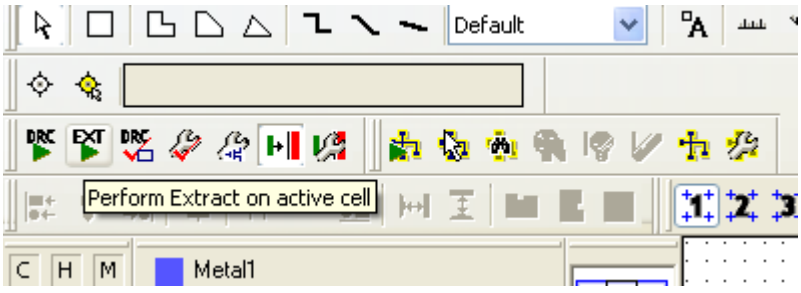
After connecting NMOS and PMOS, CMOS layout looks like as follows.



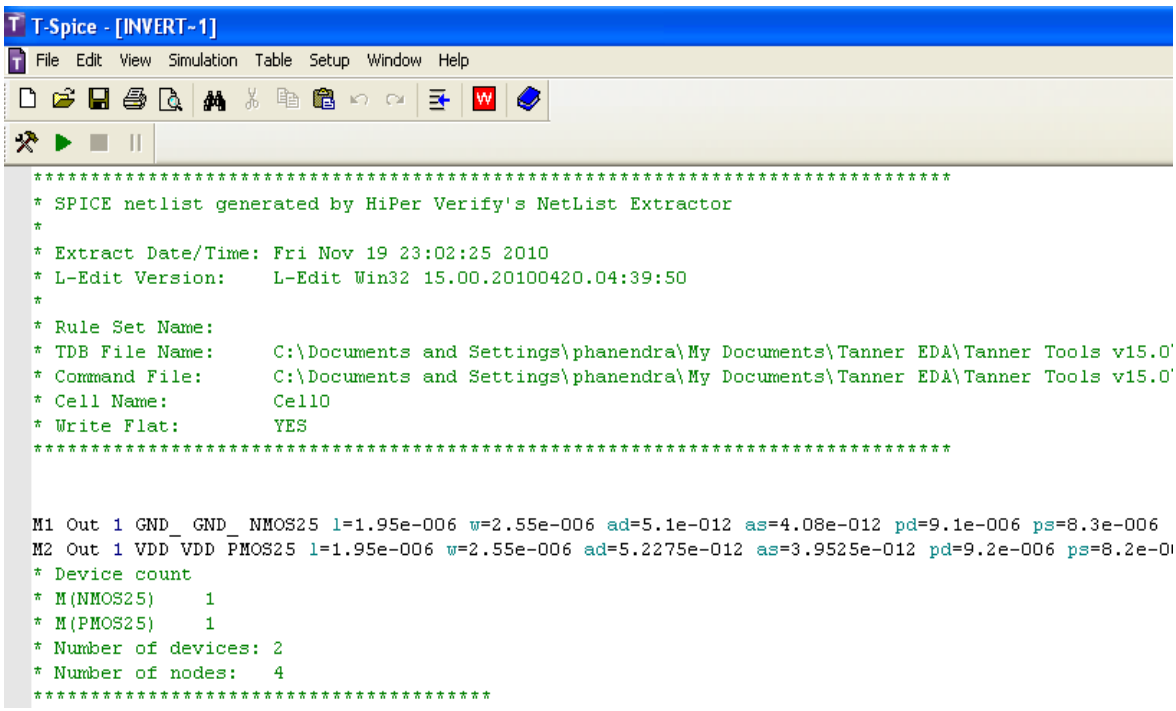
Now we can extract netlist by doing some settings



Click options in Setup Extract above, and uncheck all Hiper Verify Options.



Run Extraction, A spice file will open as follows



This netlist is saved as inverter_layout.spc

VVoltageSource_1 Vdd Gnd DC 5
VVoltageSource_2 vin Gnd PULSE (0 5 0 5n 5n 95n 200n)
.PRINT TRAN V(vin)
.PRINT TRAN V(vout)
. tran 1ns 500ns

Final netlist

.lib "C:\Documents and Settings\phanendra\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT

M1 Vout Vin GND GND_ NMOS25 l=1.95e-006 w=2.55e-006 ad=5.1e-012 as=4.08e-012 pd=9.1e-006 ps=8.3e-006 $(24.65 -272199 26.6 -272197)
M2 Vout Vin VDD VDD PMOS25 l=1.95e-006 w=2.55e-006 ad=5.2275e-012 as=3.9525e-012 pd=9.2e-006 ps=8.2e-006 $(24.65 -272194 26.6 -272192)

VVoltageSource_1 Vdd Gnd DC 5
VVoltageSource_2 Vin Gnd PULSE (0 5 0 5n 5n 95n 200n)

.PRINT TRAN V(Vin)
.PRINT TRAN V(Vout)
. tran 1ns 500ns
. end

INVERT~1

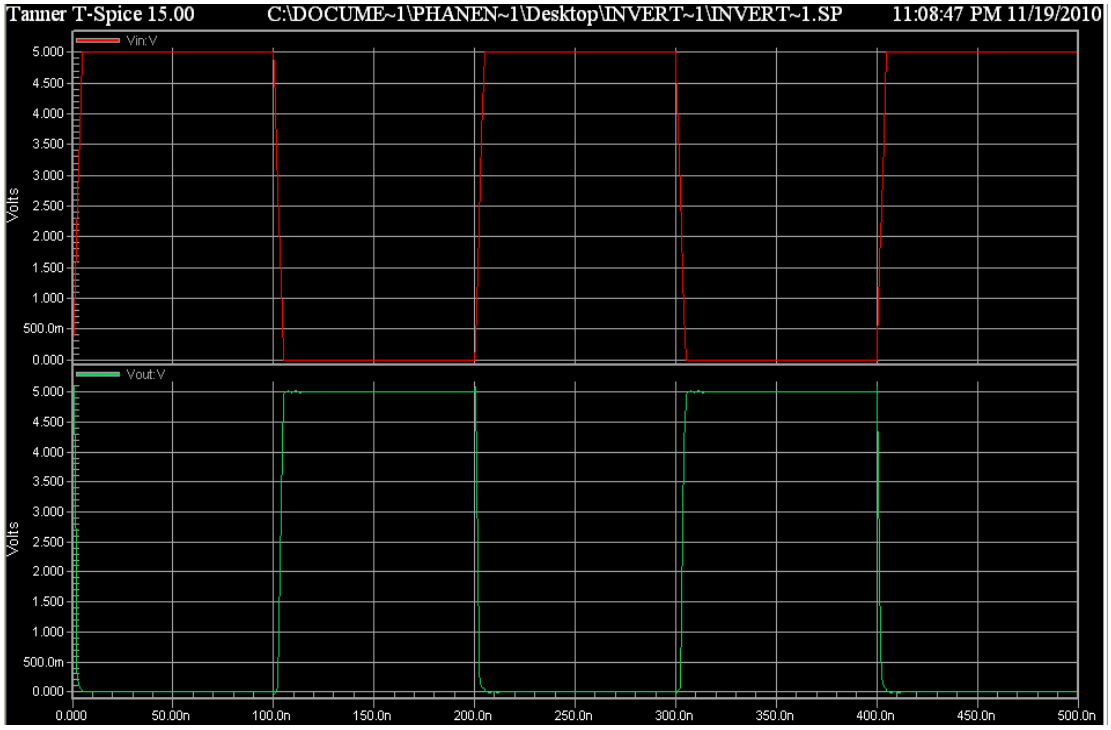
```
********************************************************************************
* SPICE netlist generated by HiPer Verify's NetList Extractor
*
* Extract Date/Time: Fri Nov 19 23:02:25 2010
* L-Edit Version:    L-Edit Win32 15.00.20100420.04:39:50
*
* Rule Set Name:
* TDB File Name:     C:\Documents and Settings\phanendra\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\
* Command File:      C:\Documents and Settings\phanendra\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\
* Cell Name:         Cell0
* Write Flat:        YES
********************************************************************************
.lib "C:\Documents and Settings\phanendra\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\Generic_250nm_T

M1 Vout Vin GND GND_ NMOS25 l=1.95e-006 w=2.55e-006 ad=5.1e-012 as=4.08e-012 pd=9.1e-006 ps=8.3e-006  $(24.65 -272199 26.6
M2 Vout Vin VDD VDD PMOS25 l=1.95e-006 w=2.55e-006 ad=5.2275e-012 as=3.9525e-012 pd=9.2e-006 ps=8.2e-006  $(24.65 -272194


VVoltageSource_1 Vdd Gnd  DC 5
VVoltageSource_2 Vin Gnd  PULSE(0 5 0 5n 5n 95n 200n)
.PRINT TRAN V(Vin)
.PRINT TRAN V(Vout)
.tran 1ns 500ns

.end
```

After saving spice file, we can simulate it, W-Edit will be invoked and we can check the spice:



And the result of the inverter will be shown like this.

Appendix-2

Acceptance Letter:

Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

'A++ Grade'

SCHOOL OF ELECTRICAL & COMMUNICATION
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

INTERNATIONAL CONFERENCE ON
SMART SYSTEM TECHNOLOGIES AND APPLICATIONS (ICSSTA 2023)
APRIL 28th & 29th 2023

Acceptance Letter

Date:07-04-2023

Dear Author(s),

Greetings,

The review and selection process for your article has been completed.

Paper ID:3-2049

Paper Title: A High performance and Low Recoil Noise Three Stage Comparator

Author(s): Sujatha Y, Chaitanya Ram M, Ganesh Sai B, Uma Ch, Rajesh B

Affiliation: Sri Vasavi Engineering College.

Based on the recommendations from the reviewer(s) assigned for your paper, I am pleased to inform you that your paper has been **ACCEPTED with MAJOR REVISION** for the ICSSTA 2023 Conference which to be held at Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Chennai during 28th and 29th April 2023.

The registration for ICSSTA 2023 is already open, hence you are requested to complete the registration process at the earliest. Please note that your paper has been **accepted** for presentation and forwarded for publication in Scopus indexed journals. Please check the registration details for ICSSTA 2023 on the conference website (https://www.veltech.edu.in/icssta/) and proceed with your registration process. The template for camera ready paper and registration form are available on the conference portal.

Reviewer 1:

1. The novelty of the paper is highly motivated.
2. The format and alignment of the paper is good.
3. It would be great, if more recently published papers referred.

Reviewer 2:

1. Paper to be organized.
2. Voltage charge pump justification
3. Justification for proposed circuit design is required.
4. Novelty is not sufficient with only modified three stage comparator.
5. Comparison table results need to be convinced.

Please send the soft copies of all the above documents to icssta@veltech.edu.in after the payment of the registration fee.

Vel Tech
Rangarajan Dr. Sagunthala
R&D Institute of Science and Technology
(Deemed to be University Estd. u/s 3 of UGC Act, 1956)

SCHOOL OF ELECTRICAL & COMMUNICATION
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

INTERNATIONAL CONFERENCE ON
SMART SYSTEM TECHNOLOGIES AND APPLICATIONS (ICSSTA 2023)
APRIL 28th & 29th 2023

Payment and Camera-ready copy submission should be done on or before 10.04.2023.

Please do not hesitate to contact us for further queries (if any). Visit our website for updates on ICSSTA 2023.

We look forward to your participation in ICSSTA 2023. Many thanks for your support to ICSSTA 2023.

With Best Regards,
Convener – ICSSTA 2023