A High performance and Low Recoil Noise Three Stage Comparator

[1]Sujatha Y, [2]Chaitanya Ram M, [3]Ganesh Sai B, [4]Uma Ch, [5]Rajesh B

[1]Sr.Asst.Professor, Dept of ECE, SVEC, Tadepalligudem, India,

[2345]student, Dept of ECE, SVEC, Tadepalligudem, India,

[1] y.sujatha@srivasaviengg.ac.in

***Abstract* — Now a days fast Analog to Digital Converters (ADC) are required to catch up with the speed of this digital world. The main element of this ADC is a Comparator. In this paper a three-stage comparator is designed to increase the efficiency and decrease the recoil noise. Once accompanied by existing comparator, in this design a charge pump is introduced instead of a preamplifier. Here, the charge pump acts as an amplifier. This technique greatly reduces the number of transistors as well as recoil noise and increases the speed of comparator. Compared to the modified three stage comparator, this proposed model occupies less area. For easy comparison, the three-stage comparator, modified three stage comparator and proposed model are designed in same CMOS technology using Tanner EDA Tool.**

Keywords—ADC, CMOS, Comparator, High speed, Recoil noise, Charge pump

I. INTRODUCTION

A comparator is the fundamental building block in analog to digital converter, that compares an input with fixed voltage level and produce an output '1' and '0' based on input level.

As a result, a typical comparator produces digital 0 or digital 1 depending on whether the input voltage and reference voltage are compared. A clocked comparator, on the other hand, only performs evaluation when it is triggered by the rising or lowering edge of the clock. A clocked comparator typically has two stages: the first stage serves to link the input signals, and the second stage is made up of two cross-coupled inverters, each of whose inputs is coupled to an adjacent inverter's output. This is stage is called as Regenerative stage.

II. EXISTING METHOD

A. Two stage comparator

The preamplifier stage and latch stage make up the two primary stages of a two-stage comparator. Comparators are used in several different kinds of analog digital conversations. High-speed, high-resolution Strong ARM latch ADCs' accuracy is constrained by several variables, including the comparator's speed, the magnitude of recoil noise [2], the intensity of input referred noise, and the size of the offset. It's critical to develop a high-performance comparison. Strong ARM architecture is a traditional structure that offers numerous benefits due to the nature of its positive feedback, which has a low stand by power consumption and the greatest comparison with low leakage

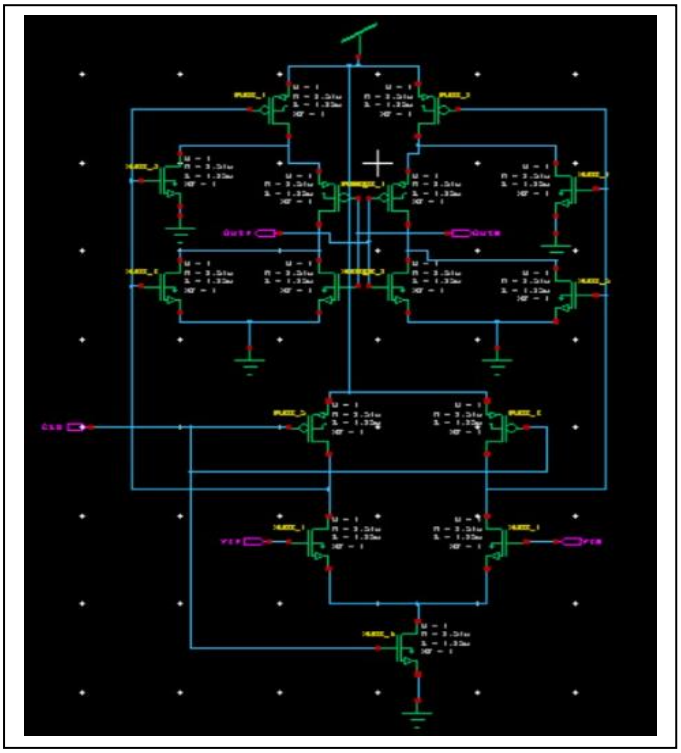

Fig1. Schematic of Two stage comparator

currents. This strong-arm design is employed by a Miyahara's comparator [5]. Because its input mode transistors PMOS1-PMOS2, are biased by the supply voltage VDD/2, than the is biased voltage is nearly twice as high as that of a Strong ARM latch, and as a result, the recovery speed is never controlled by the source current. The supply voltage demand is decreased because the two-stage design uses fewer transistors.

The main disadvantage of this two-stage comparator is we cannot control the regeneration speed due to its biasing of PMOS1-PMOS2 transistors and at low currents the generation of recoil noise occurs. The parasitic capacitances of the transistors are used to link the significant voltage variations on the regeneration nodes to the comparator's input. The input voltage is disrupted because the circuit before it does not have zero output impedance, which could reduce the converter's accuracy [3].

By including an additional oscillator to the two-stage comparator, a three-stage comparator was developed to

address this drawback. At the latch step in this case, we use an NMOS input [1].

B. Comparator with three stages

This comparator consists of three stages they are pre amplification stage, decision making stage and latch stage [1]. The three-stage comparator is evolved to

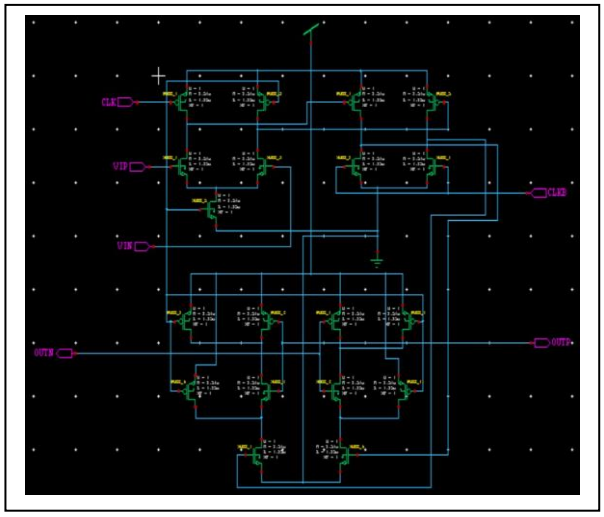

Fig2.Schematic of Three stage comparator

overcome the disadvantage of two stage comparator in order to gain control over regeneration speed [1]. The primary distinction between two stage and three stage comparators is an additional preamplifier. The extra preamplifier can control the regeneration speed due to its invertor functionality and allow latch stage to use NMOS pair.

After first stage amplification, FP and FN are connected to ground, this makes high gate-source voltage for PMOS3-PMOS4 results in pulling RP and RN to VDD. Before going to latch stage, the signal must flow through two stages which results in increasing the delay and the existence of recoil noise due to feedback.

C. Modified Three stage comparator

This novel architecture was developed to improve the three stage comparator's performance. It has an additional preamplifier with a PMOS input pair, which creates an additional path when compared to a conventional three stage comparator[1].

CLK=0 and CLKB=1 during the reset period. The RN1 and the RP1(R means Rising and F means falling) shorted to ground, while FP1 and FN1 are connected to VDD. In this condition NMOS15-NMOS17 transistors will turn off and we can estimate there is no electricity flow in a side route NMOS14-NMOS17.

In the period of amplification, CLK=1 and CLKB=0. In this condition RP1 and RN1 are connected to VDD, FP1 and FN1 are shorted to ground. It occurs simultaneously, before depletion of FP1 and FN1, the RP1 and RN1 are boosted. Thus it can turn on the extra path NMOS14-NMOS17. This can generate differential voltage at OUT-P and OUT-N which in turn help boosting the regeneration.

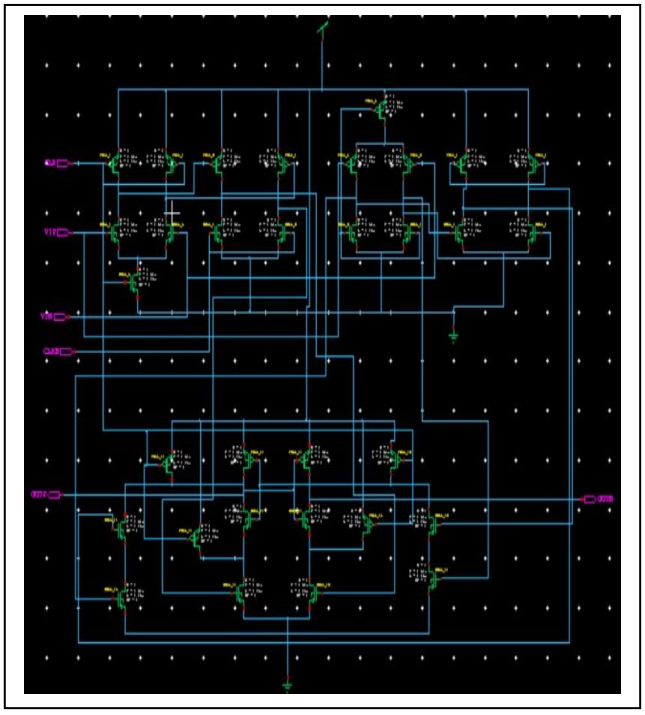

Fig3. Schematic of Modified Three stage comparator

III. PROPOSED METHOD

A. Volatge Charge Pump

A voltage charge pump is a circuit used to get higher voltage values than normal supply voltage. A voltage charge pump is a dc-dc converter, it is constructed by using storage elements and switches. It is used to raise the given voltage or current and used for amplification purposes.

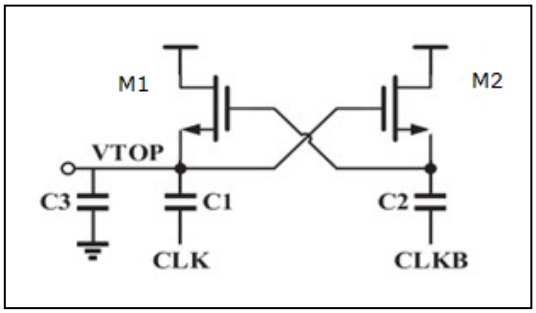

Fig4. Voltage charge pump

Here NMOS transistors can be used as switches and capacitors as storage elements. It consists of mainly two NMOS transistors which are cross coupled to each other and three capacitors [4].

By using this voltage charge pump we can increase the regeneration speed.

If CLK=0, CLKB=1 then C2 will be charged towards Vdd and M1 will turn ON.

If CLK=1, CLKB=0 then C1 will be charged and M2 will turn ON.

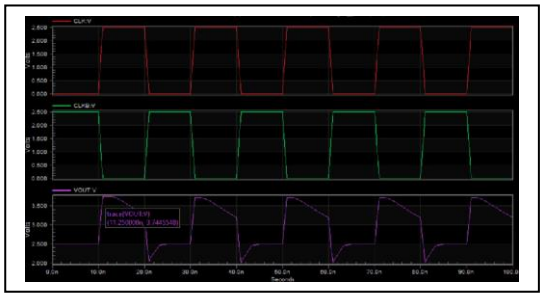

Fig 5. Output waveform of charge pump

B. Three stage comparator with Voltage charge pump

Voltage charge pumps boosts the VDD to some extent, when we use this amplified voltage in latch stage it can increase the speed which would be greater than conventional three stage comparator [4].

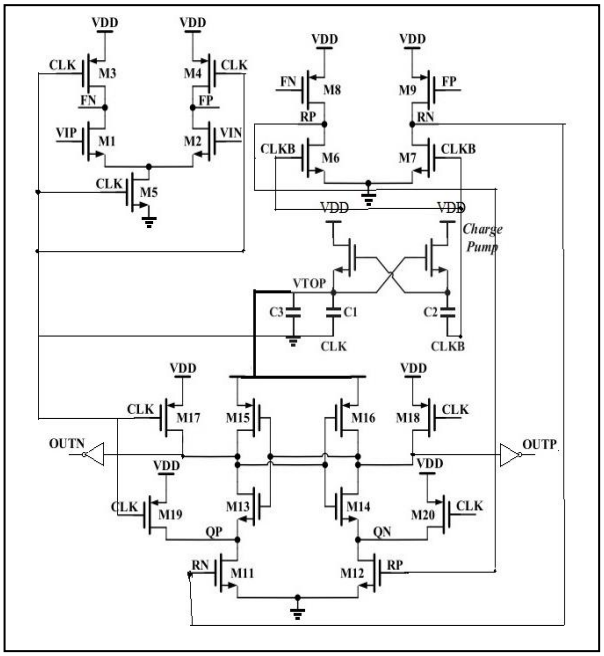

Fig6. Three stage comparator with voltage charge pump

CLK=0 and CLK=1. The nodes FP and FN are connected to VDD meanwhile the nodes RP and RN to ground. In amplification phase CLK=1 and CLKB=0. In this phase FP & FN fall to ground. The output of voltage charge pump VOUT is connected to the sources of PMOS transistors in latch stage instead of VDD i.e., M15-M16. Thus, this pumped charge can increase the speed of latch stage. Therefore, we can get quick response than conventional three stage. Actually, pumping the voltage is VDD for M15-M16 in conventional model, but pumping of voltage higher than VDD can make the circuit faster than previous one. So the proposed model's latch stage is driven by the output voltage of charge pump. To reduce the recoil noise, two inverters are added at the output nodes OUTP and OUTN. By using inverters, we can reduce recoil noise.

When CLK=0, the output of voltage charge pump is VDD and when CLK=1, the VTOP becomes nearly 1.3VDD and settles at 1.1VDD i.e.,2.8V.

IV. RESULTS

For better understanding the three models discussed here are implemented in 130nm technology. And the results of the proposed model and the comparisons are mentioned below.

A. Three stage comparator with Voltage charge pump

Transient Analysis

The output of the comparator will pass on to the output nodes whenever the CLK is high.

If VIP=VIN=0, then no output will pass through the output nodes.

If VIP > VIN, then the output will pass through the node OUTP.

If VIN > VIP, then the output will pass through the node OUTN.

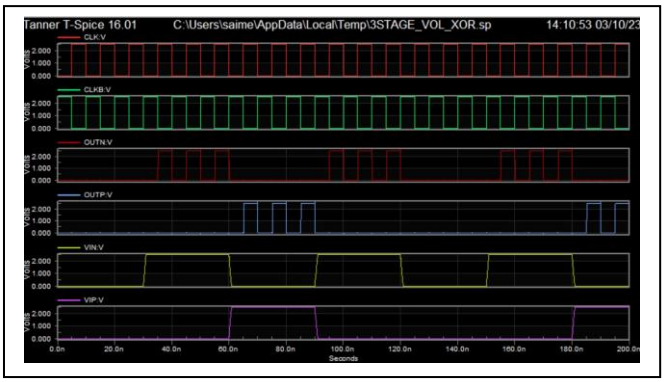

Fig7. Transient analysis of Three stage comparator with Voltage charge pump

B. Comparison table between various comparators

Below table represents the properties and performance of different types of comparators discussed above.

	DELAY (ns)	**POWER CONSUMPTION (µW)**	**NO. OF TRANSISTORS**
COMPARATOR OF THREE SATGES	143.76	33.9	19
MODIFIED THREE STAGE COMPARATOR	111.65	96.2	32
THREE STAGE COMPARATOR WITH VOLTAGE CHARGE PUMP	100.96	6.87	25

The Three Stage Comparator with Voltage Charge Pump is designed with 22% less number of transistors than the modified three-stage comparator and it consumes power less than conventional three stage comparator due to absence of extra path indulged by the PMOS input pairs. And the delay is reduced by 11%, the three stage with voltage charge pump is faster than the other models.

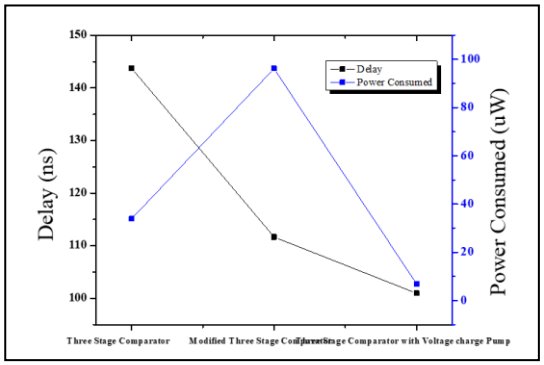

Fig7. Graphical representation of the Parameters

V. CONCLUSION

Therefore, this three-stage comparator and its voltage charge pump, which has the benefits of quick speed, little recoil noise and little input referred offset. This type of comparator works well with SAR ADCs that require high speed and great resolution. Last but not least, quantified outcomes confirm the viability of these comparators.

REFERENCES

[1] Haoyu Zhuang , Wenzhen Cao, Xizhu Peng , and He Tang," A Three-Stage Comparator and Its Modified Version With Fast Speed and Low Kickback," IEEE transactions on very large scale integration (vlsi) systems, vol. 29, no. 7, july 2021

[2] P. Harpe, E. Cantatore, and A. van Roermund, "A 2.2/2.7fJ/conversionstep 10/12b 40kS/s SAR ADC with data-driven noise reduction," in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2013, pp. 270–271.

[3] N Bala Dastagiri1 and K Hari Kishore, "Design of Dynamic Latched Comparator with Reduced Kickback Noise," Volume 118 No. 17 2018, 289-298

[4] H. Zhuang, H. Tang, and X. Liu, "Voltage comparator with 60% faster speed by using charge pump," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 2923–2927, Dec. 2020.

[5] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise selfcalibrating dynamic comparator for high-speed ADCs," in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2008, pp. 269–272.

[6] A. Khorami and M. Sharifkhani, "A low-power high-speed comparator for precise applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 26, no. 10, pp. 2038–2049, Oct. 2018