A Three-Stage Comparator and Its Modified Version With Fast Speed and Low Kickback

Haoyu Zhuang, Wenzhen Cao, Xizhu Peng, and He Tang

***Abstract*— This brief presents a three-stage comparator and its modified version to improve the speed and reduce the kickback noise. Compared to the traditional two-stage comparators, the three-stage comparator in this work has an extra amplification stage, which enlarges the voltage gain and increases the speed. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. This greatly reduces the kickback noise by canceling out the nMOS kickback through the pMOS kickback. It also adds an extra signal path in the regeneration stage, which helps increase the speed further. For easy comparison, both the conventional two-stage and the proposed three-stage comparators are implemented in the same 130-nm CMOS process. Measured results show that the modified version of three-stage comparator improves the speed by 32%, and decreases the kickback noise by ten times. This improvement is not at the cost of increased input referred offset or noise.**

***Index Terms*— Comparator, high speed, low kickback.**

I. Introduction

As a key building block, the comparator plays an important role in various types of analog-to-digital converters (ADCs) [1], [2]. Especially, in high-speed high-resolution SAR ADCs, the ADC sampling rate and accuracy are limited by the comparator speed, kickback noise, input referred noise, and offset. Under this circumstance, it is important to design a high-performance comparator.

There are many comparator structures reported in recent years. The StrongARM latch in [3] and [4] is a classic structure. It has several advantages: no static power, rail-to-rail outputs, and fast comparison due to the positive feedback [4]. Nevertheless, it also has several limitations. First, its regeneration speed is limited by the small current source under the latch. Here, the current source is the input pair transistors. Because the input pair has a common-mode input of $V_{DD}/2$, the current in the current source is limited, which limits the regeneration speed. Second, due to the several stacked transistors, a large power supply voltage is needed.

Two-stage comparators do not have these issues [5]–[11]. Take the Miyahara's two-stage comparator in [9] as an example (see Fig. 1). Its regeneration speed is no longer limited by the small current source. This is because its latch input pair M6–M7 have a gate–source voltage of V_{DD}, which is two times larger than the $V_{DD}/2$ of the StrongARM latch. Another advantage is that the number of stacked transistors is reduced. This relaxes the requirement on the power supply voltage.

Manuscript received November 20, 2020; revised April 1, 2021; accepted May 1, 2021. Date of publication May 18, 2021; date of current version June 29, 2021. This work was supported in part by the NSFC under Grant 62004023, in part by the Department of Science and Technology of Sichuan Province under Grant 2018GZDZX0003 and 2020YFG0285, and in part by the National Key Research and Development Program of China under Grant 2018YFB2100100. *(Corresponding author: He Tang.)*

The authors are with the School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China (e-mail: tanghe@uestc.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TVLSI.2021.3077624.

Digital Object Identifier 10.1109/TVLSI.2021.3077624

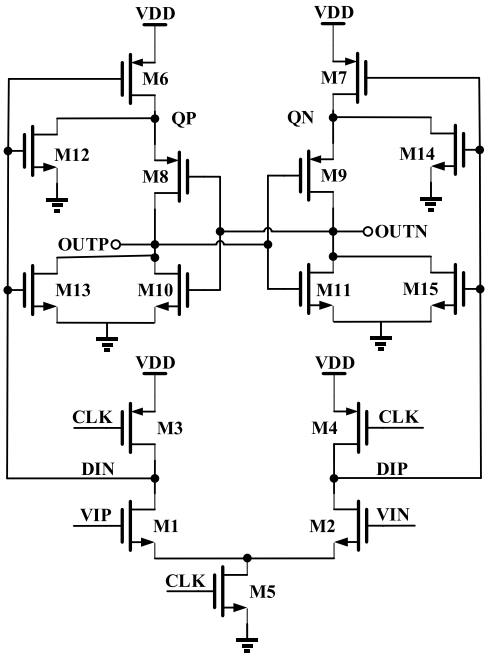

Fig. 1. Miyahara's two-stage comparator in [9].

Although the Miyahara's two-stage comparator increases the speed, its speed can be further improved in the following way. As can be seen in Fig. 1, its latch input pair M6–7 are pMOS transistors, and the pMOS hole mobility is small (2–3 times smaller than the nMOS electron mobility), limiting the regeneration speed. Thus, our goal is to use nMOS transistors instead for the latch input pair, so that the regeneration speed could be greatly improved. Meanwhile, we must maintain the nMOS transistors for the preamplifier input pair.

To this end, this brief presents a three-stage comparator. By adding an extra preamplifier stage, the nMOS input pairs can be used for both the latch-stage and the first-stage preamplifier, thus improving the regeneration speed. Besides, these input pairs work in the saturation region at the beginning of comparison, thus ensuring a small input referred noise. The extra stage of preamplifier also provides voltage gain, which helps further increase the regeneration speed and suppress the input referred offset and noise. Compared to the prior three-stage comparator of [12], the three-stage comparator in this work has a faster speed and a lower input referred noise.

This brief also proposes a modified version of three-stage comparator. By using a CMOS input pair at the first-stage preamplifier, the kickback noise is greatly reduced. An extra path is also added in the latch stage to further increase the regeneration speed and suppress the input referred offset and noise. Implemented in the same 130-nm process, the three-stage comparator in this work increases the speed by 25% compared to the conventional two-stage comparators, while the proposed modified version improves the speed by 32% and decreases the kickback noise by ten times.

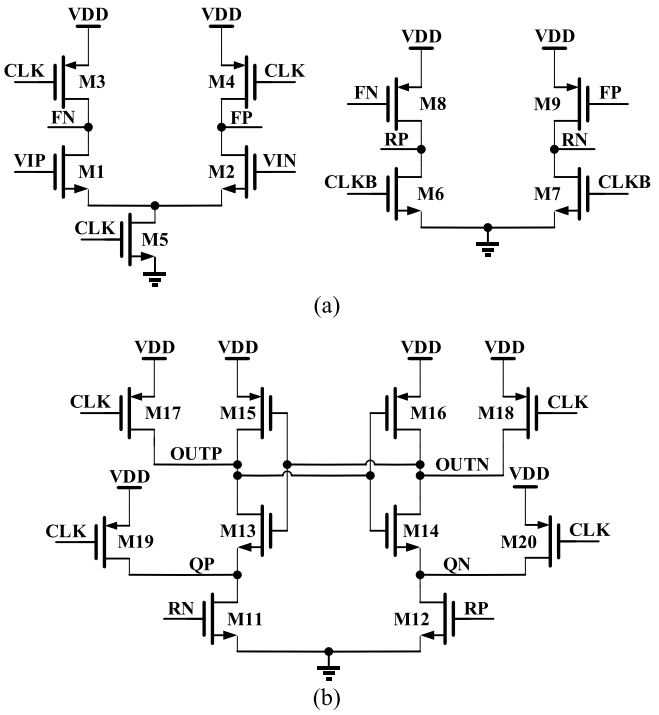

Fig. 2. Three-stage comparator in this work. (a) First two stages (preamplifiers). (b) Third stage (latch stage).

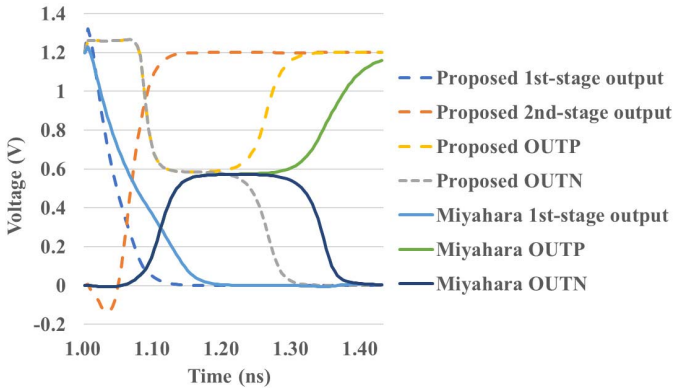

Fig. 3. Transient simulated waveforms of the Miyahara's comparator and the three-stage comparator.

This improvement is not at the cost of increased input referred offset or noise.

This brief is organized as follows. Section II discusses the three-stage comparator. Section III analyzes the modified version of three-stage comparator. Section IV shows the simulated and measured results. Section V concludes the brief.

II. Three-Stage Comparator

A. Review of Two-Stage Comparator

Fig. 1 shows the Miyahara's two-stage comparator. There are three phases of operation, namely the reset phase, the amplification phase, and the regeneration phase. In the reset phase (CLK = 0), the comparator is reset. In the amplification phase (CLK = 1), the input signal VIP–VIN is amplified and sent to the latch stage. In the regeneration phase, OUTP and OUTN regenerate to V_{DD} or GND. As mentioned before, such a structure has the limitation of pMOS input pair in the latch stage.

B. Three-Stage Comparator

Fig. 2 shows the three-stage comparator in this work. The three stages are connected one after another. Compared with the Miyahara's comparator, the major difference is that one extra preamplifier (the second stage) is added. This extra preamplifier acts as an inverter, and makes the latch stage able to use nMOS input pair M11–12 instead of pMOS input pair, which leads to increased speed. The extra preamplifier also provides voltage gain, thus improving the regeneration speed and suppressing the input referred offset and noise.

Although the extra preamplifier helps increase the speed, this extra stage itself incurs extra delay, because the amplified signal has to go through two stages, rather than one stage, before arriving at the latch stage. Thus, it is necessary to discuss whether this extra delay overwhelms the benefit it brings about. As can be seen in Fig. 2, after the first-stage amplification, its outputs FP and FN fall to GND. This makes the second-stage input pair M8–9 have a large gate–source voltage equal to V_{DD}. As a result, the current on M8–9 is large enough for quickly pulling up RP and RN. This means that the extra delay incurred by the second stage is small (about 20 ps in post-layout simulation) compared to the large delay of the latch stage (about 200 ps in post-layout simulation). This makes sense because the second stage is actually a dynamic inverter which does not incur much delay. Furthermore, compared to the first-stage output load in the Miyahara's comparator (M6–7 and M12–15 in Fig. 1), the first-stage output load in the three-stage comparator is only M8–9 in Fig. 2. The output load is reduced by several times, improving the amplification speed.

Fig. 3 shows the transient simulation comparison between the Miyahara's comparator and the three-stage comparator. As can be seen, the first-stage output of the three-stage comparator settles faster than the Miyahara's first-stage output by 60 ps, due to the decreased output load. Even if the extra delay of the second stage is taken into account, the second-stage output of the three-stage comparator still settles faster than the Miyahara's first-stage output by 40 ps, considering 90% settling. Furthermore, the regeneration time of the latch stage is also reduced by 76 ps due to the nMOS input pair.

Compared to the three-stage comparator in [12], the three-stage comparator in this work also has several advantages. First, the gate of M6–7 in Fig. 2 is connected to CLKB, rather than to the first-stage output. This reduces the parasitic capacitance at the first-stage output. Second, the gate of M17–20 is connected to CLK, rather than to the second-stage output. This reduces the parasitic capacitance at the second-stage output. Third, the clocked cascode nMOS on top of M1–2 is deleted. This reduces the parasitic capacitance in the first stage. More importantly, it helps ensure that the drain of M1–2 is at V_{DD} at the beginning of comparison. This is important, because the saturation region of input pair helps reduce the input referred noise. Overall, post-layout simulated results show that the input referred noise is reduced by 15% due to the guaranteed saturation region of input pair, and the speed is increased by 6% due to the less parasitic capacitances.

III. Proposed Modified Version of Three-Stage Comparator

A. Circuit Structure

In order to reduce the kickback noise and further improve the speed, this brief proposes a modified version of three-stage comparator, as shown in Fig. 4. Compared to the original version in the previous section, the only difference is that the modified version has the extra first two stages of Fig. 4(b) and extra paths M29–32 in the latch stage of Fig. 4(c). The extra first two stages use pMOS input pair

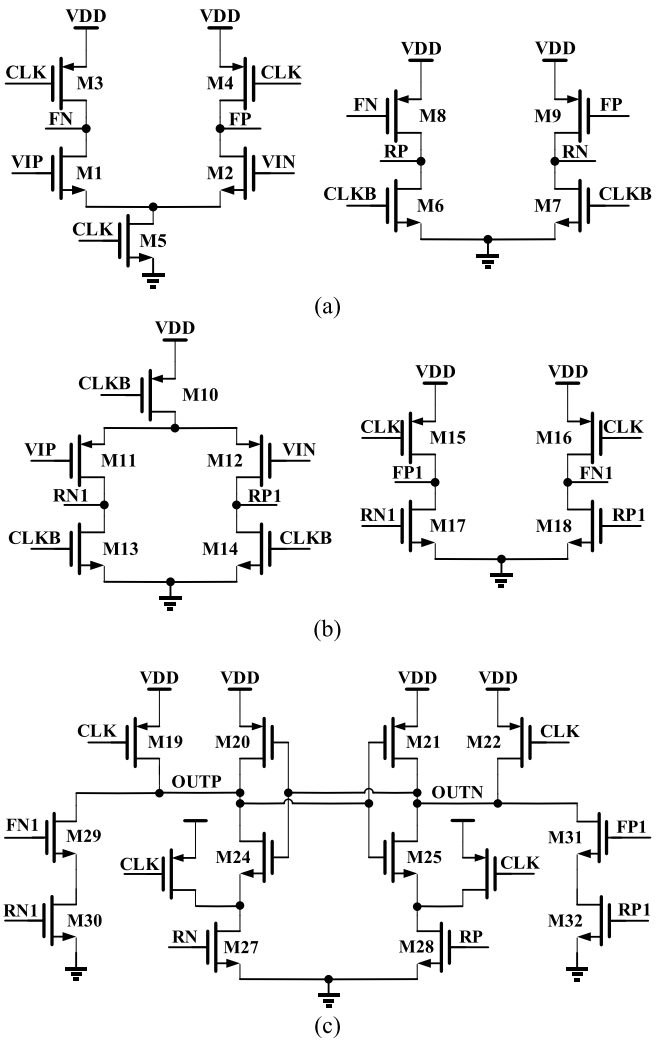

Fig. 4. Proposed modified version of three-stage comparator. (a) Original first two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

M11–12 to cancel out the nMOS input pair M1–2 kickback noise. Besides, the extra paths M29–32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further, and the input referred offset and noise are suppressed further.

The operation of these extra circuits is as follows. In the reset phase, CLK is 0 and CLKB is 1. The RP1 and RN1 in Fig. 4(b) are reset to GND, while FP1 and FN1 are reset to V_{DD}. This turns off M30 and M32 in Fig. 4(c), ensuring that there is no static current in the extra path M29–32.

In the amplification phase, CLK rises to 1 and CLKB falls to 0. RP1 and RN1 in Fig. 4(b) rise to V_{DD} (R stands for rise). Then, FP1 and FN1 fall to GND (F stands for fall). Because the rising of RP1 and RN1 occurs before the falling of FP1 and FN1, the extra paths in Fig. 4(c) are turned on for a limited time, drawing a differential current from the latching nodes OUTP and OUTN. This generates a differential voltage at OUTP and OUTN, which helps speedup the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths in Fig. 4(c) are turned off again to prevent the static current.

Overall, the modified version of three-stage comparator has the advantages of faster speed, lower input referred offset and noise, and lower kickback noise. It is suitable for high-speed high-resolution SAR ADCs.

TABLE I

COMPARATOR DELAY VERSUS INPUT VOLTAGE UNDER DIFFERENT CORNERS ($V_{\mathrm{cm}} = 600$ mV)

tt corner				
Input	**Miyahara**	**Elzakker**	**Three-Stage**	**Modified Version**
10 mV	219.93 ps	215.61 ps	170.98 ps	151.85 ps
1 mV	266.37 ps	277.25 ps	213.97 ps	189.52 ps
ff corner				
Input	**Miyahara**	**Elzakker**	**Three-Stage**	**Modified Version**
10 mV	166.36 ps	168.14 ps	137.21 ps	116.18 ps
1 mV	207.10 ps	226.06 ps	180.47 ps	153.46 ps
ss corner				
Input	**Miyahara**	**Elzakker**	**Three-Stage**	**Modified Version**
10 mV	306.60 ps	306.18 ps	229.85 ps	193.80 ps
1 mV	373.41 ps	383.27 ps	264.51 ps	225.31 ps

As an example, the proposed modified version is suitable for the time-interleaved noise-shaping SAR ADC in [13]. As pointed out in [13], its ADC speed is limited by the comparator speed, and its ADC resolution is limited by the comparator kickback noise. Although Zhuang *et al.* [13] use a channel isolation to reduce the influence of kickback noise, this isolation increases the complexity of system. By contrast, the proposed modified version of three-stage comparator can solve these issues. It has the fastest speed and the smallest kickback noise compared to other comparators, as will be validated later in Section IV.

B. Design Consideration

According to [14], the comparator input referred noise is inversely proportional to the integration time as well as the input pair transconductance. Due to the application of high-speed high-resolution ADCs, the comparator integration time should be reduced as much as possible. Meanwhile, to keep a low input referred noise, the input pair transconductance of each stage should be increased as much as possible (including the input pair of each preamplifier as well as the latch stage). To this end, we use large input pair sizes for each stage in this work (W/L is approximately 3 μm/0.13 μm).

IV. SIMULATED AND MEASURED RESULTS

A. Post-Layout Simulated Results

This section compares the three-stage comparators of this work with the two-stage comparators of Miyahara's comparator [9] (Fig. 1) and Elzakker's comparator [11]. For fair comparison, all comparators are post-layout simulated under the same 130-nm process. All comparators are also designed with the same input referred noise of 440 μV, so that other specifications can be compared.

Table I shows the delay at 90% settling. The common-mode input V_{cm} is set to 0.6 V. As can be seen, the delay of three-stage comparators is smaller than the two-stage comparators by 15%–25% under all conditions. Meanwhile, the delay of modified version is smaller than the original version by 10%–18%.

Fig. 5 shows the circuit to evaluate the kickback noise [15], where R_{TH} is 4 kΩ, the differential input V_{id} is 10 mV, and the common-mode input V_{cm} is 600 mV. Simulated results show

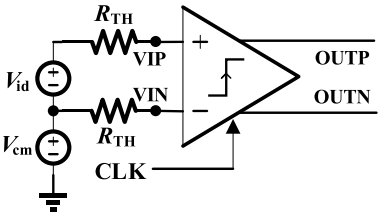

Fig. 5. Circuit for evaluating the kickback noise.

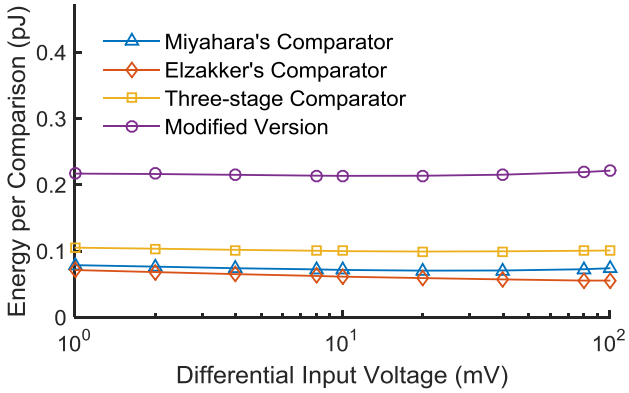

Fig. 6. Power consumption versus differential input voltage.

that the kickback noise are 186.34, 209.61, 223.65, and 19.78 mV, respectively, for the four comparators (Miyahara, Elzakker, Three-Stage, and Modified Version). The modified version reduces the kickback noise by about ten times.

To evaluate the input referred offset, Monte-Carlo simulation is performed with 400 samples. It shows that the standard deviation of input referred offset is 14.04, 13.36, 10.74, and 9.68 mV, respectively, for the four comparators. Compared to the two-stage comparators (Miyahara and Elzakker), the three-stage comparator reduces the offset by 24% and 20%, respectively, while the modified version reduces the offset by 31% and 27%, respectively. This improvement comes from the extra preamplifier with extra gain to suppress the offset.

Fig. 6 shows the power consumption versus the differential input voltage. As can be seen, the three-stage comparators consume more energy than the two-stage comparators, due to the extra circuits and the increased complexity.

Despite the larger power consumption, the three-stage comparators have key advantages over the two-stage comparators. For example, the two-stage comparators cannot have a faster speed than the three-stage comparators, even if their power consumption is increased. This is due to the limitation in speed and power tradeoff. The larger power consumption means larger transistor sizes, and leads to larger parasitic capacitances. This means that the speed can hardly be further increased, even with a larger power consumption. By contrast, the three-stage comparators effectively increase the speed through larger power consumption. This is the advantage of the three-stage comparators.

Overall, the key highlight of the three-stage comparators is the increased speed and the reduced kickback. And this is not at the cost of increased input referred offset or noise.

B. Measured Results

All the four comparators are fabricated in the same 130-nm process. Fig. 7 shows the die photographs of the three-stage comparators. We do not show the die photographs of the two-stage comparators, because the space of brief is limited.

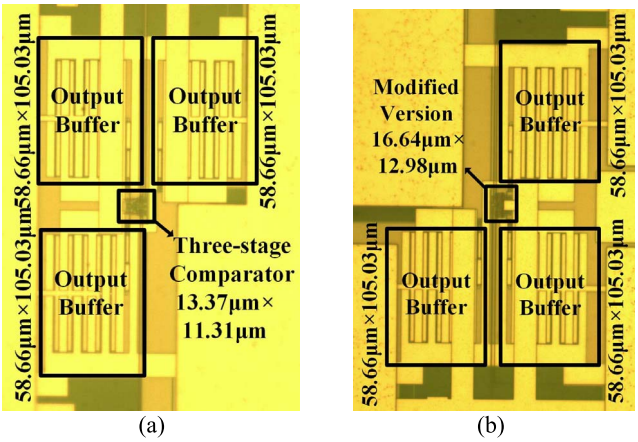

Fig. 7. Die photographs of (a) three-stage comparator and (b) modified version of three-stage comparator.

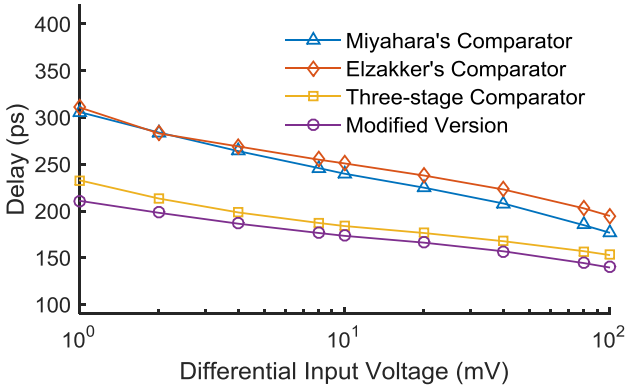

Fig. 8. Measured delay versus differential input voltage.

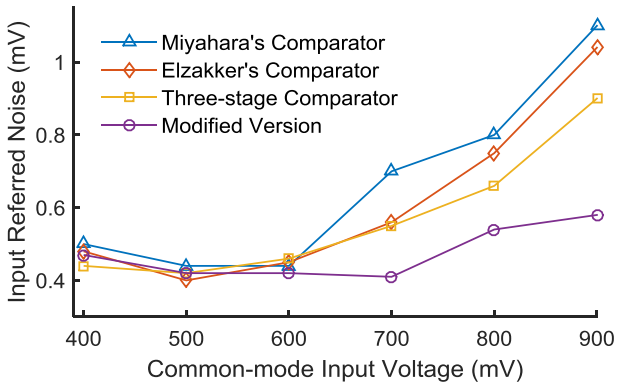

Fig. 9. Measured input referred noise versus common-mode input voltage.

Fig. 8 shows the measured delay. For each comparator, 22 chips are measured and a mean value is calculated. As can be seen, compared to the two-stage comparators, the three-stage comparator reduces the delay by about 25%, and the modified version reduces the delay by about 32%. This matches with the post-layout simulated results.

Fig. 9 shows the input referred noise versus the common-mode input voltage V_{cm}. The input referred noise is designed to 0.44 mV at $V_{cm} = 600$ mV. But the measured input referred noise increases with V_{cm}, when $V_{cm} > 600$ mV. The three-stage comparators also

TABLE II
COMPARISON WITH STATE-OF-THE-ART WORKS

	[2]*	[5]	[6]	Miyahara*	Elzakker*	Three-stage*	Modified Version*
Technology (nm)	65	180	180	130			
Supply Voltage (V)	1.2	1.2	1.8	1.2			
Area (μm^2)	125	392	490	79	117	151	216
Low Kickback Noise	No	No	No	No	No	No	Yes
Input Referred Offset (mV)	—	7.8	2	15	17	13	11
Energy per comparison (pJ)	0.034	0.658	0.40	0.109	0.111	0.137	0.215
Input Referred Noise (mV)	0.4	—	—	0.44	0.45	0.46	0.42
Delay	1240 ps @ V_{cm}=0.6 V, V_{id}=1 mV	550 ps @ V_{cm}=0.6 V, V_{id}=1 mV	301 ps @ V_{cm}=0.9 V, V_{id}=1 mV	306 ps @ V_{cm}=0.6 V, V_{id}=1 mV	311 ps @ V_{cm}=0.6 V, V_{id}=1 mV	233 ps @ V_{cm}=0.6 V, V_{id}=1 mV	211 ps @ V_{cm}=0.6 V, V_{id}=1 mV

* Measured results.

have a smaller input referred noise than the two-stage comparators, due to the larger voltage gain.

Table II compares this work with the state-of-the-art works. As can be seen, the three-stage comparator and its modified version have the smallest delay. The modified version has the smallest kickback noise as well. The power consumption and area are also smaller than [5], [6], regardless of the increased circuit complexity.

V. CONCLUSION

This brief presents a three-stage comparator and its modified version, which have the advantages of fast speed, low kickback noise, and low input referred offset and noise. These comparators are well suited for high-speed high-resolution SAR ADCs. Finally, measured results validate the effectiveness of these comparators.

REFERENCES

[1] P. Harpe, E. Cantatore, and A. van Roermund, "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with data-driven noise reduction," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 270–271.

[2] H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta, "A 1.2-V dynamic bias latch-type comparator in 65-nm CMOS with 0.4-mV input noise," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1902–1912, Jul. 2018.

[3] Y. T. Wang *et al.*, "An 8-bit 150-MHz CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 308–317, Mar. 2000.

[4] B. Razavi, "The StrongARM latch [A circuit for all Seasons]," *IEEE Solid StateCircuits Mag.*, vol. 7, no. 2, pp. 12–17, Spring 2015.

[5] S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 343–352, Feb. 2014.

[6] A. Khorami and M. Sharifkhani, "A low-power high-speed comparator for precise applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 10, pp. 2038–2049, Oct. 2018.

[7] M. Abbas, Y. Furukawa, S. Komatsu, J. Y. Takahiro, and K. Asada, "Clocked comparator for high-speed applications in 65nm technology," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2010, pp. 1–4.

[8] J. Lu and J. Holleman, "A low-power high-precision comparator with time-domain bulk-tuned offset cancellation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1158–1167, May 2013.

[9] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 269–272.

[10] D. Shinkel *et al.*, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 314–315.

[11] M. van Elzakker *et al.*, "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.

[12] M. Brandolini *et al.*, "A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2922–2934, Dec. 2015.

[13] H. Zhuang, J. Liu, and N. Sun, "A fully-dynamic time-interleaved noise-shaping SAR ADC based on CIFF architecture," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Mar. 2020.

[14] H. Zhuang, H. Tang, and X. Liu, "Voltage comparator with 60% faster speed by using charge pump," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 2923–2927, Dec. 2020.

[15] P. M. Figueiredo and J. C. Vital, "Kickback noise reduction techniques for CMOS latched comparators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 7, pp. 541–545, Jul. 2006.