Lab 2: Modeling Blocks with HDL

ELEC 4601

Introduction

- ***In this lab exercise you will import an RTL design into System Generator as a black box.***

- A black box allows the design to be imported into System Generator even though the description is in Hardware Description Language (HDL) format.

- The System Generator Black Box block allows VHDL, Verilog, and EDIF to be brought into a design.

- The Black Box block behaves like other System Generator blocks - it is wired into the design, participates in simulations, and is compiled into hardware.

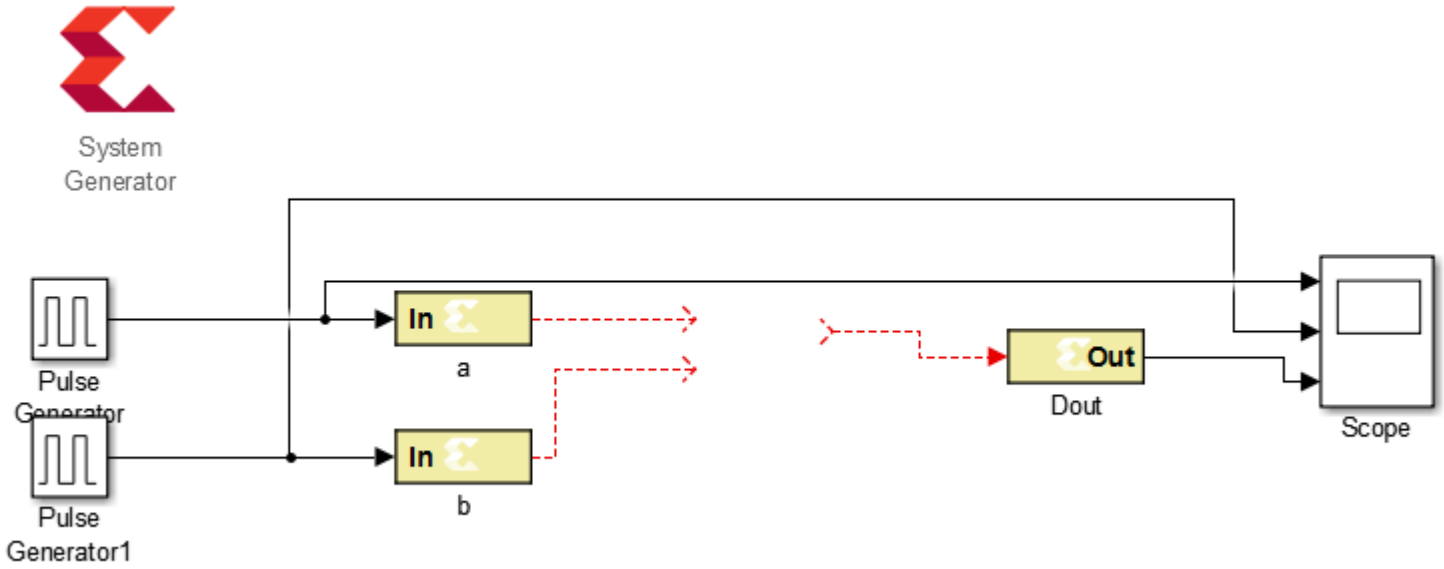
- When System Generator compiles a Black Box block, it automatically connects the ports of the Black Box to the rest of the design.

1. Design 8 bit adder using black box

- VHDL codes are given for 8-Bit Ripple Carry Adder design.
- Top level VHDL file for 8-bit adder is given in ‘bit8adder.vhd’ and low level full adder is given in ‘fulladder.vhd’.

Step 1

➢ Design a simulink model as given below to test 8-bit Adder .

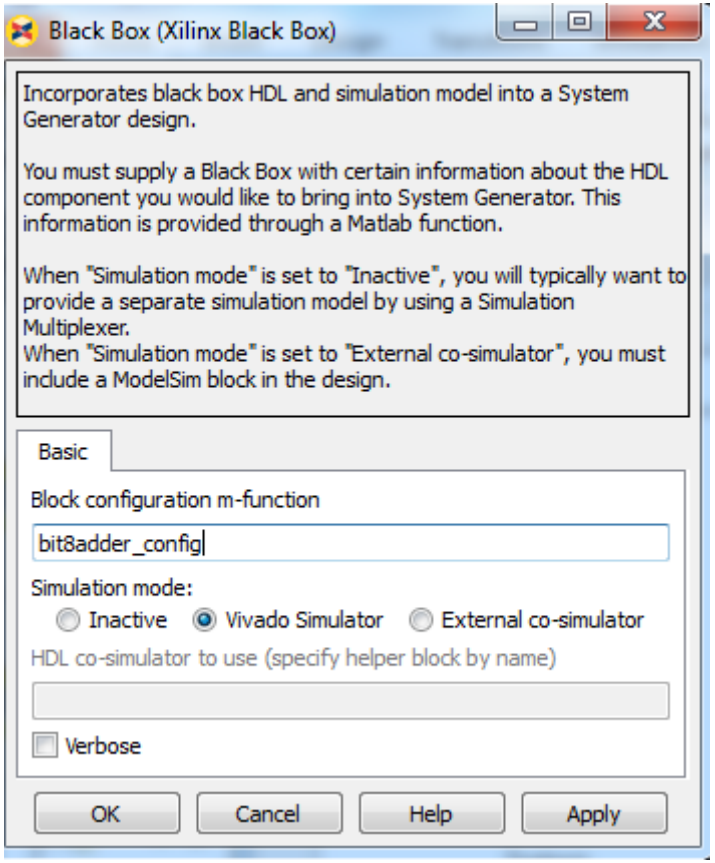


Step 2

- Right-click the design canvas, select **Xilinx BlockAdd**, and add a **Black Box** block to this subsystem.
- A browser window opens, listing the VHDL source files that can be associated with the black box.
- From this window, select the top-level VHDL file ‘bit8adder.vhd’.
- The associated configuration M-code ‘bit8adder_config.m’ opens in an Editor for modifications.
- Close the Editor.
- Wire the ports of the black box to the corresponding subsystem ports and save the design.

Step 3

- Double click the **Black Box** block to open the dialog box:
- Set the **Simulation mode** to **Vivado Simulator** and click **OK** to close the dialog box.



Step 4

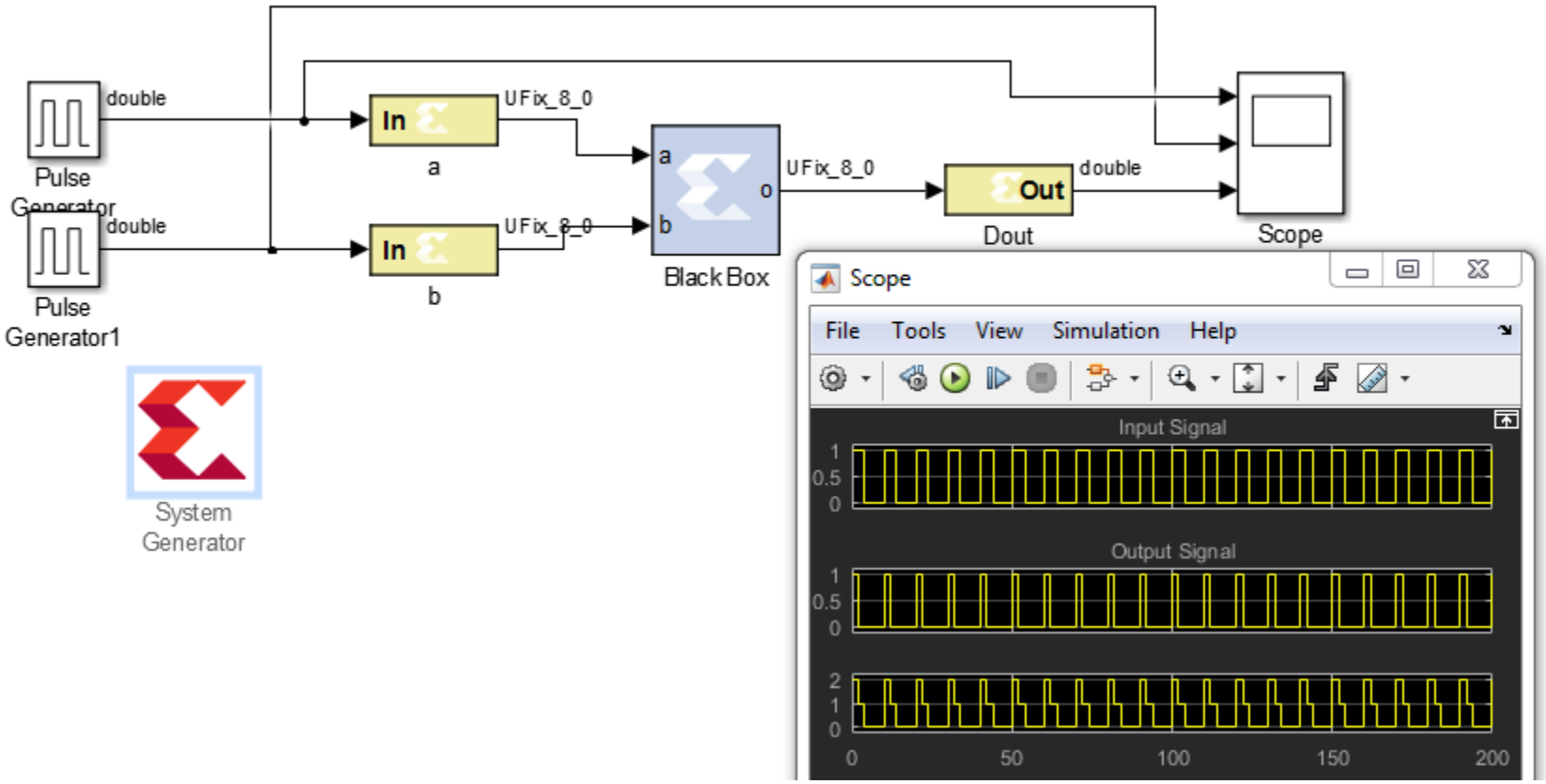
- Locate line 76:
  this_block.addFile('bit8adder.vhd')
- Immediately above this line, add the following:
  this_block.addFile('fulladder.vhd');

Step 5

- From the Simulink Editor menu, select **Display > Signals & Ports > Port Data Types** to display the port types for the black box.
- Compile the model (Ctrl-D) to ensure the port data types are up to date.
- Notice that the black box port output type is UFix_8_0.

Step 5

- Move to the design's top level and run the simulation by clicking the **Run** simulation button, then double-click the Scope block.



2. Design 1st order IIR filter using adder created with black box

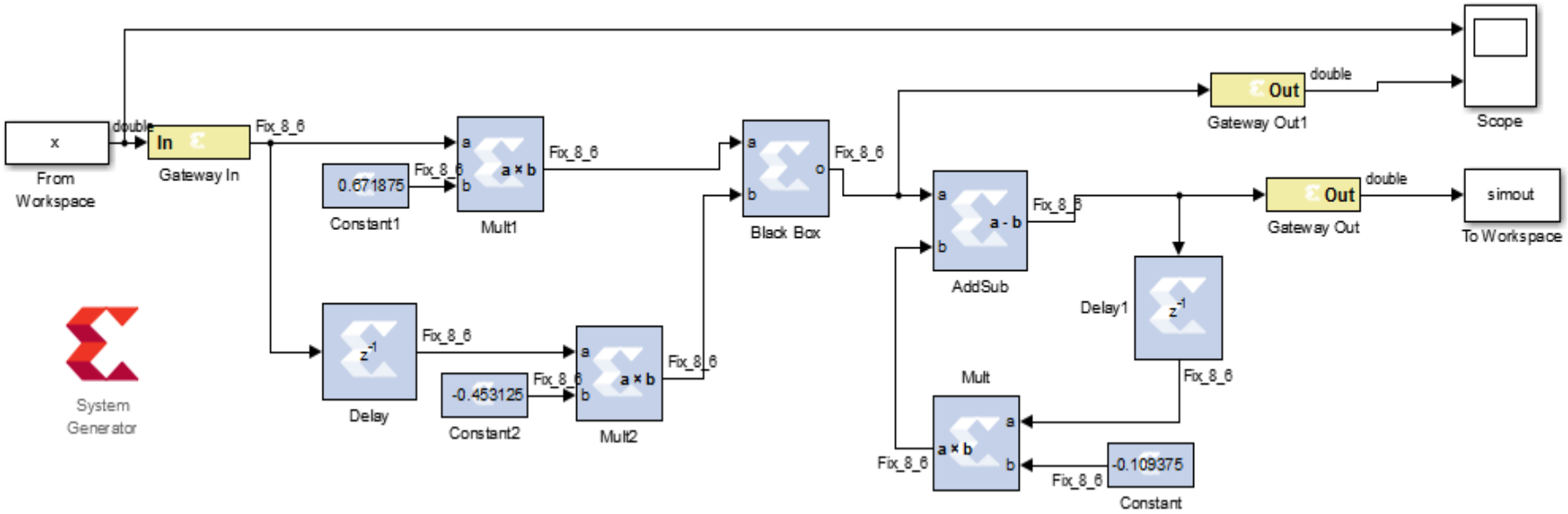
1st order transfer function: $H(z) = \frac{0.6732 - 0.447\, z^{-1}}{1 - 0.1118 z^{-1}}$

Step 1

- Use the implemented 8-bit adder in black box to implement numerator of the above transfer function.

Step 2

- Notice that the black box port output type is UFix_8_0.
  This means it is unsigned, 8-bits wide, and has a binary point 0 positions to the left of the least significant bit.
- Open the configuration M-function 'bit8adder_config.m' and change the output type from UFix_8_0 to Fix_8_6.
  The modified line (line 26) should read: o_port.setType('Fix_8_6');
- Change the fixed point precision values of the other simulink blocks to match the implemented adder in black box.


x
From Workspace
double
In
Gateway In
Fix_8_6
0.671875
Constant1
a × b
Mult1
Black Box
Out
Gateway Out1
double
Scope
AddSub
a - b
Out
Gateway Out
double
simout
To Workspace
Delay1
Mult
Delay
-0.453125
Constant2
Mult2
-0.109375
Constant
System Generator

Reference

1.https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_2/ug948-vivado-sysgen-tutorial.pdf