Lab Activity 3

ELEC 4601, Digital and Embedded System Design, Session 2 2018

Task Description

Consider the following infinite impulse response (IIR) filter

$$y(n) = x(n) + ay(n-3) + by(n-5)$$

where the filter coefficients are given as $a = 0.3$ and $b = -0.412$. A Matlab script producing the ideal impulse and frequency responses of this filter is provided to you.

(i) It is required to implement this filter to achieve a real-time processing throughput of 150M samples per second and it turns out that you have to employ parallel processing techniques to achieve this throughput (the best possible clock speed corresponding to this filter with re-timing and no look-ahead pipelining is ≈90MHz). Implement a 2-parallel version of this filter and verify the functionality with hardware co-simulation on Zedboard. You will have to use the J-unfolding technique to obtain the parallel implementation and the down-sampling blocks to obtain a polyphase decomposition (2-phase decomposition in this case) of the input. Report the filter response from a correctly implemented design and provide FPGA resource consumption, T_{cpd}, speed and throughput figures of your implementation. You should select a suitable fixed point precision for your design.

(ii) In another scenario, it is required to obtain a 2-folded implementation of the above filter to achieve reduced area while compromising the real-time throughput. Implement the above IIR filter in a 2-folded architecture that uses one adder and one multiplier and minimum number of registers possible. Note that this is the same example you did the class, hence the folded design is already available. Use 1-stage pipelining for the folded adder and 2-stage pipelining for the folded multiplier. Verify the functionality of the filter by computing the impulse and frequency responses from hardware co-simulation. Obtain FPGA resource consumption, T_{cpd}, speed and throughput figures of your implementation.

Submit a hardcopy report (2-4 page) no later than **08/10/2018** including correctly implemented and tested designs for both (i) and (ii) and a comparison between the two architecture in terms of FPGA resources and throughput.

Student Name:

Student ID:

Lab demonstrator signature: