Lab Activity 2

ELEC 4601, Digital and Embedded System Design, Session 2 2018

Task Description

1. With the given VHDL files of an 8-bit ripple carry adder, verify the operation of this adder using the "black-box" in the Xilinx block set. Follow the steps given in the guidelines.

2. Use the verified black-box adder design to implement the feed-forward addition (i.e. the adder in the numerator) of the following first order IIR transfer function:

$$H(z) = \frac{a_0 + a_1 z^{-1}}{1 + b_1 z^{-1}},$$

where the coefficients are $a_0 = 0.6732$, $a_1 = -0.447$, $b_1 = -0.1118$. Since the VHDL adder is hard-coded to 8-bits, use appropriate fixed-point precision for rest of the design. Verify the functionality of the IIR filter by comparing the frequency response to the ideal response. Perform synthesis and implementation (generate for HDL netlist) and obtain the critical path of the design. Perform hardware co-simulation on the Zedboard and verify the correct operation of the filter. (You may use pipelining in the feed-forward part of the design to optimise for critical path).

Submit a hardcopy report (1-2 page) no later than **17/09/2018** showing a correctly implemented design.

Student Name:

Student ID:

Lab demonstrator signature: