Lab Activity 1

ELEC 4601, Digital and Embedded System Design, Session 2 2018

Task Description

Consider a 32-tap FIR low-pass filter given by

$$y(n) = \sum_{k=0}^{31} a_k x(n-k),$$

where the filter coefficients are given in the Matlab script provided for this lab. The provided Matlab script also generates a two tone signal to be used as the test input. Perform the following steps.

1. Implement the given filter in a suitable structure and perform a functional verification by evaluating the filter response and using the test input signal provided. Examine the operation by playing the audio input and output to verify the low-pass operation. You should select a reasonable fixed point precision based on your observations.

2. Optimise your implementation as much as you can so that it attains the best possible critical path delay (T_{cpd}). Perform HDL net list generation and report the FPGA resource utilisation, T_{cpd} and maximum speed F_{max}. Also, comment on the real-time throughput of this implementation.

3. Compile the design to the target board provided (i.e. Xilinx Zedboard Zynq Evaluation and Development kit) and perform a hardware in-the-loop co-simulation with the test input signal provided in Matlab. Verify the operation by playing the audio input and output.

Submit a hardcopy report (2-4 page) no later than **10/09/2018**. The report should include a description of any design and optimisation techniques used, functional verification results (such as filter responses, spectrum of the input and output), hardware resource and speed performance and any conclusions drawn.

Student Name:

Student ID:

Lab demonstrator signature: