(17)

*Annexure 'B'*

# SPECIFICATIONS

## Video Processing Electronics for HD Detector — Qty: 02 Sets

The work encompasses design and development of 02 Sets of Video Processing Electronics for interfacing and video signal processing of sensor data. The Video Processing Electronics will comprise of a Video Processing Card (VPC) and a Rigi-Flex cable. Vendor will also develop detector interfacing module and various image processing modules in VHDL. A PC based test software compatible with Windows 10 Pro Operating System incorporating a Graphical User Interface (GUI) for health check of the components of the VPC is to be developed. The detailed specifications are as given below

### 1. Video Processing Card (VPC)

The VPC will be interfaced with the sensor through a rigi-flex cable and will provide the necessary power, clocks and control signals for its operation. VPC will be designed around a Xilinx FPGA and the dimensions of the card are to be as per the attached drawing (70mm x 50mm). The block diagram representation of the board is given in fig 1. The VPC will be designed having interfaces and components defined below. Equivalent components having similar working, performance and qualification standards may be used and are to be mentioned in the technical bid.

~~a)~~ **FPGA** – Xilinx Kintex/Virtex 7 or Kintex/Virtex Ultrascale FPGA Device (Industrial grade) .

**b) Video Interfaces**

(i) One video input in digital format using LVDS serial link similar to CAMLINK interface using 100 pin BGA SAMTEC male connector (YFT-20-05-H-05-SB).

(ii) **28 Bit Channel Link** – Two channel Link receiver for converting LVDS data into 28 bit LVTTL/LVCMOS data on each link using FIN3386MTDX (28:4 Receiver) from Fairchild Semiconductor. It converts the four LVDS data streams back into 28 bits of LVCMOS/LVTTL data acting as the deserializer.

(iii) Two parallel composite video output through single channel video DAC ADV7123 from Analog Devices. The Green channel is to be used for input of digital data whereas blue and red channel should be tied to ground. The analog outputs to be terminated with the same load as that of the used channel. The composite video output will be terminated on two SMB connector using AD8054 or other high speed video amplifier.

(iv) One video output in digital format using LVDS link similar to CAMLINK interface using 26 pin 3M connectors (12226-8250).

(v) One Output digital video in HD-SDI format.

**c) Memory Interface**

**(i)** DDR2 Memeory – One 20MB X 16 bit fast asynchronous DDR2 RAM to be interfaced with FPGA independently.

**(ii) Flash Memory–** One 512 Mbit (32M X 16bit) non-volatile Flash Memory that can be erased electrically at the block level and programmed in-system on a Word-by-Word basis. This memory is to be interfaced with FPGA.

**(iii) EEPROM** – One no. of 02 wire serial EEPROM (AT24C08) with capacity of 2Kilobytes.

**d) Serial Interface**

(i) Three channel RS232 interface with FPGA using MAX3162 or suitable transceiver. One RS232 link each to be made available at J1, J2 and J3 connectors shown in the attached drawing.

(ii) Two channel RS422 interface with FPGA using MAX3076 or suitable transceiver .These serial interfaces should be made available on J3 connector.

(iii)One no. each of High Speed Differential Driver & Receiver (SN65LVDS3487 & 86) interfaced to FPGA for LVDS data transfer using 100 pin Samtec connector.

e) **Input Output Interface** - 16 pulled up LVTTL outputs using SN74CBDT3861/TXS0108E or suitable interface ICs to be provided on J4 Connector

f) **User LEDs** – Four user LEDs to be interfaced with FPGA

g) **Temperature Sensor** – Two wire sensor interface for temperature measurement of the FPGA board (TMP123) capable of measuring temperatures within 1.5°C of accuracy over a temperature range of −40°C to +125°C.

h) **RESET** – Power on reset to be provided for FPGA

i) **System Clock** – System Clock of 100 MHz to be generated on board and provided to FPGA.

j) **Connectors:**

(i) **Nicomatic Connector (J1)** – One no. of 08 pin 'L' shape Nicomatic connector(221R08F26)

(ii) **Nicomatic Connector (J2)** – One no. of 12 pin 'L' shape Nicomatic connector(221R12F26)

(iii) **Nicomatic Connector (J3)** – One no. of 08 pin straight Nicomatic connector(221Y08F21)

(iv) **Nicomatic Connector (J4)** – One no. of 20 pin straight Nicomatic connector(221Y20F21)

(v) **3M Connector(J5)** – One no. of 26 pin 3M Connector (12226-8250)

(vi) **Nicomatic (J6, J7)** – Two nos. of coaxial video connector for composite video interface.

(vii) **Samtec Connector (J8)** - One no. of 100 pin BGA Samtec male connector for sensor interface (YFT-20-05-H-05-SB).

(viii) **Nicomatic (J9)** – One no. of coaxial video connector for digital HD-SDI digital video interface.

**k) Configuration**

(i) JTAG interface for FPGA and its configuration PROM to be provided. This JTAG interface should be available on J2 connector for external revision control and download of new bit stream.

(ii) At least 02 nos. of platform flash In-System programmable PROMs (XCF32P) for configuration of FPGA should be provided. They should have provision for two independent bit streams for storing either two revisions or two separate programs. The downloading of the bit stream to be controlled through external interface.

**l) Power Supply**

(i) Input power supply of +5 V is to be given on Nicomatic connector (J1).

(ii) All other necessary power supplies are to be generated on board.

**m) Master Clock** - Master Clock of 100 MHz.

*Annexure 'B'*

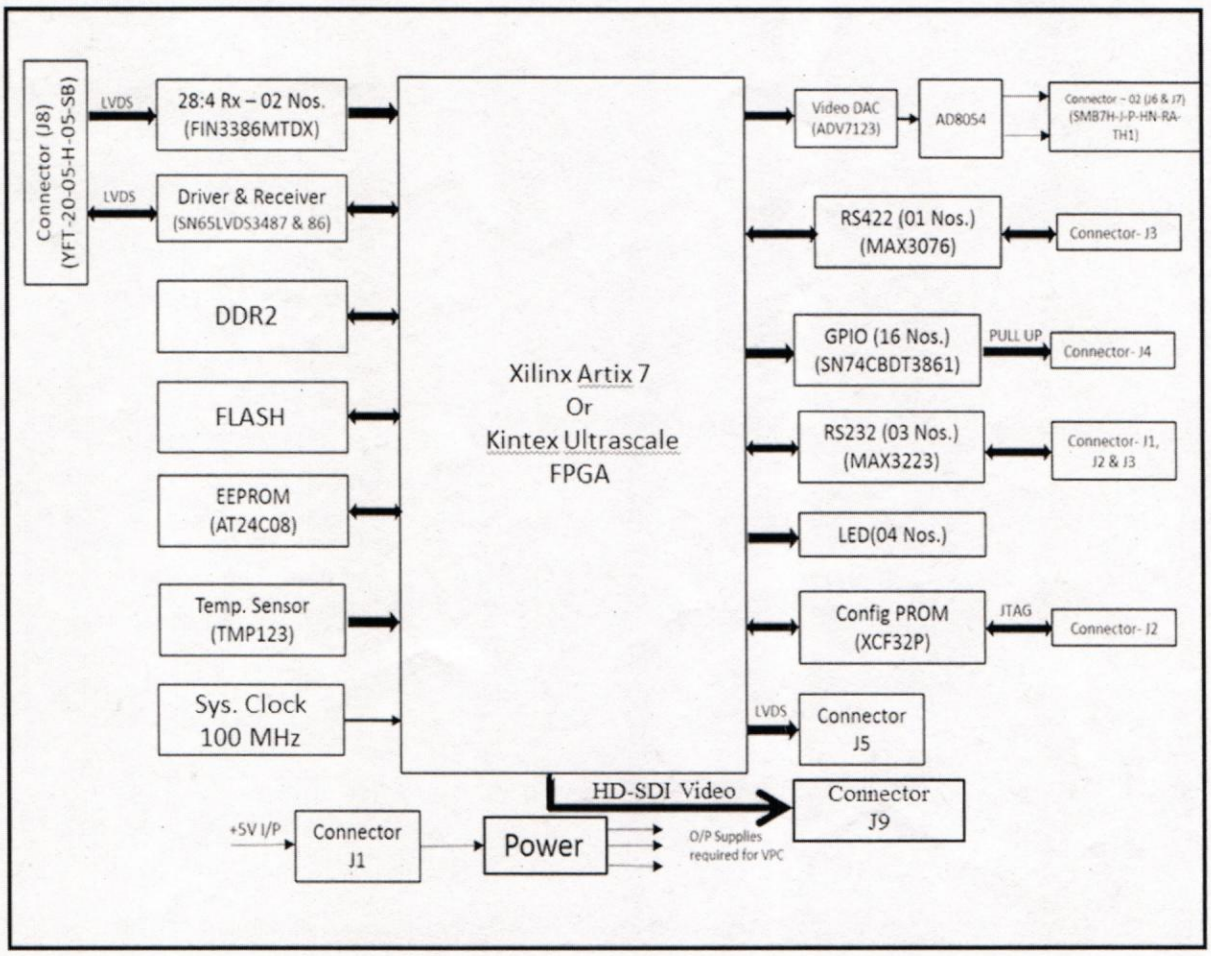


**Fig 1: Block Diagram of Video Processing Card**

## 2. Rigi-Flex PCB

a) Upto 6 layer Flex-PCB addressing all high speed constraints and noise issues.

b) Two 100 Pin BGA Connectors from SAMTEC (YFS-20-03-H-05-SB-K) to be used on Flex PCB for connecting IDDCA to Signal Processing Card

c) Mechanical Dimensions/Drawing of the Flex PCBs to be as per attached drawing

d) Design/Schematics for Flex PCB connections will be provided by IRDE.

**3. Software**

1. Vendor should develop hardware project in VHDL and PC based application. PC based graphical user interface should be developed for providing various commands to the system and also for controlling the sensor parameters. This GUI should also provide feature for camera calibration and maintenance.
2. Vendor should develop hardware project in VHDL to interface HD MWIR Detector and implement following image processing features/calibration:
    i. Real time implementation using FPGA.
    ii. IR Sensor control & interface.
    iii. Digital scan conversion.
    iv. Non-uniformity corrections and PC based calibration software.
    v. One point NUC.
    vi. Reticle/Symbology generation.
    vii. Bad pixel replacement
    viii. Polarity inversion
    ix. Electronic Zoom
    x. Dynamic range compression for automatics image adjustment.
    xi. Manual brightness and contrast adjustment.
    xii. Contrast improvement.
    xiii. Edge enhancement and noise removal.
    xiv. Image Enhancement Algorithm (Histogram Based).
    xv. Optics Controller .
    xvi. Motion Detection in Video.
    xvii. Pseudo Coloring.
    xviii. Real time Bad Pixels Identification and Replacement with moving cursor.
    xix. PC based interface & control.
    xx. Software development for autofocussing.
    xxi. ROIC

3. Vendor should develop HDL test codes and PC based software with Graphical User Interface (GUI) for testing of all the components/interfaces on board.

4. Vendor should develop the hardware projects and PC based application for SRAM (read and write) and Flash Interface (read, write and erase) for their functionality.
5. The testing software is to be developed for the PC based hardware platform compatible with Windows 10 Pro Operating System and to be supplied with the video processing electronics and rigi-flex cable on a memory stick.
6. The vendor should test the PCB for full functionality by integrating with the sensor system in presence of IRDE scientists at IRDE.

## 4. PCB Design

(i) Mechanical dimensions and mounting hole locations are given in the drawings attached in Annexure 'B' for the VPC and rigi-flex.

(ii) All boards are to be multilayer PCB having upto 14 layers with high-speed considerations and all signal integrity and noise issues addressed.

(iii) Vendor should generate and get approved, the complete schematic and layout of all the boards before fabrication

(iv) Vendor to ensure that the PCB is designed to work properly from -30°C to +80°C temperature range using SMD components in Industrial grade.

(v) All PCBs are to be rugged and designed for EMI/EMC compliance.

(vi) Locations for the connectors on the boards are provided in the attached drawings

## 5. Deliverables

**Video Processing Unite** **02 sets**

One set will comprise of following items:

(i) One (01) no. of Video Processing Card as per specifications above.

(ii) One (01) no. of rigi-flex cable as per specifications above.

(iii) One (01) no. of Xilinx OEM USB programmer with JTAG interface for configuration of FPGA.

(iv) 02 (01 + 01 Spare) sets of mating connector for each connector used in the Video Processing Card (VPC)

(v) Two (02) No. of 3M SDR Cable Assembly (1SD26-R120-00C-A00)

(vi) One (01) no. of Integrated Development Environment with Workstation (HP Zbook Firefly 15.6 G8 mobile workstation or better).

(vii) Vendor should supply the gerber data for all boards.

(viii) All software with source codes, application program, hardware project files with source codes and test programs are to be provided on a pen drive.

(ix) Complete PCB related documents to be provided for all boards.

(x) Complete software and hardware design documents are to be provided.

**6. Warranty**

One Year from date of delivery.

**7. OTHER TERMS AND CONDITIONS:**

a) Only Indian Vendors are eligible to quote.

b) Non-recurring expenditure (NRE) cost also to be mentioned separately.

c) Industry partner shall compulsorily enclose all proofs as Annexure to response to RFP. Responses which are not in compliance with our RFP conditions will be rejected, without assigning any reasons thereof. IRDE reserves the right to request for any additional information, if required. Failure to furnish all requisite information or and/or documents shall result in repudiation of the RFP, without assigning any reasons thereof.

d) Industry partner must submit duly filled compliance/ non compliance chart of the requested technical and techno-commercial terms.

e) The industry partner may be called for a presentation in front of the Techno-commercial Evaluation Committee (TCEC) after opening of the technical bids if required. Identified agency will not sell the technology, process, equipment or systems to any Third party, unless otherwise authorized by IRDE/DRDO/MoD/Govt. of India.

f) Intellectual property of the products will rest to the IRDE. IRDE will be the sole owner of all patents, papers and other publications, which are generated directly or indirectly on the work carried out for this activity.

g) Any issues related to licensing / development / run time fees for all the software used in the project should be handled by the industry partner, and all such licenses should be valid perpetually.

h) The quoted price should include deputation of 2 engineers for 6 months at IRDE for customization of software along with IRDE team, free of cost. The deputation should cover the complete customization of hardware / software aspects of the system.

i) Industry partner is responsible for onsite integration, testing, demonstration and onsite warranty at IRDE, Dehradun. Industry partner should provide warranty of the system for one year from the date of acceptance of final deliverable system anywhere in India.

j) Industry partner may modify the design during development subject to the prior approval of IRDE.

k) The vendor will provide workstations (HP Zbook Firefly 15.6 G8 mobile workstation or better) along with the development tool to their engineers for the development work, which will be handed over to IRDE after completion of work.

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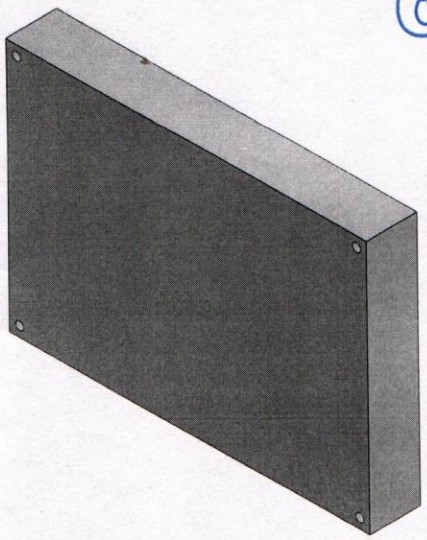

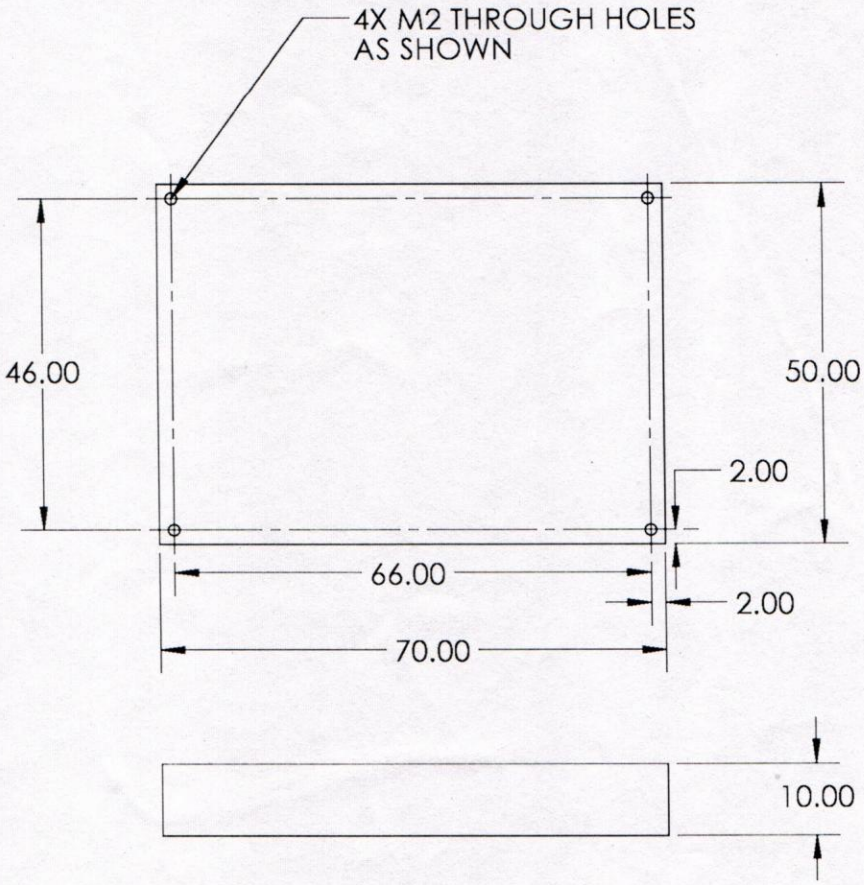


NOTE: THE VIDEO CARD INCLUDING POPULATED COMPONENT SHOULD BE FIT INSIDE THE GIVEN VOLUME

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MATERIAL : AL ALLOY IS:733-24345 | | | | | | | |
| | | | | | FINISH : ANODISED BLACK | | | | | | | |
| | | | | | GENERAL MACHINING TOLERANCE : | | | | | | AUTHORITY | NAME & SIG. | DATE |
| | | | | | LINEAR UP TO 6 >6-30 >30-120 >120-315 >315 ±0.1 ±0.2 ±0.3 ±0.5 ±0.8 | | | | | | DESIGNED BY | | |
| | | | | | ANGULAR ±30' | | | | | | DRAWN BY | | |
| | | | | | POSITION ±0.1 | | | | | | CHECKED BY | | |
| | | | | | CONCENTRICITY ±0.1 | | | | | | APPROVED BY | | |
| | | | | | SURFACE FINISH <12.5 µm | | | | | | CAT/ PT. NO. | | |
| | | | | | CORNER RADIUS 0.5(Max.) | | | | | | | | |
| | | | | | CHAMFER ON EDGES 0.5X0.5 | | | | | | | | |
| @ | | ISSUE-1 | | 02-07-13 | ROUGHNESS SYM. | | | | | | BASED ON | | |
| SYMBOL | ZONE | ISSUE | AUTH. | DATE | ROUGHNESS VALUE( m) | 50-25 | 25-6.3 | 6.3-0.8 | 0.8-0.1 | < 0.1 | USED ON | | |

ALL DIMENSIONS ARE IN mm UNLESS OTHERWISE SPECIFIED

# PCB

IRDE INSTRUMENTS RESEARCH & DEVELOPMENT ESTABLISHMENT, DEHRA DUN

DRG. NO. ----------

SCALE 1:1 SHT OF

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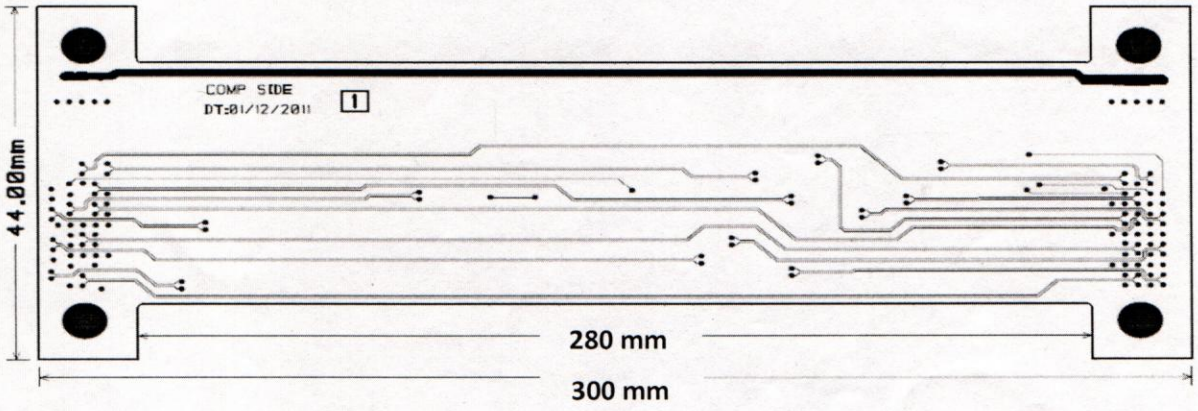
(7)

**Regiflex Cable** **Qty: 02 Sets**

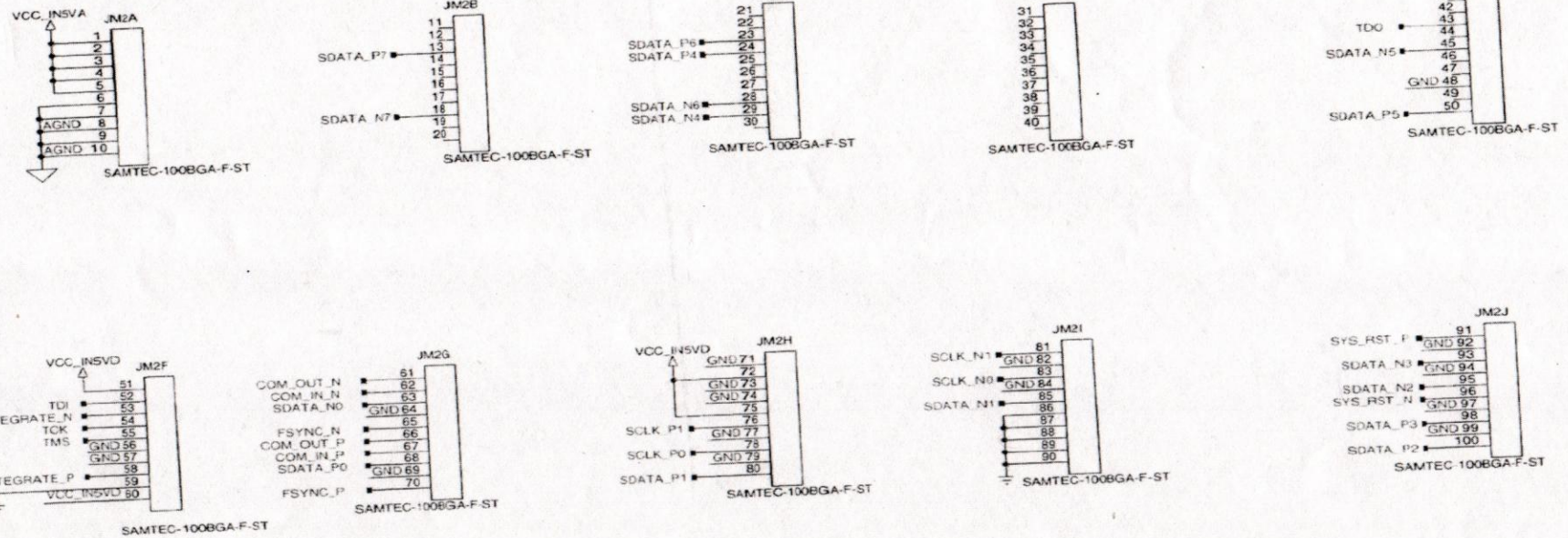
- Upto 6 layer PCB addressing all high speed constraints and noise issues.
- Two 100 Pin BGA Connectors from SAMTEC to be used on Flex PCB for connecting IDDCA to Signal Processing Card
- Operating temp : -30°C to +60°C
- Mechanical Dimensions/Drawing of the Flex PCBs are as given below
- Flex PCB Connections to be as per schematic.
- Vendor should generate and get approved, the complete schematic and layout of the PCB before fabrication.
- Complete Final Hardware Schematic and Gerber Data should be provided

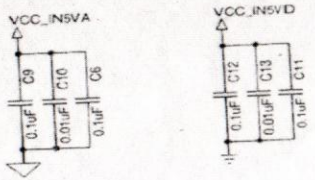
**STRAIGHT FLEX PCB WITH LENGTH 300 mm**



(6)

## VPC SIDE



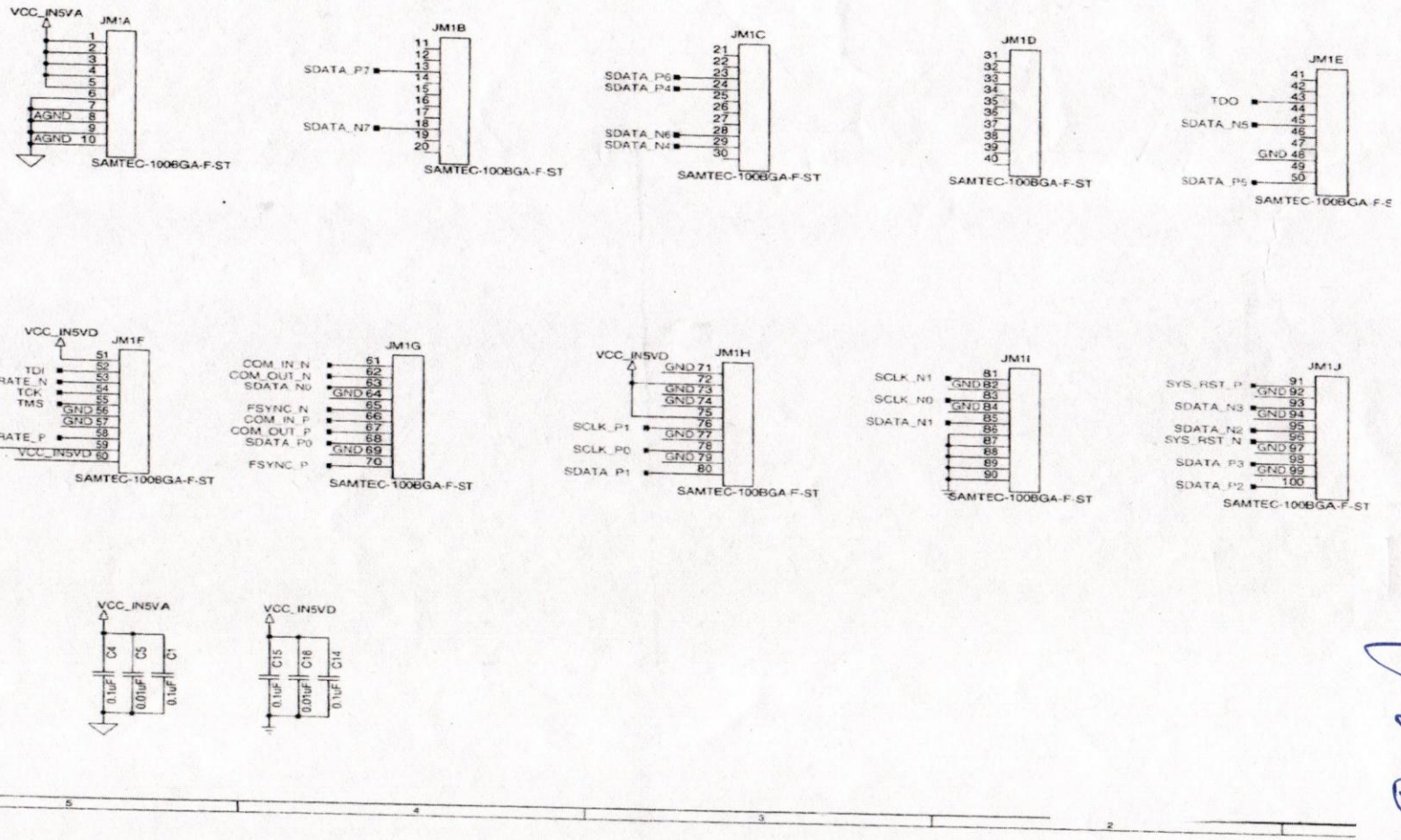




SAMTEC Connecter – YFS-20-03-H-05-SB-K

Rule 6

(5)

# PROXY SIDE


VCC_IN5VA
JM1A
AGND
AGND
SAMTEC-100BGA-F-ST
JM1B
SDATA_P7
SDATA_N7
SAMTEC-100BGA-F-ST
JM1C
SDATA_P6
SDATA_P4
SDATA_N6
SDATA_N4
SAMTEC-100BGA-F-ST
JM1D
SAMTEC-100BGA-F-ST
JM1E
TDO
SDATA_N5
GND
SDATA_P5
SAMTEC-100BGA-F-S
VCC_IN5VD
JM1F
TDI
INTEGRATE_N
TCK
TMS
GND
GND
INTEGRATE_P
VCC_IN5VD
SAMTEC-100BGA-F-ST
JM1G
COM_IN_N
COM_OUT_N
SDATA_N0
GND
FSYNC_N
COM_IN_P
COM_OUT_P
SDATA_P0
GND
FSYNC_P
SAMTEC-100BGA-F-ST
VCC_IN5VD
JM1H
GND
GND
GND
SCLK_P1
GND
SCLK_P0
GND
SDATA_P1
SAMTEC-100BGA-F-ST
JM1I
SCLK_N1
GND
SCLK_N0
GND
SDATA_N1
SAMTEC-100BGA-F-ST
JM1J
SYS_RST_P
GND
SDATA_N3
GND
SDATA_N2
SYS_RST_N
GND
SDATA_P3
GND
SDATA_P2
SAMTEC-100BGA-F-ST
VCC_IN5VA
C4
0.1uF
C5
0.01uF
C1
0.1uF
VCC_IN5VD
C15
0.1uF
C18
0.01uF
C14
0.1uF