

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**ECA31- NANOELECTRONICS**

**LIST OF LAB EXPERIMENTS**

1. Simulation of band structure and density of states of Materials (Metals, semiconductor, Insulators)
2. Simulation of density of states of Quantum well
3. Simulation of band structure of Nano Wire
4. Simulation of mesh analysis of Nano Wire
5. Simulation of energy state of Quantum dot
6. Simulation Voltage current characteristics of Resonance Tunneling Diode
7. Simulation of V-I characteristics of MOSFET by varying channel length
8. Simulation of VI Characteristics of MOSFET by varying oxide thickness
9. Simulation of VI Characteristics of Double gate MOSFET
10. Simulation of VI Characteristics of FinFET by varying the Channel Width and oxide thickness
11. Simulation of the equivalent circuit of Single Electron Transistor
12. Simulation of VI Characteristics of Coulomb Blockade
13. Simulation of electrical properties of Carbon Nanotube based on chiral vector (n,m)
14. Simulation of density of states and conductance mobility of electrons in CNTFET
15. Simulation of VI characterstics of Schottky barrier CNFET
16. Simulation of the temperature distribution on a moving substrate material prior to plasma treatment in a roll – to – roll plasma CVD system
17. Simulation of VI Characteristics of CNTFET by varying channel length
18. Simulation of VI Characteristics of CNTFET by varying cnt diameter
19. Simulation of Band structure and Density of States of Graphene by varying chiral vector
20. Simulation of VI characteristics of Graphene field effect transistor
21. Simulation of absorption spectra of nanomagnetic particles by varying the size.
22. Simulation of Tunnelling Magneto resistance (TMR) by varying oxide thickness and voltage of magnetic tunnel junction
23. Simulation of band structure and density of states of magnetic tunnel junction by varying barrier height
24. Simulation of Potential of a sensor by varying the pH value of an electrolyte and insulator thickness of biosensor
25. Simulation of VI characteristics of Bio-FET

**LAB MANUAL FOR NANO ELECTRONICS**

**Simulation of band structure and density of states of Materials**

**( Metals, semiconductor, Insulators)**

**Ex. No: 1**

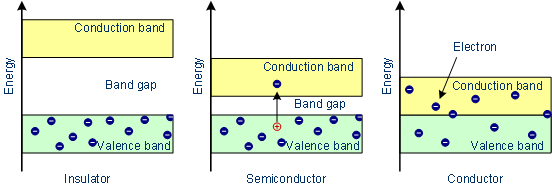
**Date:**

**Aim:**

To Obtain the band structure and density of states of Semiconductor, Metal and Insulator.

**Software:** NanoHub Online Tube

**Theory:**



1. (b) (c)

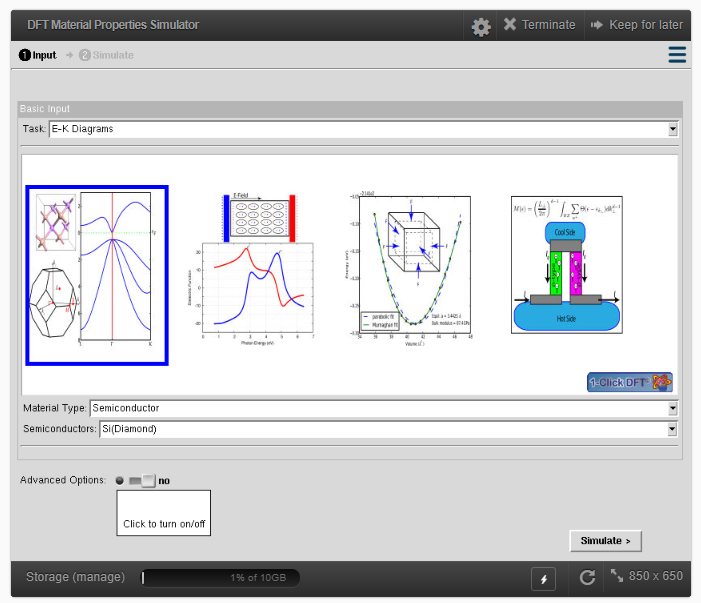
Every solid has its own characteristic energy band structure. In order for a material to be conductive, both free electrons and empty states must be available. Insulators have filled valence bands and empty conduction bands, separated by a large band gap Eg(typically >4eV), they have high resistivity (a ). Semiconductors have similar band structure as insulators but with a much smaller band gap. Some electrons can jump to the empty conduction band by thermal or optical excitation (b). Eg=1.1 eV for Si, 0.67 eV for Ge and 1.43 eV for GaAs

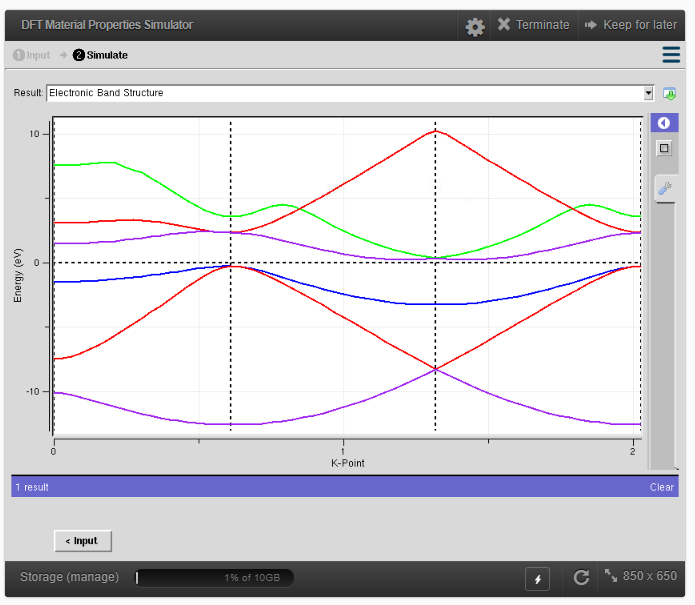
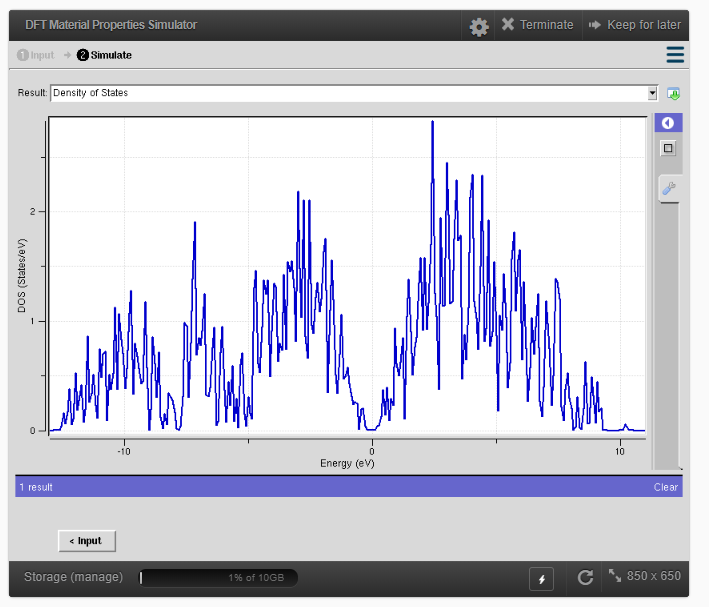
Metals or conductor have free electrons and partially filled valence bands, therefore they are highly conductive (c).

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select Band structure -> DFT Materials Properties -> Launch.
* Press Launch tool in info section.
* Select the Materials (Metal/Semiconductor/Insulator).
* Press simulate to view results.
* Select Result -> band Structure
* Select Result -> Density of States.

**Model Output:**



** **

Band Structure Density of States

.

**Result:**

**Simulation of density of states of Quantum well**

**Ex. No: 2**

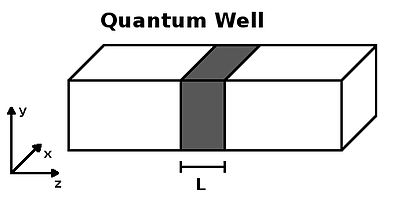
**Date:**

**Aim:**

To simulate density of states of quantum well structure with various nano meter thickness.

**Software:** NanoHub Online Tube

**Theory:**



A quantum well is a potential well with only discrete energy values. The classic model used to demonstrate a quantum well is to confine particles, which were originally free to move in three dimensions, to two dimensions, by forcing them to occupy a planar region. The effects of quantum confinement take place when the quantum well thickness becomes comparable to the de Broglie wavelength of the carriers (generally electrons and holes), leading to energy levels called "energy subbands", i.e., the carriers can only have discrete energy values.

**Procedure:**

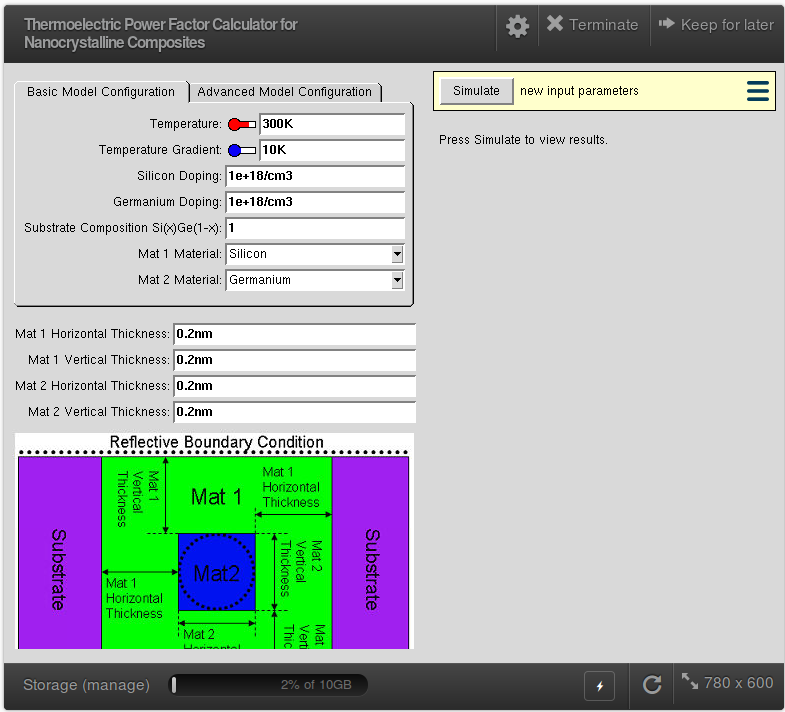
* Open nanoHUB.
* Goto Resources -> Tools.
* Select Quantum wells in Tags.
* Select Thermolelectric Factor calculator for nanocrystalline Composites in Resources.
* Press Launch tool in info section.
* Enter appropriate values in required section.
* Select the Materials (Germanium/ Silicon).
* Enter the material thickness required.
* Press simulate to view results.
* Select the Materials (Germanium/ Silicon).
* Enter the material thickness required.
* Press simulate to view results.
* Compare both the results.

**Parameters:**

**Tabulation:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.NO** | **Materials** | **Material Thickness (nm)** | **Density of States** |
| 1 | Material 1: Silicon  Material 2: Germanium |  |  |
| 2 | Material 1: Germanium  Material 2: Silicon |  |  |
| 3 | Material 1: Silicon  Material 2: Germanium |  |  |
| 4 | Material 1: Germanium  Material 2: Silicon |  |  |

**Model Output:**

.

**Result:**

**Simulation of band structure of Nano Wire**

**Ex. No: 3**

**Date:**

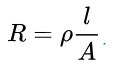
**Aim:**

To simulate the band structure of nanowire for various materials.

**Software:** NanoHub Online Tube

**Theory:**

A quantum wire is an electrically conducting wire in which quantum effects influence the transport properties. Usually such effects appear in the dimension of nanometres. If the diameter of a wire is sufficiently small, electrons will experience quantum confinement in the transverse direction. As a result, their transverse energy will be limited to a series of discrete values. One consequence of this quantization is that the classical formula for calculating the electrical resistance of a wire



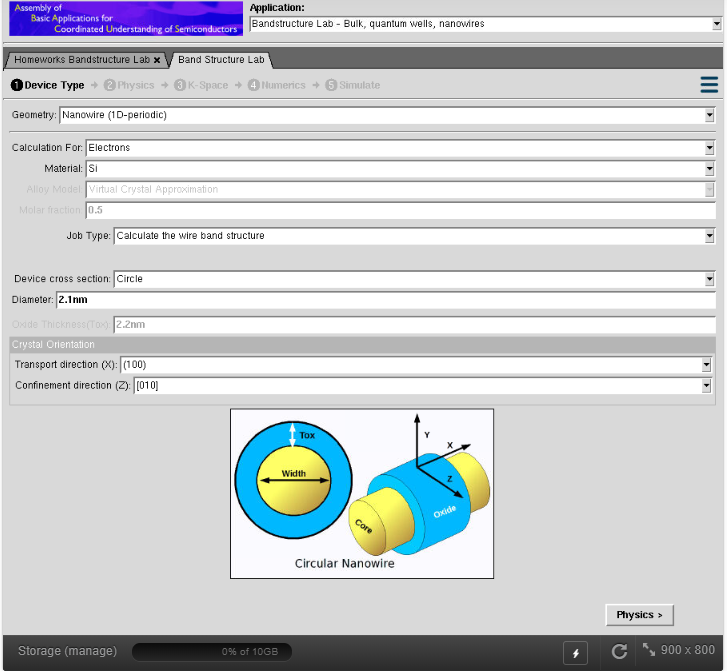
**Procedure:**

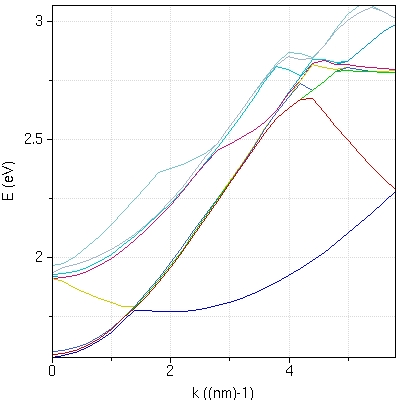
* Open nanoHUB.
* Goto Resources -> Tools.
* Select Nanowire in Tags.
* Select ABACUS - Assembly of Basic Applications for Coordinated Understanding of Semiconductors in Resources.
* Press Launch tool in info section.
* Select the Applications -> Band structure Lab
* Select Geometry -> 1D Nanowire
* Device cross section -> Circular
* Select the Material Type
* Press simulate to view results.
* Compare the results of various materials.

**Parameters:**

**Model Output:**

For Silicon having diameter 2 nm

****



.

**Result:**

**Simulation of mesh analysis of Nano wire by varying the following parameters**

* **Doping concentration**
* **Gate Voltage**
* **Source and drain voltage**

**Ex. No: 4**

**Date:**

**Aim:**

Mesh analysis of Nano wire by varying the following parameters are Doping concentration, Gate Voltage, Source and drain voltage.

**Abstract:**

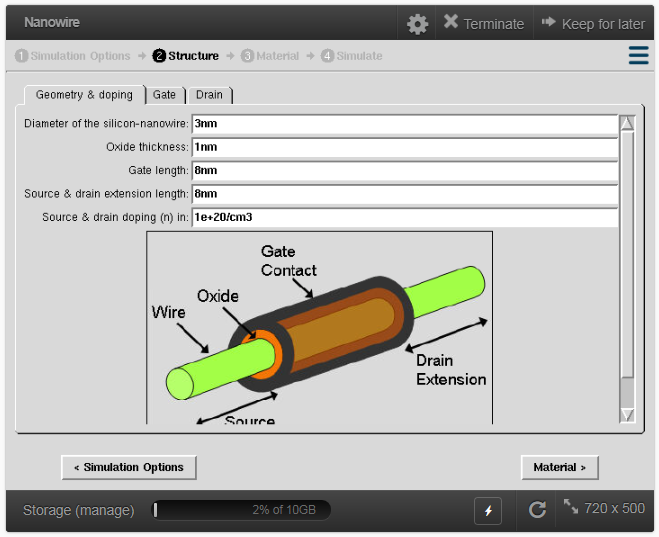
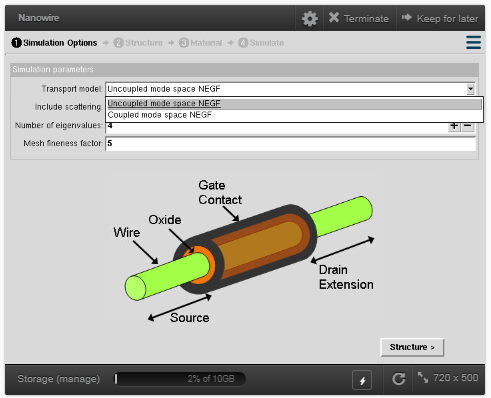
Silicon nanowire transistors are promising device structures for future integrated circuits. Short channel effects are becoming more and more important in the nanoscale regime, and therefore effective gate control will be necessary to achieve good device performance. Devices based on silicon nanowires can be manufactured with multigate and gate-all-around transistors and you can explore them with this tool.

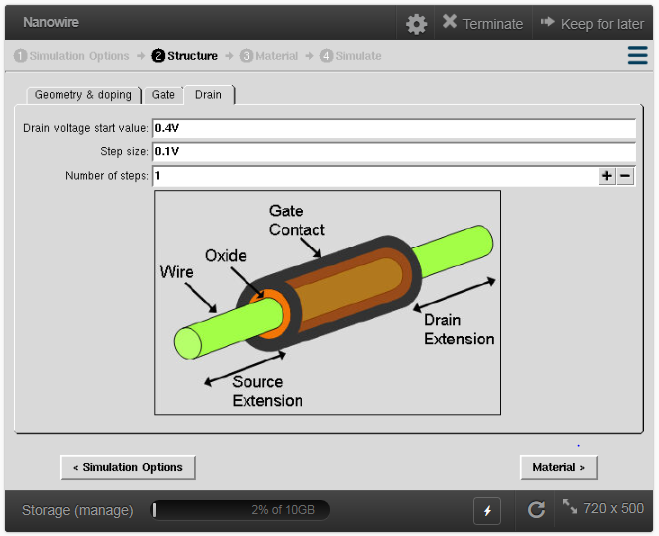
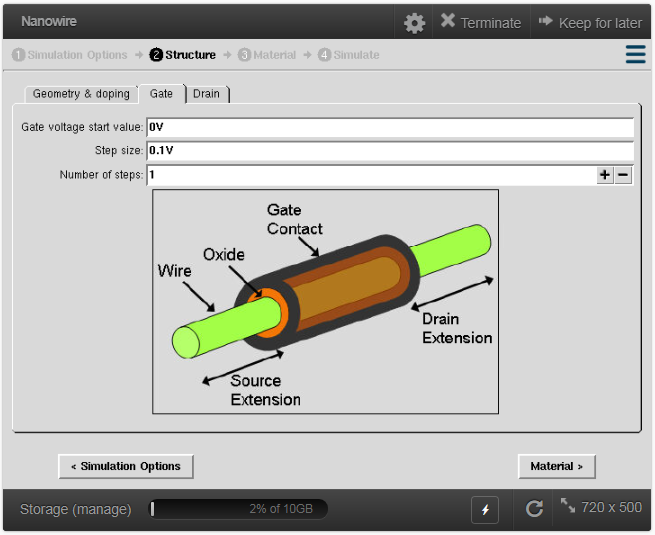
In contrast to planar MOSFETs which have uniform charge and potential profiles in the transverse direction (i.e., normal to both the gate and the source-drain direction), a silicon nanowire transistor has a genuinely 3D distribution of electron density and electrostatic potential. Therefore self-consistent 3D simulations are mandatory, and you run them with this tool. One of the transport models assumes ballistic transport, which gives the upper performance limit of the devices. The effective-mass mode space approach (either coupled or uncoupled) produces high computational efficiency that makes this simulator practical for extensive device simulation and design.

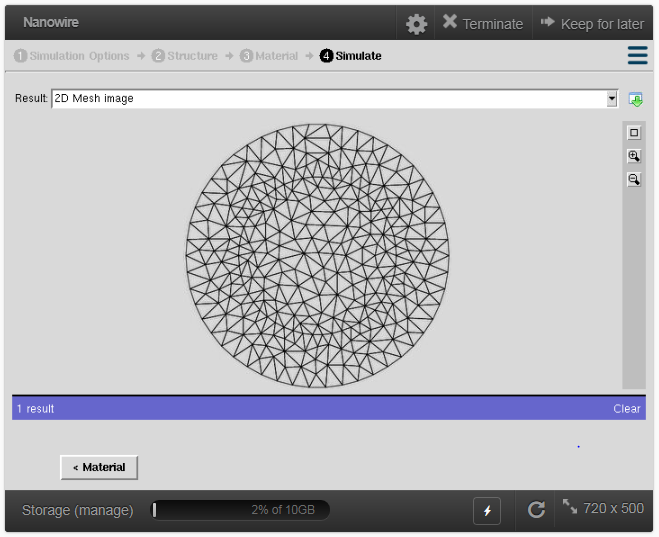
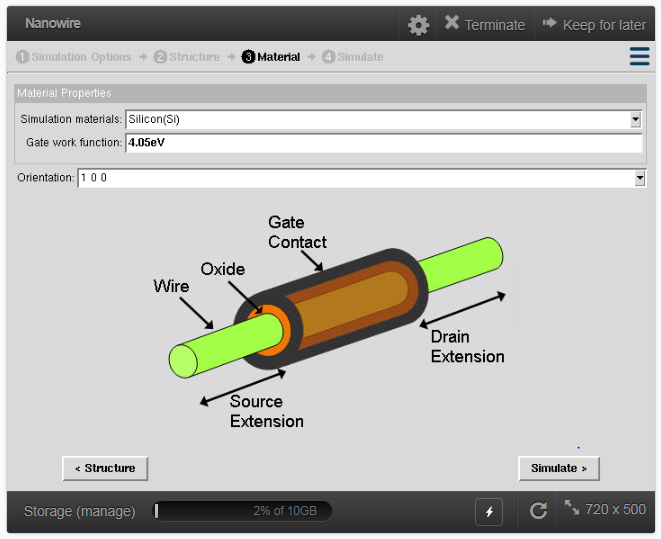
**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select Nanowire NEGF in Tags.
* Select Nanowire
* Select Simulate 3D nanowire transport in the effective mass approximation with phonon scattering and 3D Poisson self-consistent solution
* Press Launch tool in info section.
* Enter appropriate values in required section.
* Proceed simulation option.
* Proceed structure.
* Proceed material.
* Press simulate to view results.
* Enter appropriate values in required section.
* Proceed simulation option.
* Proceed structure.
* Proceed material.
* Press simulate to view results.
* Compare both the results.

**Outputs:**







**Results:**

**Simulation of energy state of Quantum dot**

**Ex. No: 5**

**Date:**

**Aim:**

To obtain the energy states of Quantum dot.

**Software:** NanoHub Online Tube

**Theory:**

Quantum dots (QD) are very small semiconductor particles, only several nanometres in size, so small that their optical and electronic properties differ from those of larger particles. They are a central theme in nanotechnology. Many types of quantum dot will emit light of specific frequencies if electricity or light is applied to them, and these frequencies can be precisely tuned by changing the dots' size, shape and material, giving rise to many applications. Quantum dots exhibit properties that are intermediate between those of bulk semiconductors and those of discrete molecules. Their optoelectronic properties change as a function of both size and shape. Larger QDs (diameter of 5–6 nm, for example) emit longer wavelengths resulting in emission colors such as orange or red. Smaller QDs (diameter of 2–3 nm, for example) emit shorter wavelengths resulting in colors like blue and green, although the specific colors and sizes vary depending on the exact composition of the QD. Because of their highly tunable properties, QDs are of wide interest. Potential applications include transistors, solar cells, LEDs, diode lasers and second-harmonic generation, quantum computing, and medical imaging.

**Procedure:**

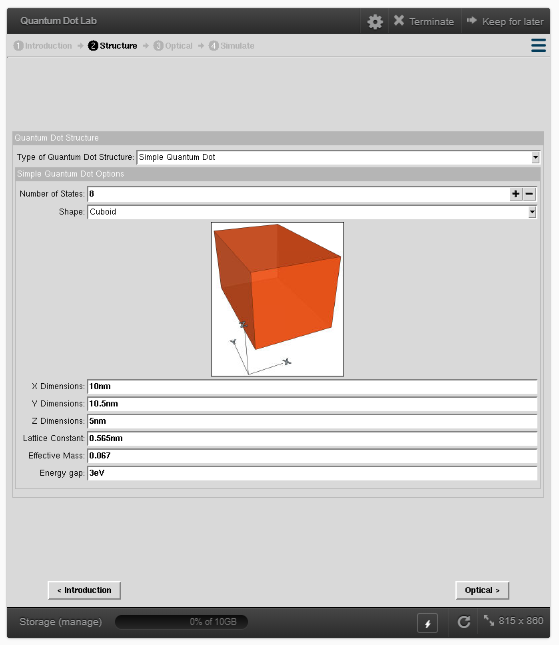
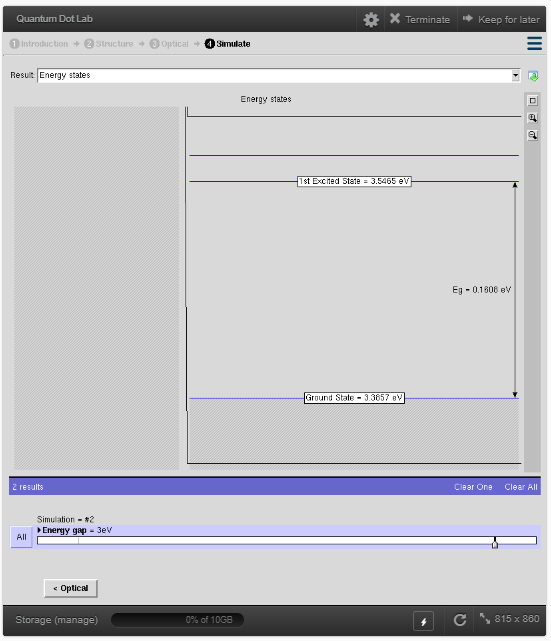
* Open nanoHUB.
* Goto Resources -> Tools.
* Select Quantum Dot in Tags.
* Select Quantum dot -> Quantum dot Lab
* Press Launch tool in info section.
* Select the type of Quantum dot Structure
* Select Energy Bandgap and enter the value
* Press simulate to view results.
* Select Result - > Energy States
* Repeat the above steps for simple and multi-layer quantum dot
* Compare the results of various materials.

**Parameters:**

**Tabulation:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.no** | **Type of Quantum Dot** | **Energy gap (Eg)** | **Energy states** |
| 1 | Simple Quantum Dot |  |  |
|  |
|  |
| 2 | Simple Quantum Dot |  |  |
|  |
|  |
| 3 | Simple Quantum Dot |  |  |
|  |
|  |

**Model Output:**

** **

.

**Result:**

**Simulation Voltage current characteristics of Resonance Tunneling Diode**

**Ex. No: 6**

**Date:**

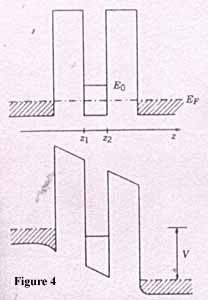
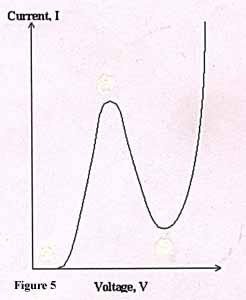
**Aim:**

To obtain the Voltage current characteristics of resonant Tunneling diode (RTD)

**Software:** NanoHub Online Tube

**Theory:**

The use of a barrier to control the flow of electrons from one lead to the other is the basis of transistors. The miniaturization of solid-state devices can’t continue forever. That is, eventually the barriers that are the key to transistor function will be too small to control quantum effects and the electrons will tunnel when the transistor should be off. This is a consequence of the particle-wave duality of electrons, and the single electron characterization of Schrodinger’s equation. At the quantum level the wave nature of the electron will allow the electrons to tunnel through the barriers and create a current. Quantum effects are seen at dimensions less then a micron, but the tunneling effect is expected to be dominant when the critical dimensions approach the wavelength of an electron (approx. 10nm). Ingenious devices exploit the quantum effects of miniature structures to control electrical current. These devices operate by single electron control, and they require that electron movement be confined to two (quantum well), one (quantum wire), or zero (quantum dot) dimensions. In these devices small voltages heat electrons rapidly, inducing complex nonlinear behavior; the study of “hot” electrons, as they are termed, is central to the further development of these devices. Two such devices are the Resonant Tunneling Diode and the Resonant Tunneling Transistor. These devices create a new “switching” mechanism that requires controlled quantum tunneling to function.

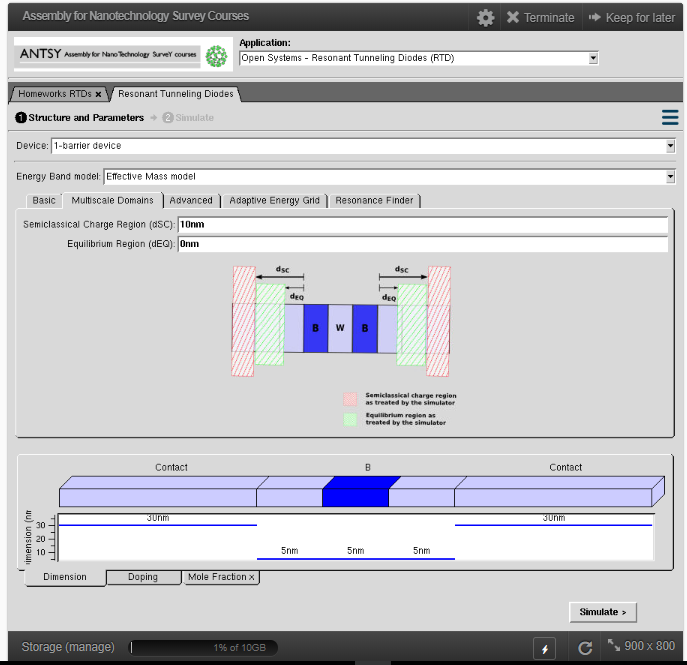
The Resonant Tunneling Diode (RTD) consists of an emitter and a collector separated by two barriers with a quantum well in between these barriers. The quantum well is extremely narrow (5-10nm) and is usually p doped. Resonant tunneling across the double barrier occurs when the energy of the incident electrons in the emitter match that of the unoccupied energy state in the quantum well. An illustration of the double barrier Resonant Tunneling Diode is shown in Figure 4 . When the quantum well energy level is below E0, no current may flow by the tunneling mechanism. When the bias is such that the energy level in the quantum well is aligned with a population of electrons above E0 in the emitter, the electrons may tunnel from the emitter, to the quantum well, and through to the collector. As the voltage is increased, the flow of electrons drops as the electrons are unable to tunnel above the resonant level. As the voltage bias continues to increase, the current begins to increase again, this time as a result of the electrons flowing over the top of the barriers. What results is an S shaped IV curve for the Resonant Tunneling Diode shown in Figure 5 . There are several proposed applications of the resonant tunneling diode. The interesting S shaped IV characteristic makes multistate memory and Logic circuits a possibility. Several resonant tunneling diodes can be combined to form multiple peaks. The implication is that there can be multiple operating points for a circuit. Rather then determining if the memory cell or logic state is a one or a zero, we can determine if it is any number of states. The tunneling diode has not yet been fabricated using Silicon based technology, and the operating temperature of the GaAs devices fabricated is below room temperature. Repeatable control of the size of the quantum well and other structures is not yet realizable with current technologies. These and other manufacturing issues must be resolved before the resonant tunneling diode is a widely used component.

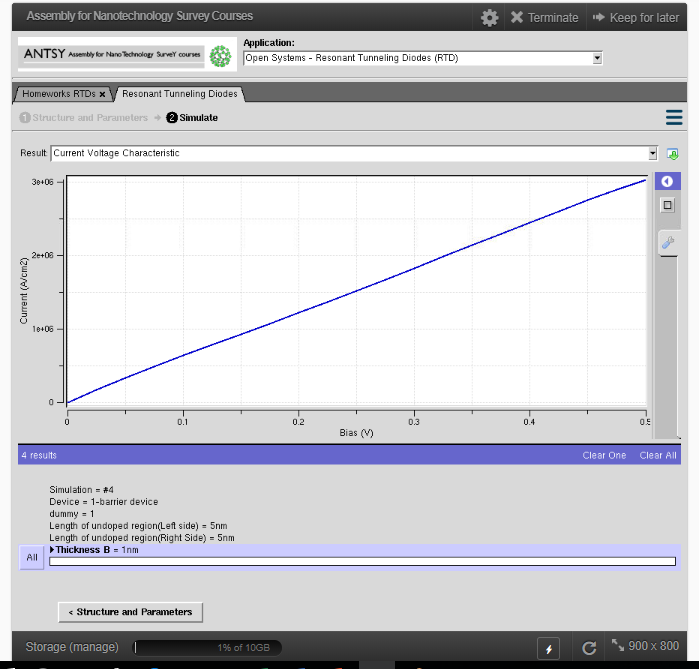
**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select Tunneling in Tags.
* Select Tunneling -> ANTSY
* Press Launch tool in info section.
* Select Applications -> opensource – Resonant tunnelling diode (RTD)
* Select Device -> 1 Barrier
* Press simulate to view results.
* Select Result - > current voltage characteristics
* Select Device ->1 Barrier
* Change the dimension of barrier
* Press simulate to view results.
* Select Device -> 2 Barrier
* Press simulate to view results.
* Select Device -> 2 Barrier
* Change the dimension of barrier
* Press simulate to view results.
* Compare the results of various barriers

**Parameters:**

**Model Output:**

****



1 Barrier Device

**Result:**

**Simulation of V-I characteristics of MOSFET by varying channel length**

**Ex. No: 7**

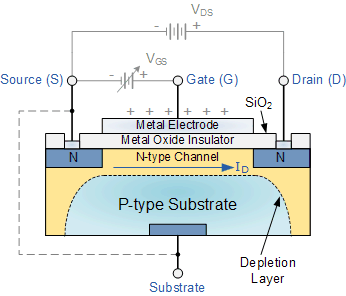
**Date:**

**Aim:**

To Obtain the VI Characteristics of MOSFET by varying Source/Drain Length

**Software:** NanoHub Online Tube

**Theory:**



MOSFET is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the MOSFET extremely high way up in the Mega-ohms ( MΩ ) region thereby making it almost infinite.

As the Gate terminal is electrically isolated from the main current carrying channel between the drain and source, “NO current flows into the gate” and just like the JFET, the MOSFET also acts like a voltage controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the MOSFET becoming easily damaged unless carefully handled or protected.

Like the previous JFET tutorial, MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

Depletion Type – the transistor requires the Gate-Source voltage, ( VGS ) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “Normally Closed” switch.

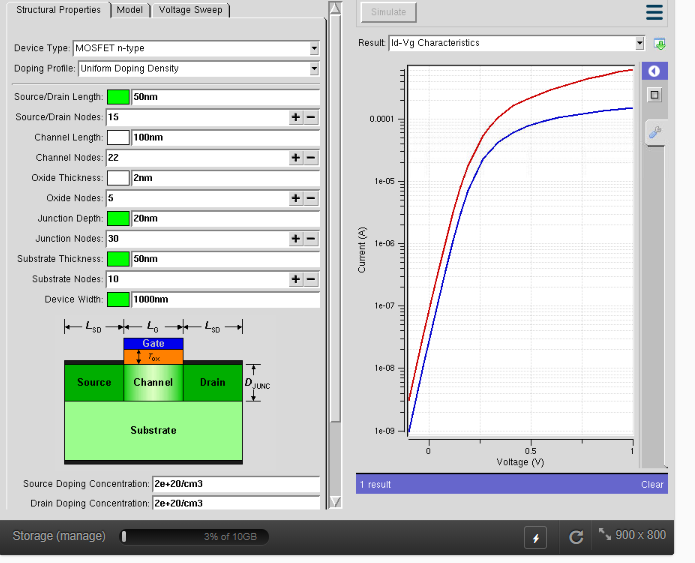
Enhancement Type – the transistor requires a Gate-Source voltage, ( VGS ) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “Normally Open” switch.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select MOSFET ->ABACUS.
* Press Launch tool in info section.
* Select the -> Applications ->MOSFET
* Select Source/Drain Length ->Simulate
* Select ->Result -> VI Characteristics
* Repeat the above steps for various values of Source/Drain Length
* Select ->Applications -> MOSFET
* Select Channel length ->Simulate
* Press simulate to view results.
* Select ->Result -> VI Characteristics
* Repeat the above steps for various values of Source/Drain Length

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of VI Characteristics of MOSFET by varying oxide thickness**

**Ex. No: 8**

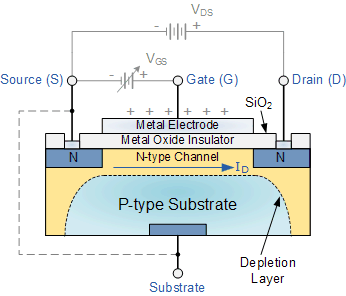
**Date:**

**Aim:**

To Obtain the VI Characteristics of MOSFET by varying Oxide Thickness

**Software:** NanoHub Online Tube

**Theory:**



MOSFET is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the MOSFET extremely high way up in the Mega-ohms ( MΩ ) region thereby making it almost infinite.

As the Gate terminal is electrically isolated from the main current carrying channel between the drain and source, “NO current flows into the gate” and just like the JFET, the MOSFET also acts like a voltage controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the MOSFET becoming easily damaged unless carefully handled or protected.

Like the previous JFET tutorial, MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

Depletion Type – the transistor requires the Gate-Source voltage, ( VGS ) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “Normally Closed” switch.

Enhancement Type – the transistor requires a Gate-Source voltage, ( VGS ) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “Normally Open” switch.

**Procedure:**

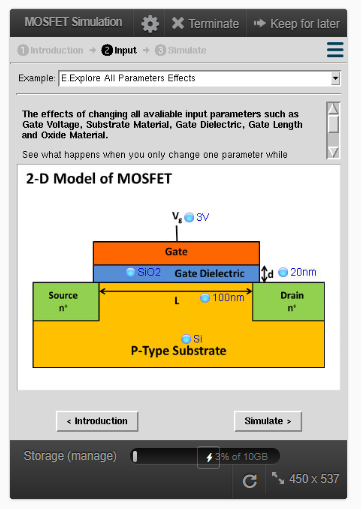
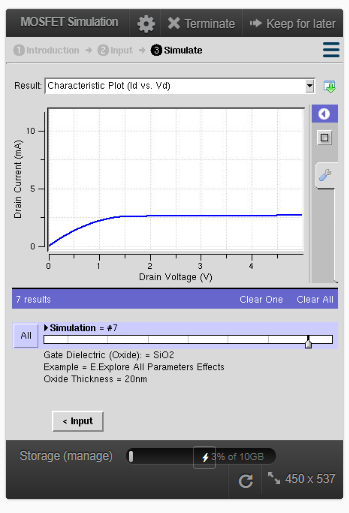
* Open nanoHUB.
* Goto Resources -> Tools.
* Select MOSFET ->MOSFET Simulation.
* Press Launch tool in info section.
* Select the -> Explore -> All Parameter Effects
* Select Oxide thickness ->Simulate
* Select ->Result -> VI Characteristics
* Repeat the above steps for various thickness of Oxide Material

**Parameters:**

**TABULATION:**

|  |  |  |
| --- | --- | --- |
| **S.NO** | **OXIDE THICKNESS (nm)** | **DRAIN CURRENT (mA)** |
| **1** |  |  |
| **2** |  |  |
| **3** |  |  |
| **4** |  |  |
| **5** |  |  |
| **6** |  |  |
| **7** |  |  |
| **8** |  |  |
| **9** |  |  |
| **10** |  |  |

**Model Output:**

** **

**Result:**

**Simulation of VI Characteristics of MOSFET High k-Dielectric Material**

**Ex. No: 9**

**Date:**

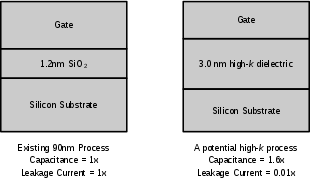
**Aim:**

To Obtain the VI Characteristics of MOSFET by varying High k Dielectric Material

**Software:** NanoHub Online Tube

**Theory:**

The term high-κ dielectric refers to a material with a high dielectric constant κ (as compared to silicon dioxide). High-κ dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a device.



Silicon dioxide (SiO2) has been used as a gate oxide material for decades. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance. As the thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high-κ material allows increased gate capacitance without the associated leakage effects.

Replacing the silicon dioxide gate dielectric with another material adds complexity to the manufacturing process. Silicon dioxide can be formed by oxidizing the underlying silicon, ensuring a uniform, conformal oxide and high interface quality. As a consequence, development efforts have focused on finding a material with a requisitely high dielectric constant that can be easily integrated into a manufacturing process. Other key considerations include band alignment to silicon (which may alter leakage current), film morphology, thermal stability, maintenance of a high mobility of charge carriers in the channel and minimization of electrical defects in the film/interface. Materials which have received considerable attention are hafnium silicate, zirconium silicate, hafnium dioxide and zirconium dioxide, typically deposited using atomic layer deposition.

**Procedure:**

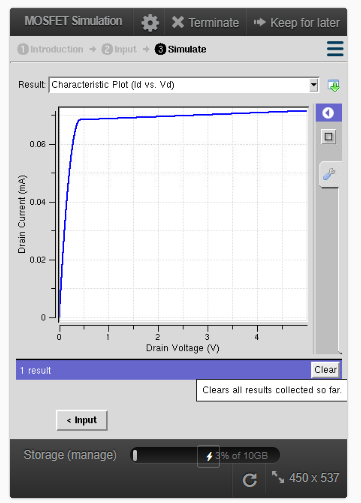
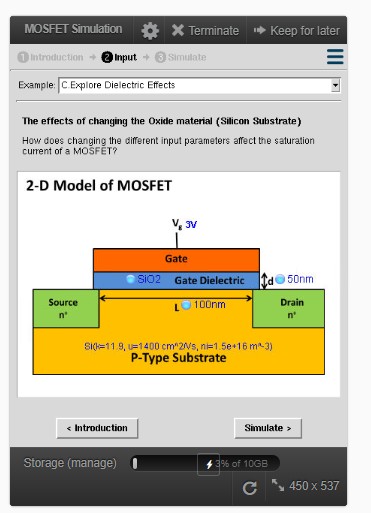
* Open nanoHUB.
* Goto Resources -> Tools.
* Select MOSFET ->MOSFET Simulation.
* Press Launch tool in info section.
* Select the -> Explore -> Dielectric Effects
* Select Dielectric material ->Simulate
* Select ->Result -> VI Characteristics
* Repeat the above steps for various high k dielectric material

**Parameters:**

**TABULATION:**

|  |  |  |
| --- | --- | --- |
| **S.NO** | **DIELECTRIC MATERIAL** | **CURRENT (Ma)** |
| **1** |  |  |
| **2** |  |  |
| **3** |  |  |
| **4** |  |  |

**Model Output:**

****

**Result:**

**Simulation of VI Characteristics of Double gate MOSFET**

**Ex. No: 10**

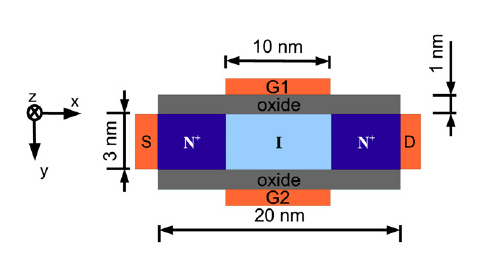
**Date:**

**Aim:**

To Obtain the VI Characteristics of DOUBLE GATE MOSFET by varying Source/Drain Length

**Software:** NanoHub Online Tube

**Theory:**



The dual gate MOSFET is used in many RF and other applications where two control gates are required in series.

The dual gate MOSFET is essentially a form of MOSFET where two gates are fabricated along the length of the channel - one after the other. In this way, both gates affect the level of current flowing between the source and drain.

The dual gate MOSFET has what may be referred to as a tetrode construction where the two grids control the current through the channel.

The different gates control different sections of the channel which are in series with each other.

The double-gate control of silicon-on-insulator (SOI) transistors was used to force the whole silicon film (interface layers and volume) in strong inversion (called “Volume-Inversion MOSFET”) or strong accumulation (called “Volume-Accumulation MOSFET”). This original method of transistor operation, at the origin of the unique electrostatic properties and scalability of multigate devices, offered excellent device performance, in particular, great increases in subthreshold slope, transconductance, and drain current. A simulation program and experiments on SIMOX structures was used to study this new type of device.

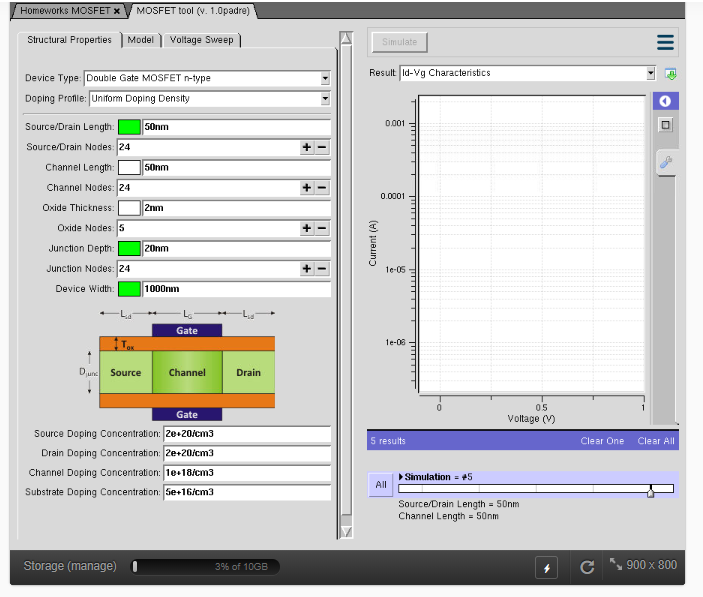
Planar double-gate transistors employ conventional planar (layer by layer) manufacturing processes to create double-gate devices, avoiding more stringent lithography requirements associated with non-planar, vertical transistor structures. In planar double-gate transistors the drain–source channel is sandwiched between two independently fabricated gate/gate-oxide stacks. The primary challenge in fabricating such structures is achieving satisfactory self-alignment between the upper and lower gates

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select MOSFET ->ABACUS.
* Press Launch tool in info section.
* Select the -> Applications ->MOSFET
* Select Device type -> Double gate MOSFET n channel
* Select Source/Drain Length ->Simulate
* Select ->Result -> VI Characteristics
* Repeat the above steps for various values of Source/Drain Length
* Select ->Applications -> MOSFET
* Select Device type -> Double gate MOSFET n channel
* Select Channel length ->Simulate
* Press simulate to view results.
* Select ->Result -> VI Characteristics
* Repeat the above steps for various values of Source/Drain Length

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of VI Characteristics of FinFET by varying the Channel Width and oxide thickness**

**Ex. No: 11**

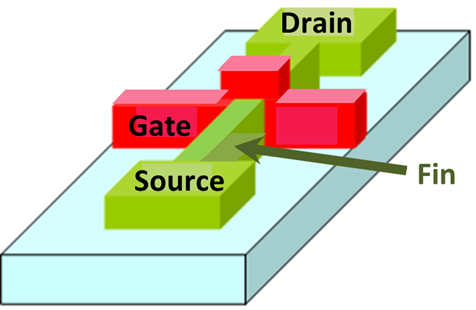
**Date:**

**Aim:**

To Obtain the VI Characteristics of FinFET by varying the Channel Width and oxide thickness

**Software:** NanoHub Online Tube

**Theory:**



FinFET technology takes its name from the fact that the FET structure used looks like a set of fins when viewed.

The main characteristic of the FinFET is that it has a conducting channel wrapped by a thin silicon "fin" from which it gains its name. The thickness of the fin determines the effective channel length of the device.

In terms of its structure, it typically has a vertical fin on a substrate which runs between a larger drain and source area. This protrudes vertically above the substrate as a fin.

The gate orientation is at right angles to the vertical fin. And to traverse from one side of the fin to the other it wraps over the fin, enabling it to interface with three side of the fin or channel.

This form of gate structure provides improved electrical control over the channel conduction and it helps reduce leakage current levels and overcomes some other short-channel effects.

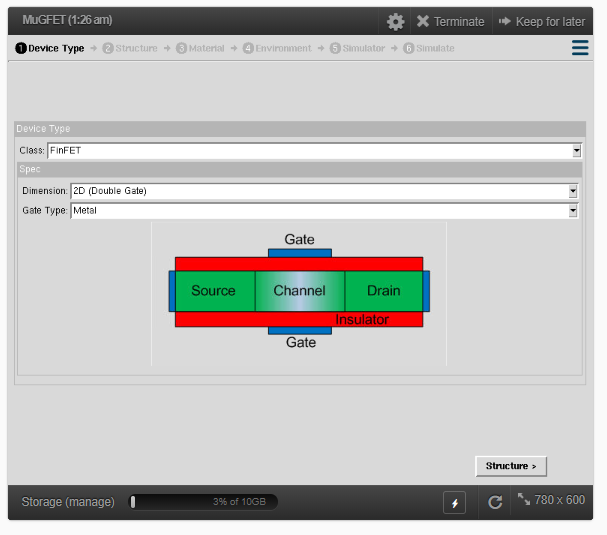
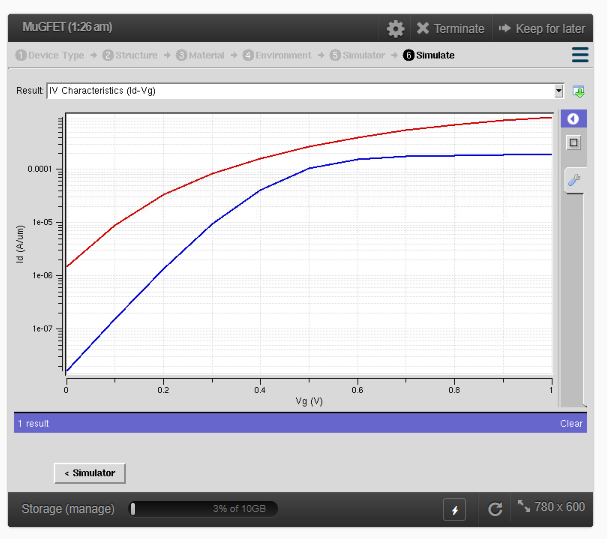
The term FinFET is used somewhat generically. Sometimes it is used to describe any fin-based, multigate transistor architecture regardless of number of gates.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select FinFET -> MuGFET
* Press Launch tool in info section.
* Select the -> class -> FinFET
* Select Channel Width -> Simulate
* Select ->Result -> VI Characteristics
* Repeat the above steps for various values of Channel Width
* Select Oxide thickness -> Simulate
* Select ->Result -> VI Characteristics
* Repeat the above steps for various values of Oxide Thickness

**Parameters:**

**Model Output:**

** **

**Result:**

**Simulation of the equivalent circuit of Single Electron Transistor**

**Ex. No: 12**

**Date:**

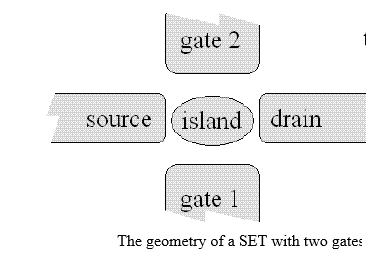
**Aim:**

To simulate the equivalent circuit of Single Electron Transistor

**Software:** Electronic Workbench

**Theory:**

**Single-electron transistors (SET's)** are often discussed as elements of nanometer scale electronic circuits because they can be made very small and they can detect the motion of individual electrons. However, SET's have low voltage gain, high output impedances, and are sensitive to random background charges. This makes it unlikely that single-electron transistors would ever replace field-effect transistors (FET's) in applications where large voltage gain or low output impedance is necessary. The most promising applications for SET's are charge-sensing applications such as the readout of few electron memories, the readout of charge-coupled devices, and precision charge measurements in metrology



A single-electron transistor consists of a small conducting island coupled to source and drain leads by tunnel junctions and capacitively coupled to one or more gates. The geometry of a SET is shown in Fig. 1(a) and the equivalent electrical circuit is shown in Fig. 1(b). A stray capacitance *C*0 from the island to ground and a random background charge on the island *Q*0 are also included in the model. There are two gates in the equivalent circuit because two gates are often used in practice. For example, one gate can be used to tune the background charge while the other is used as the input of the SET. A straightforward electrostatic calculation shows that the voltage of the island as a function of the number of electrons on the island is,

*V*(*n*) = (-*ne* + *Q*0 + *C*1*V*1 + *C*2*V*2 + *C*g1*V*g1 +*C*g2*V*g2)/*C*Σ.

Here *n* is the number of electrons on the island, *e* is the positive elementary charge, and *C*Σ is the total capacitance of the island *C*Σ = *C*1 + *C*2 + *C*g1 +*C*g2 +*C*0. The energy it takes to move an infinitesimally small charge *dq* from ground at a potential *V* = 0 to the island is *Vdq*. As soon as charge is added to the island, the voltage of the island changes.

**Procedure:**

* Open Electronic workbench
* Connect the circuit as per the circuit diagram
* Note the voltages of V1, V2, Vg1 and Vg2

**Parameters:**

**R1 =**

**R2  =**

**C1 =**

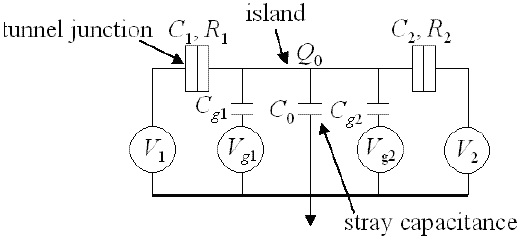
**C2 =**

**Cg1 =**

**Cg2 =**

**C0 =**

**Circuit Diagram:**

****

**Tabulation:**

|  |  |  |  |
| --- | --- | --- | --- |
| **V1** | **V2** | **Vg1** | **Vg2** |
|  |  |  |  |

**Result:**

**Simulation of VI Characteristics of Coulomb Blockade**

**Ex. No: 13**

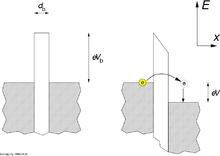
**Date:**

**Aim:**

To Obtain the VI Characteristics of coulomb blockade for single and double quantum dot

**Software:** NanoHub Online Tube

**Theory:**



Single electron devices differ from conventional devices in the sense that the electronic transport is governed by quantum mechanics. Single electron devices consist of an ‘island’, a region containing localized electrons isolated by tunnel junctions with barriers to electron tunneling. In this section, we discuss the electron transport through such devices and how Coulomb blockade originates in these devices

The energy that determines the transport of electrons through a single-electron device is Helmholtz's free energy, F, which is defined as difference between total energy, ,stored in the device and work done by power sources, W. The total energy stored includes all components that have to be considered when charging an island with an electron.



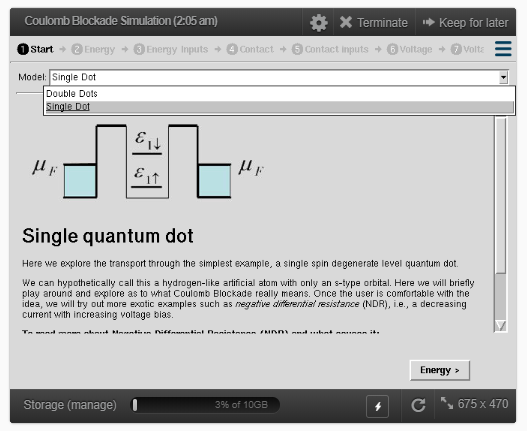
The change in Helmholtz's free energy a tunnel event causes is a measure of the probability of this tunnel event. The general fact that physical systems tend to occupy lower energy states, is apparent in electrons favouring those tunnel events which reduce the free energy

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select Coulomb blockade ->Coulomb blockade simulation
* Press Launch tool in info section.
* Select the -> model -> single dot
* Select -> Simulate
* Select ->Result -> VI Characteristics
* Select the -> model -> Double dot
* Select -> Simulate
* Select ->Result -> VI Characteristics

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of electrical properties of Carbon Nanotube based on chiral vector (n,m)**

**Ex. No: 14**

**Date:**

**Aim:**

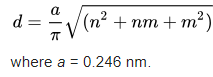
To find the electrical properties of Carbon Nanotube based on chiral vector (n,m)

**Software:** NanoHub Online Tube

**Theory:**



Carbon nanotubes (CNTs) are allotropes of carbon with a cylindrical nanostructure. These cylindrical carbon molecules have unusual properties, which are valuable for nanotechnology, electronics, optics and other fields of materials science and technology. Owing to the material's exceptional strength and stiffness, nanotubes have been constructed with length-to-diameter ratio of up to 132,000,000:1. For a given (n,m) nanotube, if n = m, the nanotube is metallic; if n − m is a multiple of 3 and n ≠ m and nm ≠ 0, then the nanotube is quasi-metallic with a very small band gap, otherwise the nanotube is a moderate semiconductor. Thus all armchair (n = m) nanotubes are metallic, and nanotubes (6,4), (9,1), etc. are semiconducting. The diameter of CNT can be given as:



The angle of CNT is given by

****

**Procedure:**

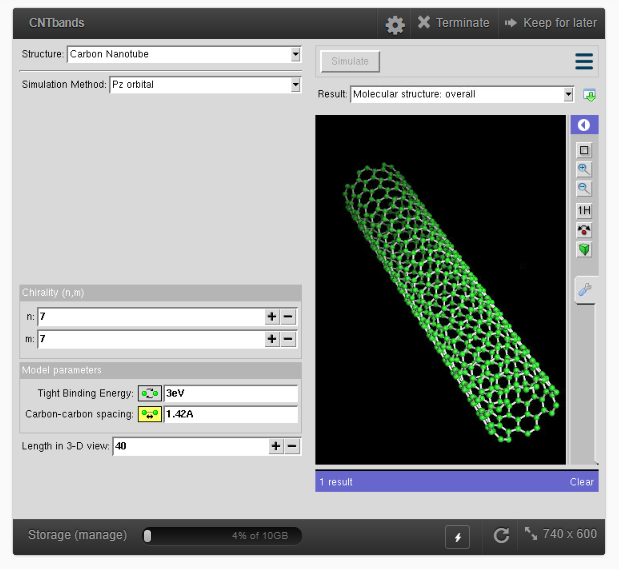
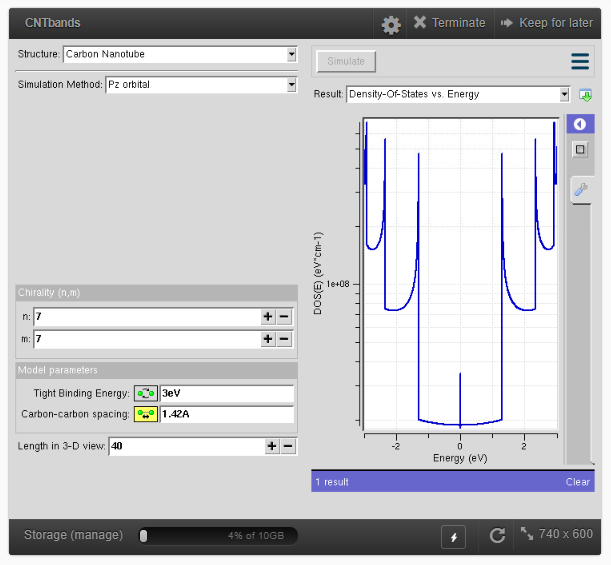
* Open nanoHUB.
* Goto Resources -> Tools.
* Select Carbonnanotube -> CNT Bands
* Press Launch tool in info section.
* Select the -> Structure - > Carbon Nanotube
* Select n and m value
* Click on Simulation
* Select ->Result -> Molecular structure
* Select -> Result -> Density of states
* Repeat the above steps for various values of Source/Drain Length

**Parameters:**

**Tabulation:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S.NO** | **Chiral Vector (n,m)** | **Type of CNT**  **(Electrical Property)** | **Diameter of CNT** | **Angle of rotation** |
| 1 | (5,5) |  |  |  |
| 2 | (5,0) |  |  |  |
| 3 | (0,5) |  |  |  |
| 4 | (7,5) |  |  |  |
| 5 | (7,2) |  |  |  |

**Model Output:**

** **

CNT Structure CNT Density of States

**Result:**

**Simulation of density of states and conductance mobility of electrons in CNTFET**

**Ex. No: 15**

**Date:**

**Aim:**

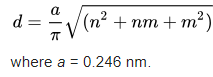
To Obtain the density of states and conductance of CNTFET by varying the diameter and length.

**Software:** NanoHub Online Tube

**Theory:**



Carbon nanotubes (CNTs) are allotropes of carbon with a cylindrical nanostructure. These cylindrical carbon molecules have unusual properties, which are valuable for nanotechnology, electronics, optics and other fields of materials science and technology. Owing to the material's exceptional strength and stiffness, nanotubes have been constructed with length-to-diameter ratio of up to 132,000,000:1. For a given (n,m) nanotube, if n = m, the nanotube is metallic; if n − m is a multiple of 3 and n ≠ m and nm ≠ 0, then the nanotube is quasi-metallic with a very small band gap, otherwise the nanotube is a moderate semiconductor. Thus all armchair (n = m) nanotubes are metallic, and nanotubes (6,4), (9,1), etc. are semiconducting. The diameter of CNT can be given as:



The angle of CNT is given by

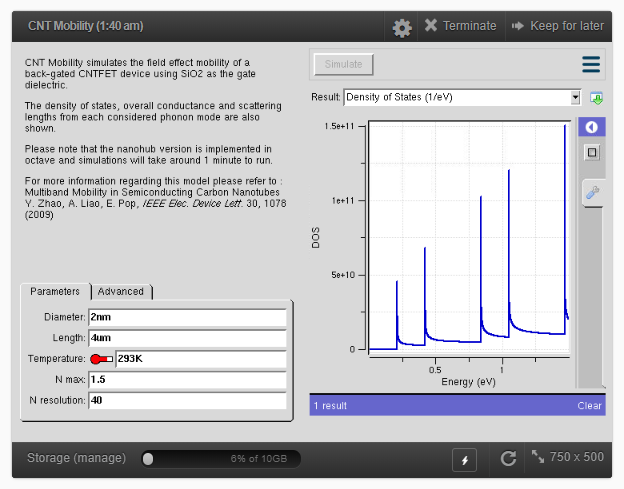
****

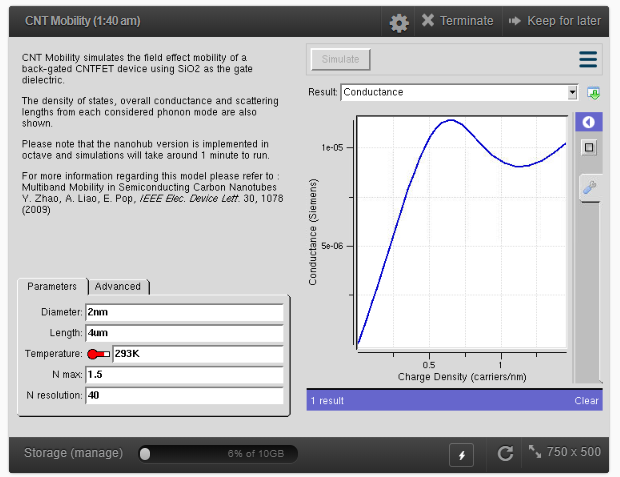
**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select CNTFET ->CNT Mobility
* Press Launch tool in info section.
* Select the -> diameter of CNT
* Select -> Simulate
* Select ->Result -> conductance
* Select ->Result -> Density of states
* Repeat the above for various diameter
* Select the -> Length of CNT
* Select -> Simulate
* Select ->Result -> conductance
* Select ->Result -> Density of states

**Parameters:**

**Model Output:**





**Result:**

**Simulation of VI characterstics of Schottky barrier CNFET**

**Ex. No: 16**

**Date:**

**Aim:**

To obtain VI characterstics of CNFET by varying schottky barrier and oxide thickness

**Software:** NanoHub Online Tube

**Theory:**

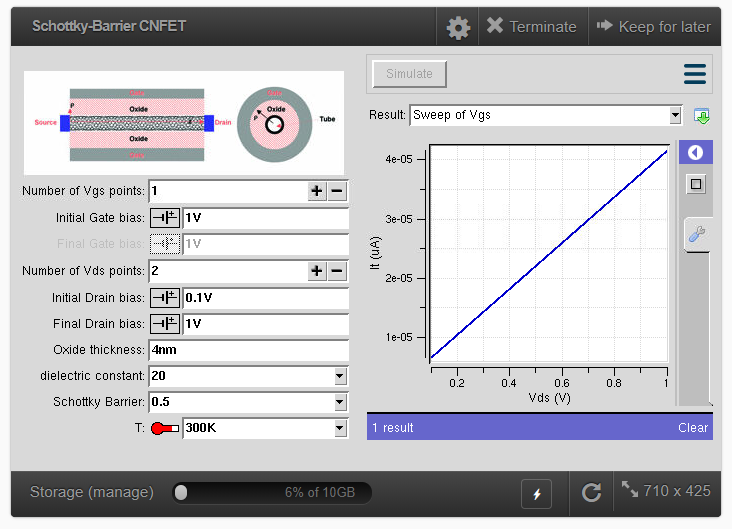
The barrier between a metal and a semiconductor is predicted by the Schottky-Mott rule to be proportional to the difference of the metal-vacuum work function and the semiconductor-vacuum electron affinity. In practice, however, most metal-semiconductor interfaces do not follow this rule to the predicted degree. Instead, the chemical termination of the semiconductor crystal against a metal creates electron states within its band gap. The nature of these metal-induced gap states and their occupation by electrons tends to pin the center of the band gap to the Fermi level, an effect known as Fermi level pinning. Thus the heights of the Schottky barriers in metal-semiconductor contacts often show little dependence on the value of the semiconductor or metal work functions, in strong contrast to the Schottky-Mott rule. Different semiconductors exhibit this Fermi level pinning to different degrees, but a technological consequence is that ohmic contacts are usually difficult to form in important semiconductors such as silicon and gallium arsenide. Non-ohmic contacts present a parasitic resistance to current flow that consumes energy and lowers device performance.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select carbon nanotubes -> schottky barrier CNFET
* Press Launch tool in info section.
* Select the -> Schottky barrier - > Enter the value of bandgap
* Click on Simulation
* Select ->Result -> VI characterstics
* Repeat the above steps for various bandgap
* Select the -> oxide thickness -> enter the thickness
* Click on Simulation
* Select ->Result -> VI characterstics
* Repeat the above steps for various thickness

**Parameters:**

**Model Output:**



**Result:**

**Simulation of the temperature distribution on a moving substrate material prior to plasma treatment in a roll – to – roll plasma CVD system**

**Ex. No: 17**

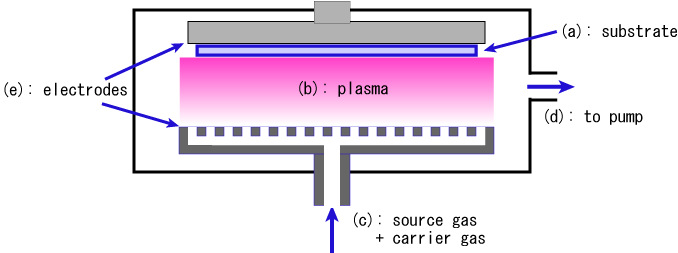
**Date:**

**Aim:**

To obtain the temperature distribution on a moving substrate material prior to plasma treatment in a roll – to – roll plasma CVD system

**Software:** NanoHub Online Tube

**Theory:**



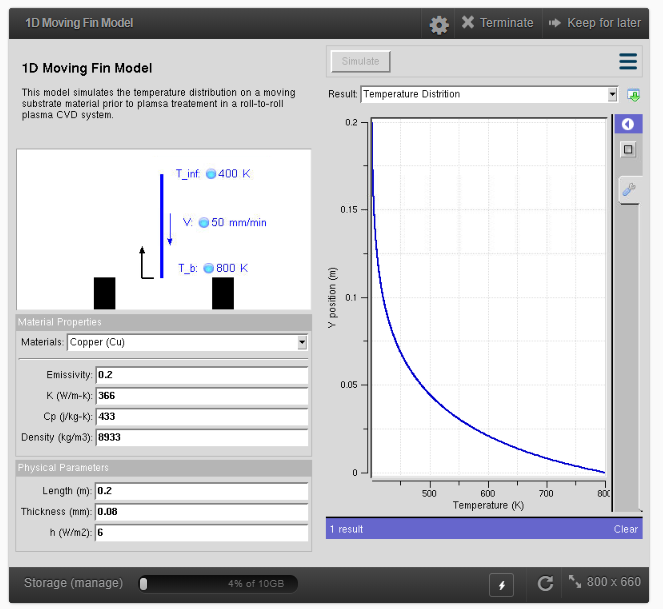
Chemical vapor deposition (CVD) is deposition method used to produce high quality, high-performance, solid materials, typically under vacuum. The process is often used in the semiconductor industry to produce thin films. Microfabrication processes widely use CVD to deposit materials in various forms, including: monocrystalline, polycrystalline, amorphous, and epitaxial. These materials include: silicon ([[Silicon dioxide|SiO carbide, nitride, oxynitride), carbon (fiber, nanofibers, nanotubes, diamond and graphene), fluorocarbons, filaments, tungsten, titanium nitride and various high-k dielectrics.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select CVD -> 1D Fin Model
* Press Launch tool in info section.
* Select the -> Material - > Copper
* Click on Simulation
* Select ->Result -> temperature distribution
* Repeat the above steps for various materials of length and thickness

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of VI Characteristics of CNTFET by varying channel length**

**Ex. No: 18**

**Date:**

**Aim:**

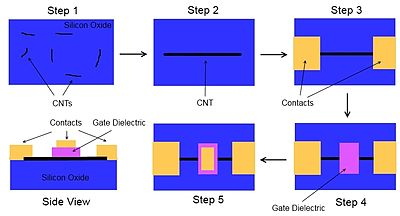
To obtain the VI Characteristics of CNTFET by varying the channel length

**Software:** NanoHub Online Tube

**Theory:**

**Top-gated CNTFETs:**

Single-walled carbon nanotubes are solution deposited onto a silicon oxide substrate. Individual nanotubes are then located via atomic force microscope or scanning electron microscope. After an individual tube is isolated, source and drain contacts are defined and patterned using high resolution electron beam lithography. A high temperature anneal step reduces the contact resistance by improving adhesion between the contacts and CNT. A thin top-gate dielectric is then deposited on top of the nanotube, either via evaporation or atomic layer deposition. Finally, the top gate contact is deposited on the gate dielectric, completing the process.



Arrays of top-gated CNTFETs can be fabricated on the same wafer, since the gate contacts are electrically isolated from each other, unlike in the back-gated case. Also, due to the thinness of the gate dielectric, a larger electric field can be generated with respect to the nanotube using a lower gate voltage. These advantages mean top-gated devices are generally preferred over back-gated CNTFETs, despite their more complex fabrication process.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select CNTFET -> CNT MOSFET LAB
* Press Launch tool in info section.
* Select the -> Channel Length
* Click on Simulation
* Select ->Result -> Ids vs Vds
* Repeat the above steps for various channel length

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of VI Characteristics of CNTFET by varying cnt diameter**

**Ex. No: 19**

**Date:**

**Aim:**

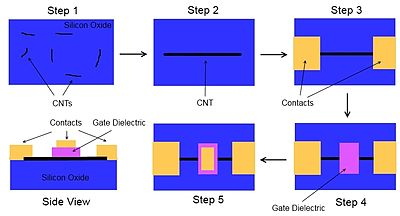
To obtain the VI Characteristics of CNTFET by varying the CNT diameter

**Software:** NanoHub Online Tube

**Theory:**

**Top-gated CNTFETs:**

Single-walled carbon nanotubes are solution deposited onto a silicon oxide substrate. Individual nanotubes are then located via atomic force microscope or scanning electron microscope. After an individual tube is isolated, source and drain contacts are defined and patterned using high resolution electron beam lithography. A high temperature anneal step reduces the contact resistance by improving adhesion between the contacts and CNT. A thin top-gate dielectric is then deposited on top of the nanotube, either via evaporation or atomic layer deposition. Finally, the top gate contact is deposited on the gate dielectric, completing the process.



Arrays of top-gated CNTFETs can be fabricated on the same wafer, since the gate contacts are electrically isolated from each other, unlike in the back-gated case. Also, due to the thinness of the gate dielectric, a larger electric field can be generated with respect to the nanotube using a lower gate voltage. These advantages mean top-gated devices are generally preferred over back-gated CNTFETs, despite their more complex fabrication process.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select CNTFET -> CNT MOSFET LAB
* Press Launch tool in info section.
* Select the -> CNT Diameter
* Click on Simulation
* Select ->Result -> Ids vs Vds
* Repeat the above steps for various CNT Diameter

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of Band structure and Density of States of Graphene by varying chiral vector**

**Ex. No: 20**

**Date:**

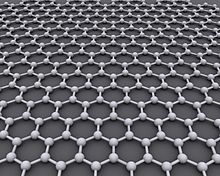
**Aim:**

To find the Band structure and Density of States of graphene by varying chiral vector

**Software:** NanoHub Online Tube

**Theory:**

Graphene is a semi-metal with small overlap between the valence and the conduction bands (zero bandgap material). It is an allotrope (form) of carbon consisting of a single layer of carbon atoms arranged in a hexagonal lattice. It is the basic structural element of many other allotropes of carbon, such as graphite, diamond, charcoal, carbon nanotubes and fullerenes.



Graphene is a zero-gap semiconductor, because its conduction and valence bands meet at the Dirac points, which are six locations in momentum space, on the edge of the Brillouin zone, divided into two non-equivalent sets of three points. The two sets are labeled K and K'. The sets give graphene a valley degeneracy of gv = 2. By contrast, for traditional semiconductors the primary point of interest is generally Γ, where momentum is zero. However, if the in-plane direction is confined, in which case it is referred to as a nanoribbon, its electronic structure is different. If it is "zig-zag", the bandgap is zero. If it is "armchair", the bandgap is non-zero. The corresponding resistivity of graphene sheets would be 10−6 Ω⋅cm. This is less than the resistivity of silver, the lowest otherwise known at room temperature

**Procedure:**

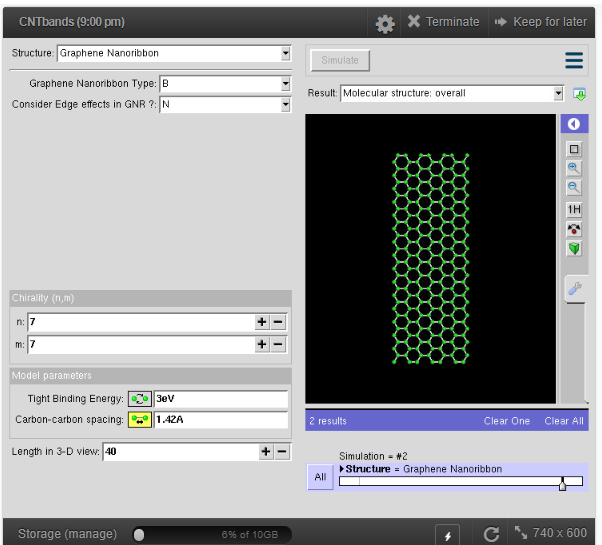
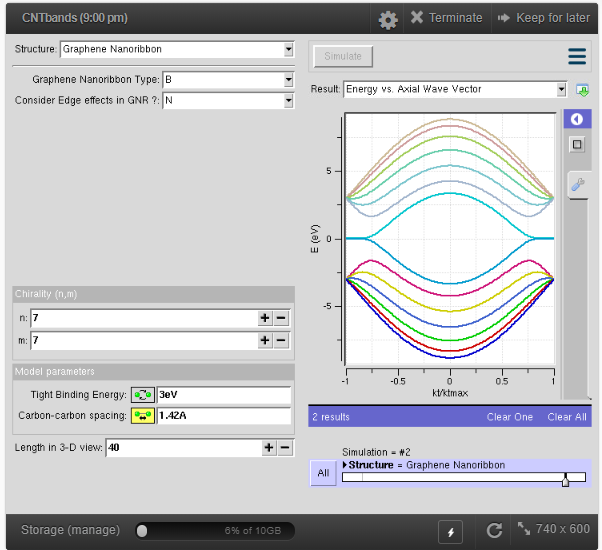
* Open nanoHUB.
* Goto Resources -> Tools.
* Select Carbonnanotube -> CNT Bands
* Press Launch tool in info section.
* Select the -> Structure - > Graphene Nanoribbons
* Select n and m value
* Click on Simulation
* Select ->Result -> Molecular structure
* Select -> Result -> Density of states
* Select -> Result -> Energy vs axial wave vector
* Repeat the above steps for various values of Source/Drain Length

**Parameters:**

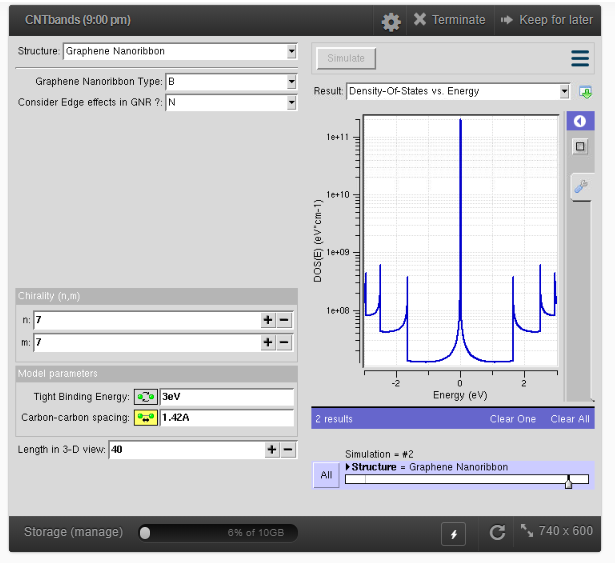
**Tabulation:**

|  |  |  |
| --- | --- | --- |
| **S.NO** | **Chiral Vector (n,m)** | **Type of Graphene**  **(Electrical Property)** |
| 1 | (5,5) |  |
| 2 | (5,0) |  |
| 3 | (0,5) |  |
| 4 | (7,5) |  |
| 5 | (7,2) |  |

**Model Output:**

** **

Graphene Structure Graphene Energy vs Axial wave Vector



Graphene Density of States

**Result:**

**Simulation of VI characterstics of Graphene field effect transistor**

**Ex. No: 21**

**Date:**

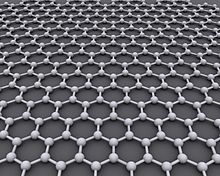
**Aim:**

To obtain the VI Characteristics of Graphene Field Effect Transistor

**Software:** NanoHub Online Tube

**Theory:**

Graphene is a semi-metal with small overlap between the valence and the conduction bands (zero bandgap material). It is an allotrope (form) of carbon consisting of a single layer of carbon atoms arranged in a hexagonal lattice. It is the basic structural element of many other allotropes of carbon, such as graphite, diamond, charcoal, carbon nanotubes and fullerenes.



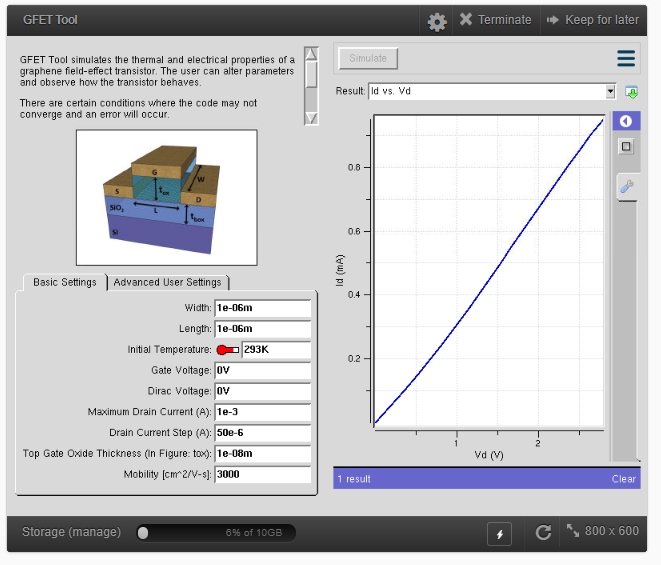
Graphene is a zero-gap semiconductor, because its conduction and valence bands meet at the Dirac points, which are six locations in momentum space, on the edge of the Brillouin zone, divided into two non-equivalent sets of three points. The two sets are labeled K and K'. The sets give graphene a valley degeneracy of gv = 2. By contrast, for traditional semiconductors the primary point of interest is generally Γ, where momentum is zero. However, if the in-plane direction is confined, in which case it is referred to as a nanoribbon, its electronic structure is different. If it is "zig-zag", the bandgap is zero. If it is "armchair", the bandgap is non-zero. The corresponding resistivity of graphene sheets would be 10−6 Ω⋅cm. This is less than the resistivity of silver, the lowest otherwise known at room temperature

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select Graphene -> GFET
* Press Launch tool in info section.
* Select the -> Width
* Click on Simulation
* Select ->Result -> Ids vs Vds
* Repeat the above steps for various width
* Select -> Length
* Select ->Result -> Ids vs Vds
* Repeat the above steps for various width

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of absorption spectra of nanomagnetic particles by varying the size.**

**Ex. No: 22**

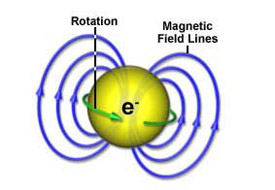
**Date:**

**Aim:**

To obtain the absorption spectra of nanomagnetic particles by varying the size.

**Software:** NanoHub Online Tube

**Theory:**



EMR stands for electron magnetic resonance. EMR is very similar to the two other resonance techniques that take place here at the lab: nuclear magnetic resonance (NMR) and ion cyclotron resonance (ICR). The big difference is that EMR looks at electrons rather than nuclei (which is the case in NMR) or ions (in the case of ICR).

There are several forms of EMR, including electron paramagnetic resonance (EPR), electron spin resonance (ESR) and electron cyclotron resonance (ECR).

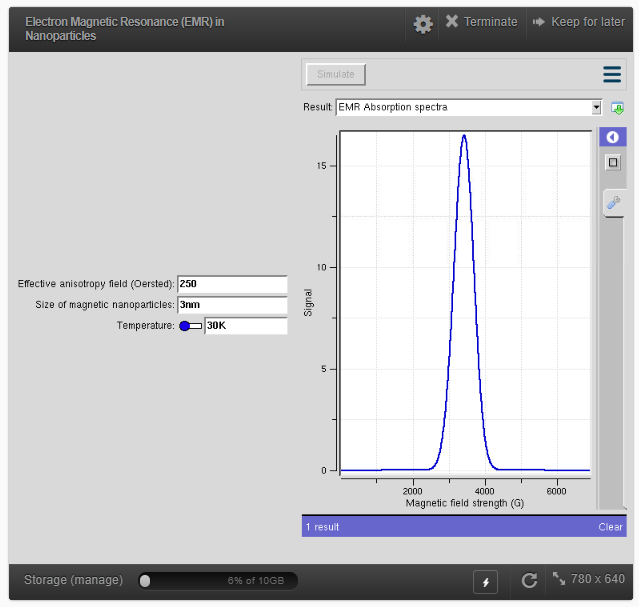
The big difference between ESR and NMR is that nature actually likes to pair up electrons (this also happens in nuclei, but not to the same extent). For the vast majority of materials, the electrons pair up so that one of them has its spin pointing one way, and the other has its spin pointing in the opposite direction. In other words, for every tiny magnet pointing one way, there is another pointing in the opposite direction. As a result, the substance has no net spin and no magnetism. In this situation, you cannot do an ESR or EPR experiment.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select Electron magnetic resonance
* Press Launch tool in info section.
* Select the -> Size of the magnetic nanoparticle
* Click on Simulation
* Select ->Result -> Absorption spectra

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of Tunnelling Magneto resistance (TMR) by varying oxide thickness and voltage of magnetic tunnel junction**

**Ex. No: 23**

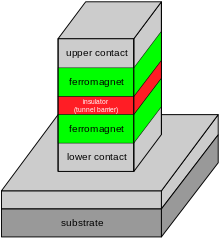
**Date:**

**Aim:**

To obtain the Tunnelling Magneto resistance (TMR) by varying oxide thickness and voltage.

**Software:** NanoHub Online Tube

**Theory:**



Tunnel magnetoresistance (TMR) is a magneto resistive effect that occurs in a magnetic tunnel junction (MTJ), which is a component consisting of two ferromagnets separated by a thin insulator. If the insulating layer is thin enough (typically a few nanometres), electrons can tunnel from one ferromagnet into the other. Since this process is forbidden in classical physics, the tunnel magnetoresistance is a strictly quantum mechanical phenomenon.

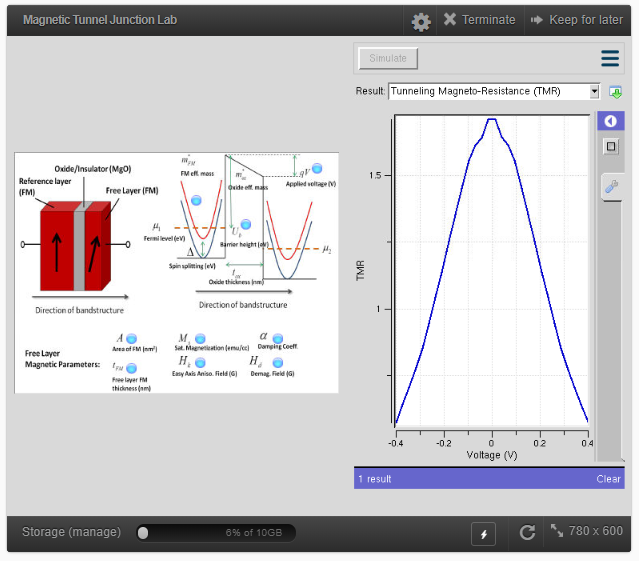
Magnetic tunnel junctions are manufactured in thin film technology. On an industrial scale the film deposition is done by magnetron sputter deposition; on a laboratory scale molecular beam epitaxy, pulsed laser deposition and electron beam physical vapor deposition are also utilized. The junctions are prepared by photolithography.

**Procedure:**

* Open nanoHUB and goto Resources -> Tools.
* Select Magnetic Tunnel Junction Lab
* Press Launch tool in info section.
* Select the -> Oxide thickness
* Click on Simulation
* Select ->Result -> Tunnel magnetoresistance (TMR)
* Repeat the above steps for various oxide thickness
* Select -> voltage
* Select ->Result -> Tunnel magnetoresistance (TMR)
* Repeat the above steps for various voltage

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of I-V Characteristics of memristor by varying the device thickness and voltage**

**Ex. No: 24**

**Date:**

**Aim:**

To obtain the I-V Characteristics of memristor by varying the device thickness and voltage

**Software:** NanoHub Online Tube

**Theory:**

A memristor is an electrical component that limits or regulates the flow of electrical current in a circuit and remembers the amount of charge that has previously flowed through it. Memristors are important because they are non-volatile, meaning that they retain memory without power.

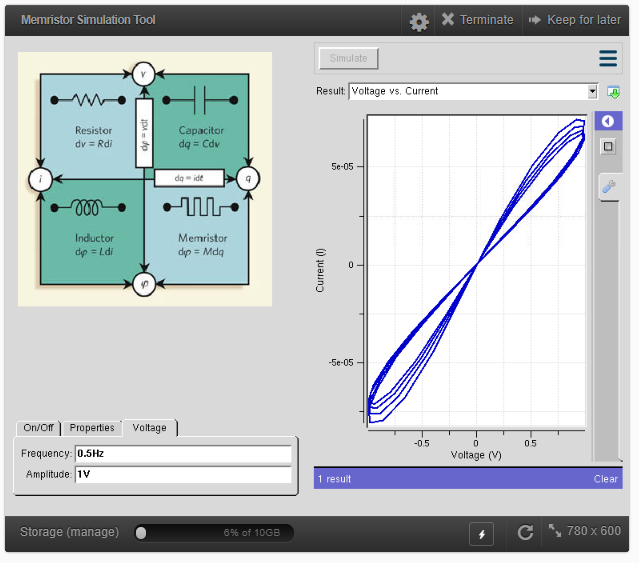


**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select memristor
* Press Launch tool in info section.
* Select the -> Device thickness
* Click on Simulation
* Select ->Result -> voltage – current characteristics
* Repeat the above steps for various device thickness
* Select -> voltage
* Select ->Result -> voltage – current characteristics
* Repeat the above steps for various voltage

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of band structure and density of states of magnetic tunnel junction by varying barrier height**

**Ex. No: 25**

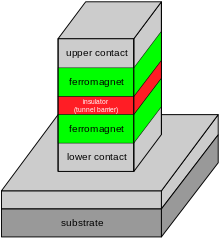
**Date:**

**Aim:**

To obtain the Tunnelling Magneto resistance (TMR) by varying barrier height.

**Software:** NanoHub Online Tube

**Theory:**



Tunnel magnetoresistance (TMR) is a magneto resistive effect that occurs in a magnetic tunnel junction (MTJ), which is a component consisting of two ferromagnets separated by a thin insulator. If the insulating layer is thin enough (typically a few nanometres), electrons can tunnel from one ferromagnet into the other. Since this process is forbidden in classical physics, the tunnel magnetoresistance is a strictly quantum mechanical phenomenon.

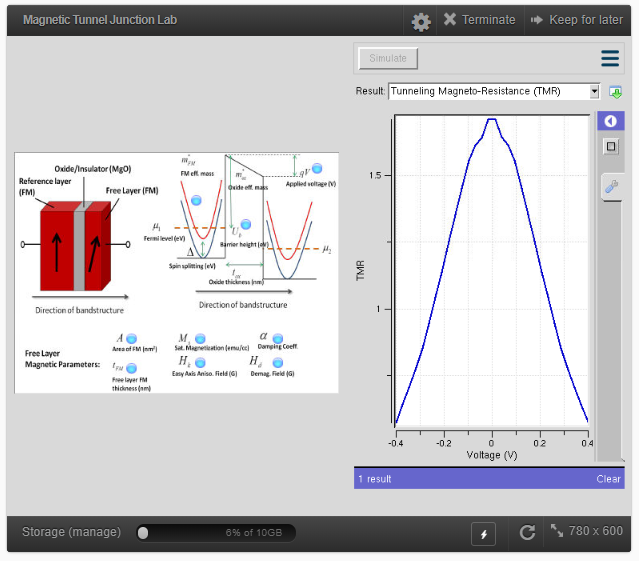
Magnetic tunnel junctions are manufactured in thin film technology. On an industrial scale the film deposition is done by magnetron sputter deposition; on a laboratory scale molecular beam epitaxy, pulsed laser deposition and electron beam physical vapor deposition are also utilized. The junctions are prepared by photolithography.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select Magnetic Tunnel Junction Lab
* Press Launch tool in info section.
* Select the -> barrier height
* Click on Simulation
* Select ->Result -> Tunnel magnetoresistance (TMR)
* Repeat the above steps for various barrier height

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of Potential of a sensor by varying the pH value of an electrolyte and insulator thickness of biosensor**

**Ex. No: 26**

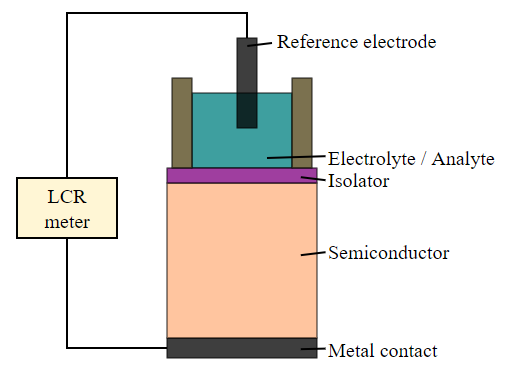
**Date:**

**Aim:**

To obtain the Potential of a sensor by varying the pH value of an electrolyte and insulator thickness

**Software:** NanoHub Online Tube

**Theory:**

****

An Electrolyte–insulator–semiconductor (EIS) sensor is a sensor that is made of these three components:

* an electrolyte with the chemical that should be measured
* an insulator that allows field-effect interaction, without leak currents between the two other components
* a semiconductor to register the chemical changes

The EIS sensor can be used in combination with other structures, for example to construct a light-addressable potentiometric sensor (LAPS).

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select -> ENBIOS 1D
* Press Launch tool in info section.
* Select the -> semiconductor/insulator/electrolyte
* Click on Simulation
* Select ->Result -> Potential
* Select -> electrolyte -> change pH value
* Click on simulation
* Select -> Result -> Potential
* Repeat the above steps for different pH values
* Select -> Insulator-> change thickness and length
* Click on simulation
* Select -> Result -> Potential
* Repeat the above steps for different thickness and length

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of VI characteristics of Bio-FET**

**Ex. No: 27**

**Date:**

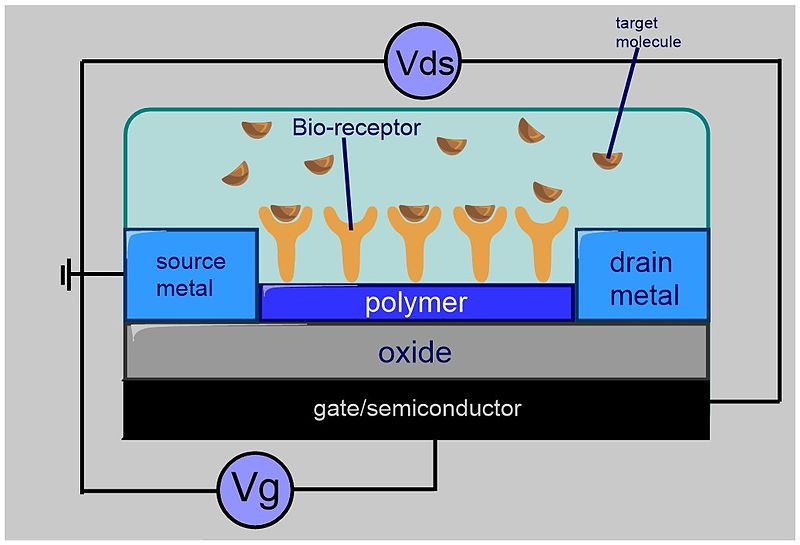
**Aim:**

To obtain the VI characteristics of BIOFET

**Software:** NanoHub Online Tube

**Theory:**

Field-effect transistor-based biosensor (Bio-FET or BioFET) is a field-effect transistor that is gated by changes in the surface potential induced by the binding of molecules. When charged molecules, such as biomolecules, bind to the FET gate, which is usually a dielectric material, they can change the charge distribution of the underlying semiconductor material resulting in a change in conductance of the FET channel. A Bio-FET consists of two main compartments: one is the biological recognition element and the other is the field-effect transistor.



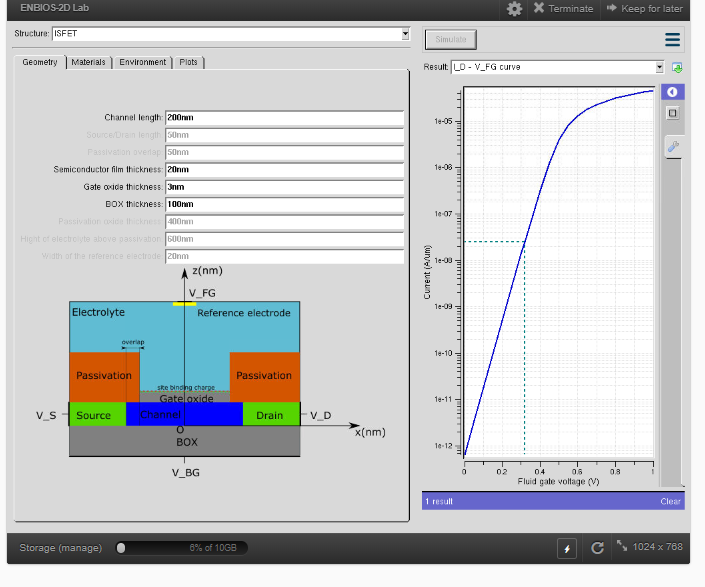
Bio-FETs couple a transistor device with a bio-sensitive layer that can specifically detect bio-molecules such as nucleic acids and proteins. A Bio-FET system consists of a semiconducting field-effect transistor that acts as a transducer separated by an insulator layer (e.g. SiO2) from the biological recognition element (e.g. receptors or probe molecules) which are selective to the target molecule called analyte. Once the analyte binds to the recognition element, the charge distribution at the surface changes with a corresponding change in the electrostatic surface potential of the semiconductor. This change in the surface potential of the semiconductor acts like a gate voltage would in a traditional MOSFET, i.e. changing the amount of current that can flow between the source and drain electrodes. This change in current (or conductance) can be measured, thus the binding of the analyte can be detected. The precise relationship between the current and analyte concentration depends upon the region of transistor operation

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select -> ENBIOS 2D
* Press Launch tool in info section.
* Select the -> ISFET
* Select -> channel length -> enter the value
* Click on Simulation
* Select ->Result -> VI Characteristics
* Repeat the above steps for different channel length
* Select -> Oxide thickness -> enter the value
* Click on Simulation
* Select ->Result -> VI Characteristics
* Repeat the above steps for different oxide thickness

**Parameters:**

**Model Output:**



**Result:**

**Simulation of VI characteristics of solar cell**

**Ex. No: 28**

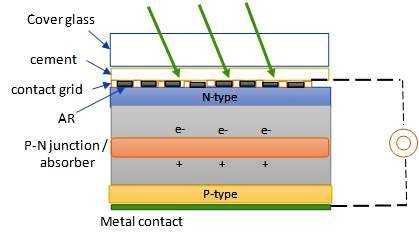
**Date:**

**Aim:**

To obtain the VI characteristics of Solar cell

**Software:** NanoHub Online Tube

**Theory:**



The solar cell works in several steps:

* Photons in sunlight hit the solar panel and are absorbed by semiconducting materials, such as silicon.
* Electrons are excited from their current molecular/atomic orbital. Once excited an electron can either dissipate the energy as heat and return to its orbital or travel through the cell until it reaches an electrode. Current flows through the material to cancel the potential and this electricity is captured. The chemical bonds of the material are vital for this process to work, and usually silicon is used in two layers, one layer being doped with boron, the other phosphorus. These layers have different chemical electric charges and subsequently both drive and direct the current of electrons.
* An array of solar cells converts solar energy into a usable amount of direct current (DC) electricity.
* An inverter can convert the power to alternating current (AC).

The most commonly known solar cell is configured as a large-area p–n junction made from silicon. Other possible solar cell types are organic solar cells, dye sensitized solar cells, perovskite solar cells, quantum dot solar cells etc. The illuminated side of a solar cell generally have a transparent conducting film for allowing light to enter into active material and to collect the generated charge carriers. Typically, films with high transmittance and high electrical conductance such as indium tin oxide, conducting polymers or conducting nanowire networks are used for the purpose

**Procedure:**

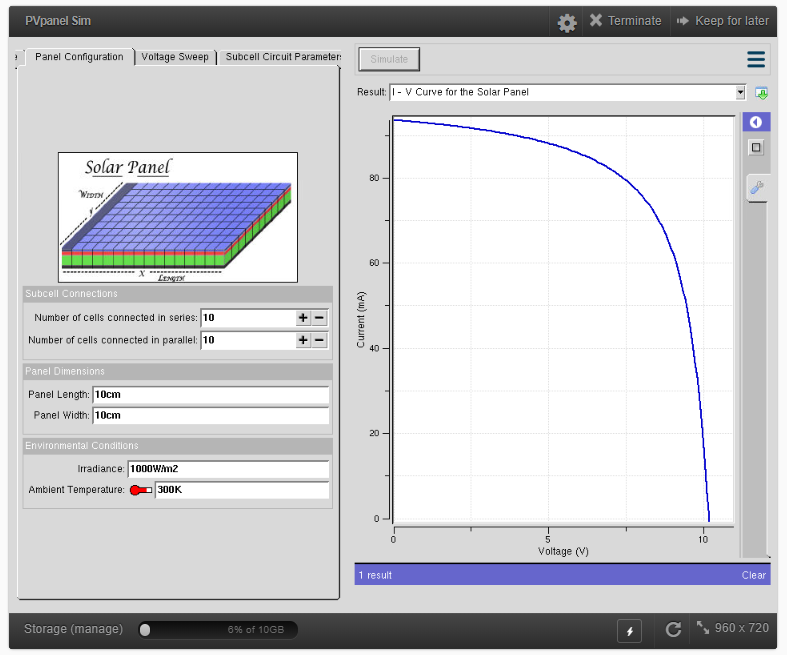
* Open nanoHUB.
* Goto Resources -> Tools.
* Select -> PV -> PV panelsim
* Press Launch tool in info section.
* Select the -> material -> amorphous silicon
* Select -> Panel configuration
* Click on Simulation
* Select ->Result -> IV curve for solar panel
* Repeat the simulation for various panel configuration
* Select the -> material -> Crystalline silicon
* Select -> Panel configuration
* Click on Simulation
* Select ->Result -> IV curve for solar panel
* Repeat the simulation for various panel configuration

**Parameters:**

**Tabulation:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.no** | **Type of Material** | **Panel Configuration** | **Current (mA)** |
| 1 | Amorphous Silicon | 10 x 10 |  |
| 2 | 1 x 1 |  |
| 3 | 100 x 100 |  |
| 4 | Crystalline Silicon | 10 x 10 |  |
| 5 | 1 x 1 |  |
| 6 | 100 x 100 |  |

**Model Output:**

****

**Result:**

**Simulation of deflection of cantilever by applying the force**

**Ex. No: 29**

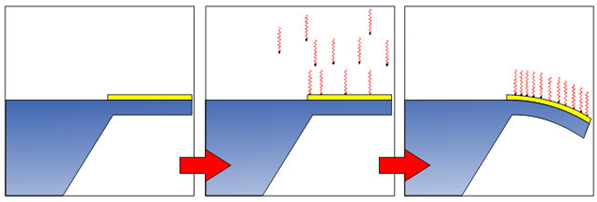
**Date:**

**Aim:**

To obtain the deflection of cantilever by applying the force

**Software:** NanoHub Online Tube

**Theory:**

****

Cantilever sensors are becoming an attractive tool for diagnostics based on their high sensitivity platform and multiplexed detection technique. Being able to use a sensor that can detect multiple target molecules from small biological samples makes this sensor technology a crucial step for studying the detection of diseases such as cancer. With malignant tumours, it is already too late to treat the cancer with a maximum success rate. As cancers spread through blood and particularly the lymphatic system in the body, it then becomes important to measure multiple parameters of biological molecules, hence the more we know at the molecular and cellular level, the more can be predicted about the current state of a disease DNA detection methods that involve DNA labelling, a cantilever biosensor platform involves adsorption of biomolecules on a micromechanical layer. As the biomolecules adsorb onto the surface of the cantilever, the reaction causes a decrease in the surface free energy. A differential surface stress is generated between either sides of the cantilever beam as a result of adsorption of biomolecules occurring at one side of the cantilever. For DNA detection, the hybridization that occurs between the target probes changes the intermolecular interactions within a monolayer at one side of the cantilever layer which induces surface stress that bends the cantilever bean and initiates a motion.

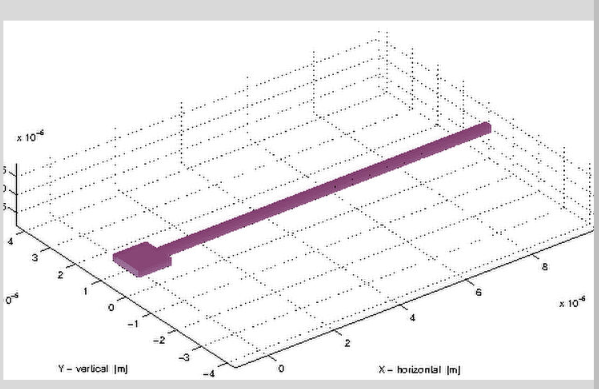
The deflection of the cantilever caused by surface stress change, which is in the range of several nanometres, is measured using a piezoelectric readout.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select -> BioMEMS -> Cantilever
* Press Launch tool in info section.
* Select the -> Tip load-> enter the value of force in x, y and z
* Click on Simulation
* Select ->Result -> Cantilever static analysis 3d
* Repeat the simulation for various force values

**Parameters:**

**Model Output:**

****

**Result:**

**Simulation of stress and strain graph of an bio composite material**

**Ex. No: 30**

**Date:**

**Aim:**

To obtain the stress and strain of an bio composite material

**Software:** NanoHub Online Tube

**Theory:**

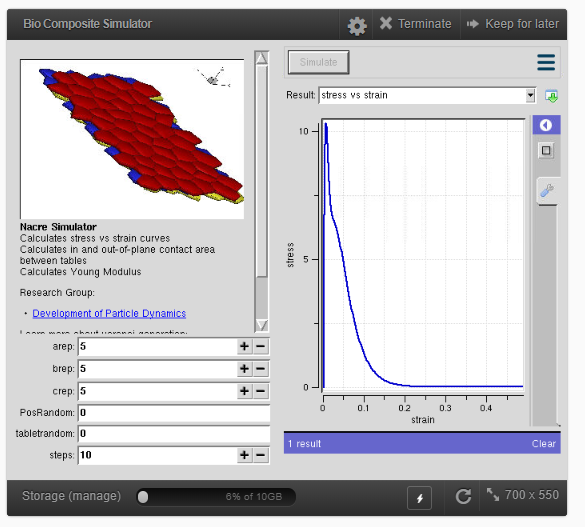
Biocomposite is a composite material formed by a matrix (resin) and a reinforcement of natural fibers. These kind of materials often mimic the structure of the living materials involved in the process keeping the strengthening properties of the matrix that was used, but always providing biocompatibility. The matrix phase is formed by polymers derived from renewable and nonrenewable resources. The matrix is important to protect the fibers from environmental degradation and mechanical damage, to hold the fibers together and to transfer the loads on it.

**Procedure:**

* Open nanoHUB.
* Goto Resources -> Tools.
* Select -> Nanocomposites-> Bio composites simulator
* Press Launch tool in info section.
* Select the -> lattice parameter (a, b, c)
* Click on Simulation
* Select ->Result -> stress vs strain
* Repeat the simulation for various lattice parameters

**Parameters:**

**Model Output:**

****

**Result:**