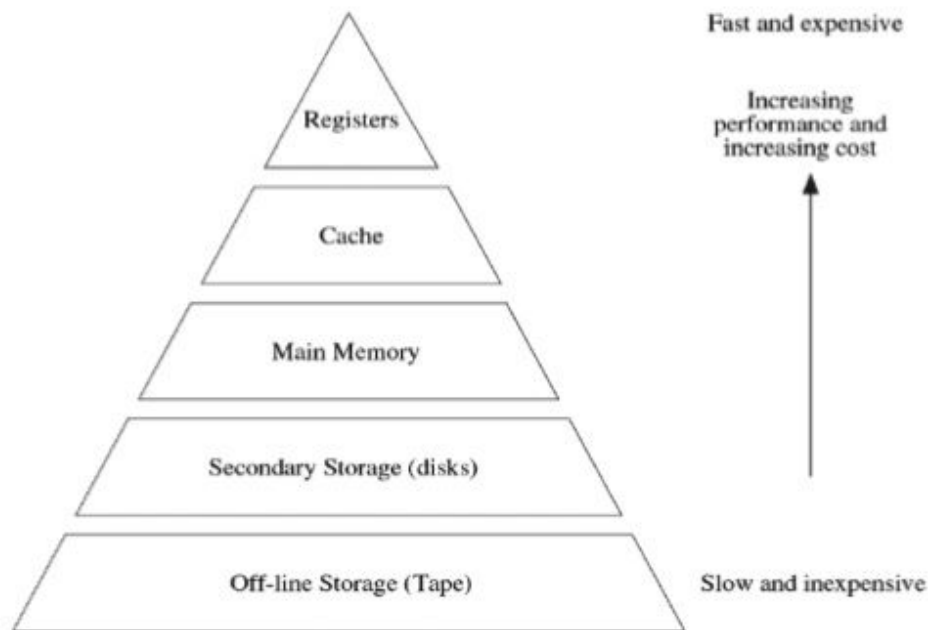


Assignment 4

EE15B025 | Ganga Meghanath

The Memory Hierarchy

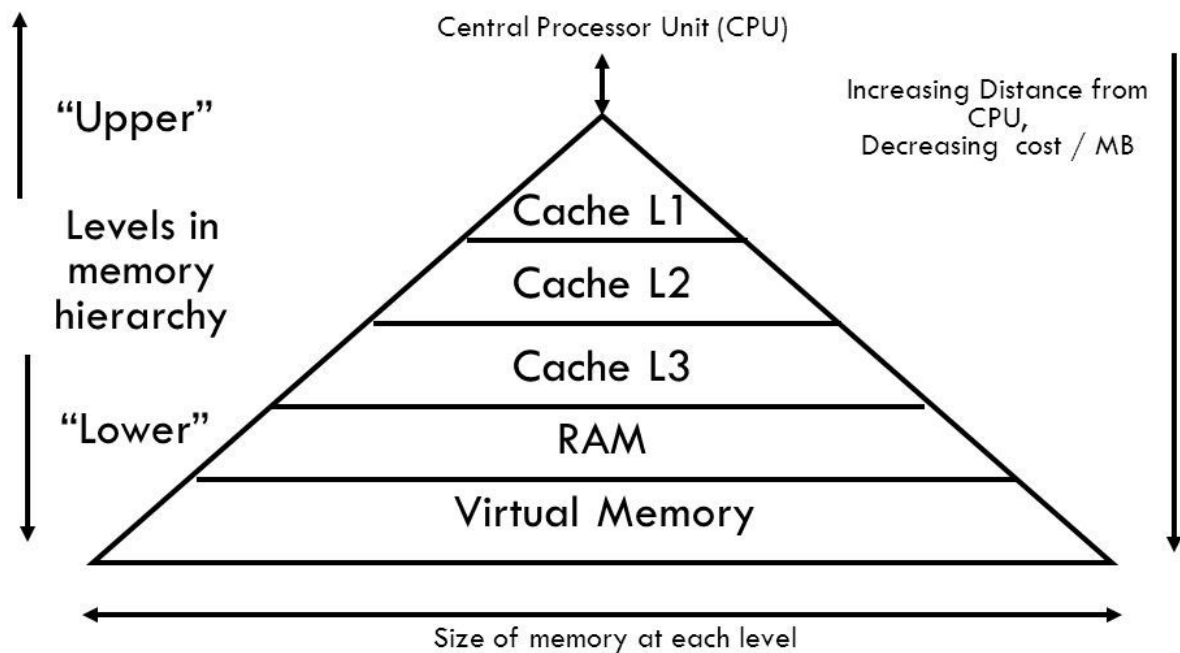


Question

Assume a computer has L1 and L2 caches, as discussed in Section 5.6.3. The cache blocks consist of 8 words. Assume that the hit rate is same for both caches and that it is equal to 0.95 for instructions and 0.90 for data. Assume also that the time needed to access an 8-word block in these caches are $C_1=1$ cycle and $C_2=10$ cycles.

- (a) What is the average access time experience by the processor if the main memory uses interleaving? Assume that the memory access parameters are as described in Section 5.6.1.
- (b) What is the average access time if the main memory is not interleaved?
- (c) What is the improvement obtained after interleaving?

Memory Conclusion (2)



Answer

Hit rate in L1 cache = h_1
= 0.95 ; for instructions
= 0.90 ; for data

Hit rate in L2 cache = h_2
= 0.95 ; for instructions
= 0.90 ; for data

$$t_{avg} = h_1 C_1 + (1 - h_1) h_2 C_2 + (1 - h_1)(1 - h_2) M$$

C_1 : Time to access information in L1 cache

C_2 : Time to access information in L2 cache

M : Time to access information in the main memory

According to Section 5.6.1,

Time to send an address to main memory = 1 clock cycle

Time to access first word = 8 clock cycles

Time to access subsequent words = 4 clock cycles per word

Time to send one word to cache = 1 clock cycle

According to Section 5.6.2,

Assumption : 30% of instructions in a typical program perform read/write operation.

=>130 memory accesses for every 100 instructions executed

$$\begin{aligned}\text{a.) Time required to load the block from the interleaved memory} &= M \\ &= 1+8+4+4 \\ &= 17 \text{ cycles}\end{aligned}$$

Therefore,

$$\begin{aligned}t_{avg} &= [0.95 \times 1 + (1-0.95) \times 0.95 \times 10 + (1-0.95) \times (1-0.95) \times 17] \quad ; \text{ instruction} \\ &\quad + \\ &\quad 0.3 \times [0.9 \times 1 + (1-0.9) \times 0.9 \times 10 + (1-0.9) \times (1-0.9) \times 17] \quad ; \text{ Data} \\ &= \underline{2.0585 \text{ cycles}}\end{aligned}$$

$$\begin{aligned}\text{b.) Time required to load the block from the interleaved memory} &= M \\ &= 1+8+(7 \times 4)+1 \\ &= 38 \text{ cycles}\end{aligned}$$

Therefore,

$$\begin{aligned} t_{avg} &= [0.95 \times 1 + (1-0.95) \times 0.95 \times 10 + (1-0.95) \times (1-0.95) \times 38] && ; \text{instruction} \\ &+ \\ &0.3 \times [0.9 \times 1 + (1-0.9) \times 0.9 \times 10 + (1-0.9) \times (1-0.9) \times 38] && ; \text{Data} \\ &= \underline{2.174 \text{ cycles}} \end{aligned}$$

$$\begin{aligned} \text{c.) Without interleaving, the average access} &=> 2.174/2.0585 \\ &= \underline{1.056 \text{ times longer}} \end{aligned}$$

$$\begin{aligned} \text{Difference in average access time} &= 2.174 - 2.0585 \\ &= \underline{0.1155 \text{ cycles}} \end{aligned}$$