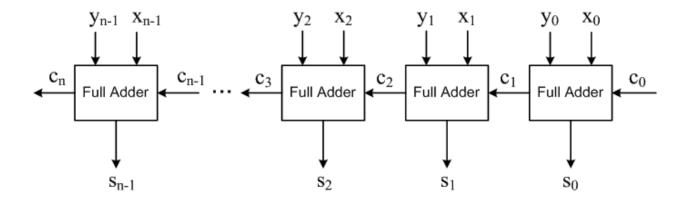
Tutorial 1 EE15B025 | Ganga Meghanath



Question

Show that the logic expression c□⊕c□-₁ is a correct indicator of overflow in the addition of 2's complement integers, by using an appropriate truth table

Answer

The (n-1)th bit is the 'sign' bit. It denotes the sign of the numbers to be added. If the (n-1)th bit is 0, then the number is positive and if it's 1, then the number is negative. Overflow during addition happens while adding either two positive numbers or while adding two negative numbers. We can figure out whether there is an overflow by checking if the (n-1)th bit of the resultant sum, ie, $s\square_{-1}$ is of the opposite sign to that of $x\square_{-1}$ and $y\square_{-1}$. The truth table for the same has been depicted below.

Truth Table

Cases	y 🗆 - 1	X	C □-1	c□	S□-1	C □ ⊕ C □ - 1
1	0	0	0	0	0	0
2	0	0	1	0	1	1
3	0	1	0	0	1	0
4	0	1	1	1	0	0
5	1	0	0	0	1	0
6	1	0	1	1	0	0
7	1	1	0	1	0	1
8	1	1	1	1	1	0

As we can see from the truth table, when the output sign bit is different from that of the inputs, $c \square \oplus c \square_{-1}$ becomes 1. Hence, we can check for overflow using $c \square \oplus c \square_{-1}$.