# Review and Simulation of a Switchable Opamp for Switched-Capacitor Integrators

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***Abstract*—In switched-capacitor integrators power disipation is mainly due to the opamp. During the sampling phase of a switched-capacitor (SC) integrator, the opamp can be turned off to save power dissipation. A switchable-opamp approach based on a current-mirror opamp with switchable transconductances is proposed in this study.The suggested approach can be applied to SC integrators with both half delay and full delay, in contrast to earlier switchable-opamp approaches that could only be employed in half delay SC integrators. Moreover, the opamp does not require any unique common-mode feedback (CMFB) circuits. The suggested method can reduce power by 30% at high sampling frequencies, with little impact on the gain error of the SC integrator. This demonstrates that the speed of the SC circuit is not restricted by the suggested switchable-opamp approach. In this SC integrator, A switchable operational amplifier (opamp) i.e, a current-mirror opamp with switchable transconductance values is used. It is shown that there is very little additional circuit design complexity and optimal switching is developed. This brief also demonstrates that, in comparison to a SO design, the absolute average power usage can be lower.**

***Index Terms*—switched-capacitor (SC), SC integrator, common mode feedback(CMFB) circuit,switched opamp (SO), , operational amplifier (opamp), switchable opamp.**

## I. Introduction

Many analog system uses integrators such as analog to digital converters(ADCs) and filters. The output of continuous-time integrator as shown in fig.1 can be written as

$$V_{\text{out}} = -\frac{1}{RC_F}\int V_{\text{in}}\, dt \tag{1}$$

here in fig.1,the opamp is ideal or gain is very large.

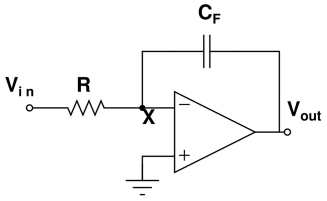



Fig. 1: Continuous-time integrator

But, in many situation we need the input value only at fix interval of time, for that we uses sampled data by using discrete time integrator i.e, Switched capacitor(SC) integrator as shown in fig.2. SC integrator is the building block of most of the SC filters such as discrete-time sigma-delta($\Delta\Sigma$) modulator. On the basis of output sampling phase ($S_{out}$), we can define the SC integrator with *full-delay* (Fig.2(a)) and the SC integrator with *half-delay* (Fig.2(b)).

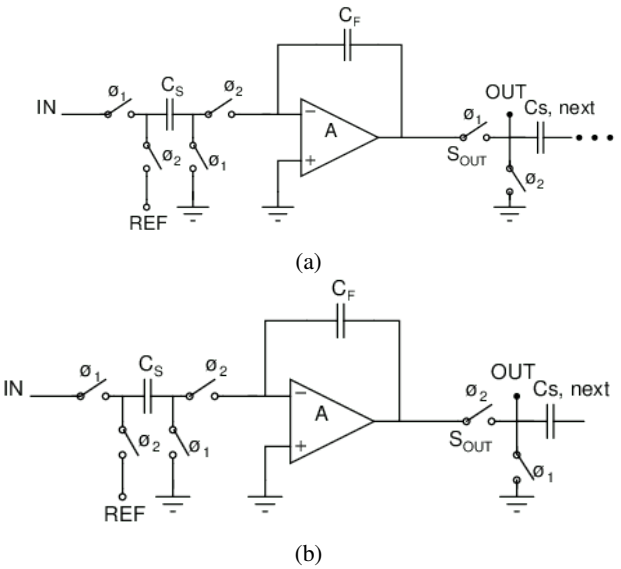
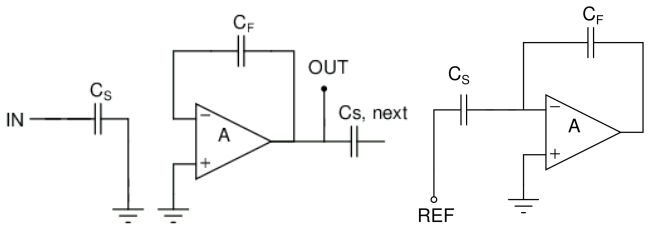



Fig. 2: SC integrator with the subsequent sampling stage loading effect with capcitor $C_{S,next}$. (a) the SC integrator with full delay . (b) the SC integrator with half-delay

Input of SC integrator is sampled on the capacitor $C_S$ during sampling phase $\phi_1$, whereas the output of the previous phase is stored on capacitor $C_F$ and sampled in a full-delay SC integrator by the sampling capacitor $C_{S,next}$ of the subsequent stage (Fig.3(a)). As the output of SC integrator remains constant throughout phase $\phi_1$, so the opamp can be switched off entirely (or partly, in the case of a full-delay SC integrator) to reduce the power dissipation. The charge stored on capacitor in previous phase $\phi_1$ get transferred during Charge-trannsfer phase $\phi_2$ and sampled in a full-delay SC integrator by the sampling capacitor $C_{S,next}$ of the subsequent stage (Fig.3(b)). Because of this, the opamp needs to be completely functional during this charge-transfer phase.




(a) Phase($\phi_1$) (b) Phase($\phi_2$)

Fig. 3: A full-delay SC integrator during: (a)sampling phase $\phi_1$; and (b) its charge-transfer phase $\phi_2$

## II. Switched-Opamp

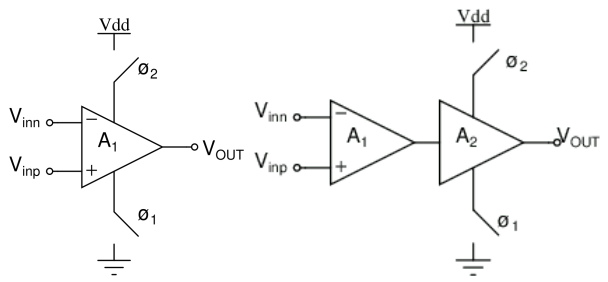
Many switchable-opamp techniques have been used to decrease power dissipation SC integrators in DT $\Delta\Sigma$ modulators and SC filters. These includes:

1) **Switched Opamp (SO).**
   In this case, the opamp of the integrator is completely turned off during the sampling stage (Fig.5(a)). This can reduce power usage by up to 50% when compared to traditional systems that have opamps operating constantly [3]. Because it takes time to turn on the opamps, this may restrict the speed of operation.
2) **Partially Switched Opamp (SO).**
   In this case, a two-stage opamp is employed and its output stage is turned off only when sampling is taking place (Fig. 5(a)). Compared to a SC integrator with a SO design, a faster turn-on time and, consequently, higher operating speed can be attained by keeping the input of opamp stage on throughout the phase. Since the input stage may burn 1/4 of the overall power consumption of the opamp, therefore, power reductions of 40

As the opamp output is in a high-impedance condition during the sampling phase, the floating switch (Fig.2(b)) can be omitted, which is another benefit of the SO and PSO approaches. This can enhance the linearity of the integrator, especially in designs with low voltage supplies. However, The drawback of both the SO and PSO approaches is that they are limited to specific DT $\Delta\Sigma$ modulator design because they can only be used in SC integrators with half delay.

## III. Proposed switchable Opamp

A switchable-opamp is suggested in this work for the low-power SC integrator architecture. the current mirror opamp is used in the design [8], however during the sampling stage, transconductances can be turned off. Both full and half delay SC integrators can implement this switchable opamp. Additionally, It is unaffected by the operation-speed constraints present in SO designs because its input transconductance is always on. As we can see in the simulation, adopting the proposed switchable-opamp instead of the current-mirror opamp, which is always fully active, can reduce power consumption in SC integrators by up to 30%.




(a) (b)

Fig. 5: Symbolic representation of: (a) the switched-opamp; and (b) the partially-switched-opamp methods

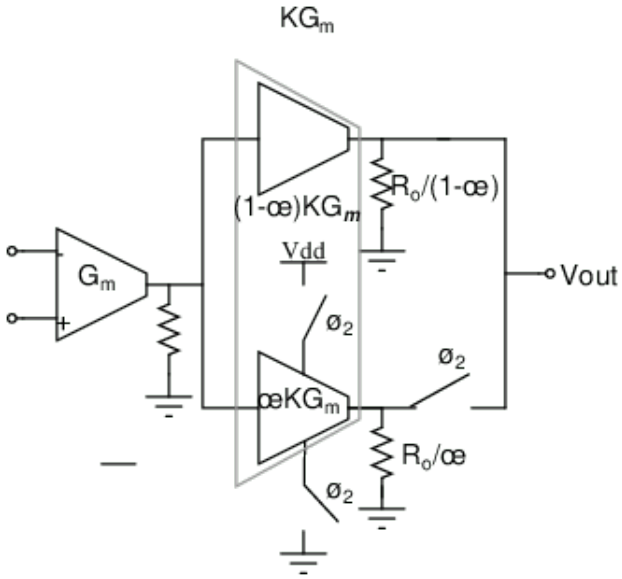



Fig. 6: Symbolic representation of proposed switchable opamp

The Symbolic representation of proposed switchable opamp can be seen in Fig. 6. where $G_m$ is input transconductance and $KG_m$ total output transconductance, where K representing the current gain from the input to the output sides of the opamp. As we can see in the fig.6, the load and the transconductance of second stage are divided into two portions, $\alpha$ and $(1-\alpha)$. In sampling phase $\phi_1$, $\alpha$ part of the load and total transconductance is turned off, on the other hand $(1-\alpha)$ part remains turned on throughout the phase. The proposed circuit has the following advantages over the switched opamp:

1) Since the opamp output is available throughout the phases, it may be utilized to create both full-delay and half-delay SC integrators. Additionally, no special is required as this opamp can be utilized with conventional SC common-mode feed-back (CMFB) circuits.
2) To optimize the unity-gain bandwidth $\omega_t$ and to get the desired settling accuracy, the opamp operates at its full output transconductance (K $G_m$), during charge transfer phase $\phi_2$. However, since the output of the opamp remains constant during the sampling phase $\phi_1$, there is no requirement for a high $\omega_t$ and thus the feedback factor

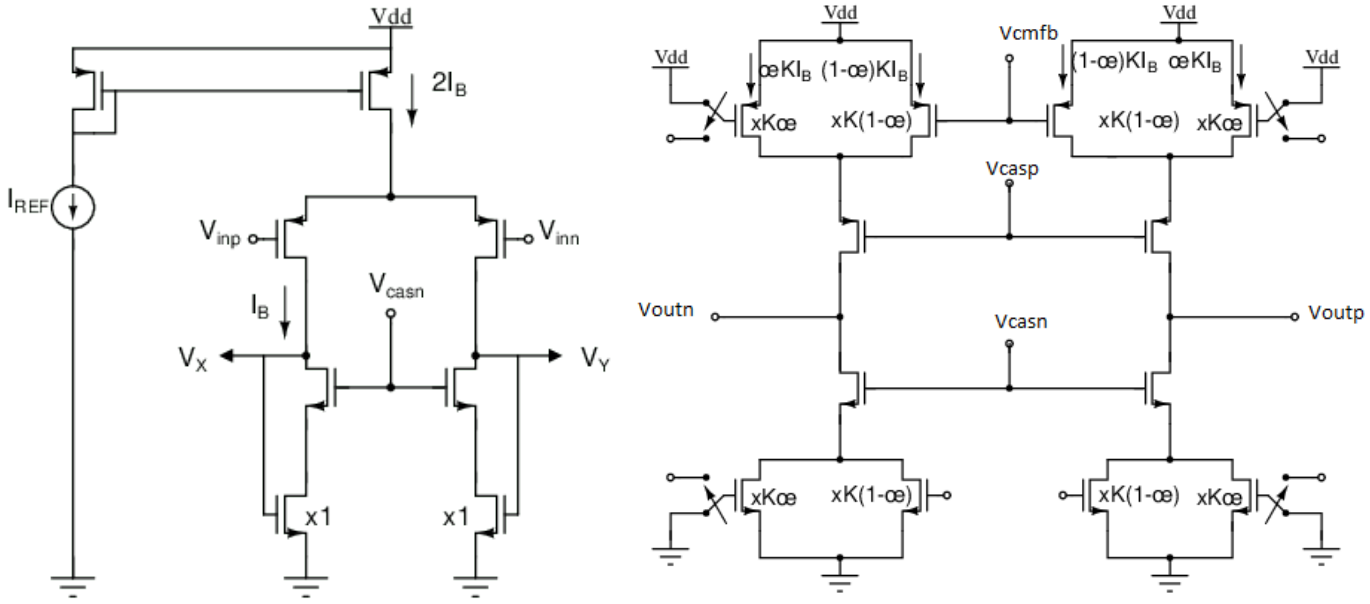



Fig. 4: Circuit diagram of Fig.6.

is close to unity. Therefore, the power dissipation can be reduce by switching off the a portion of the opamp's output transconductance during sampling phase $\phi_1$. It is significant to remember that sampling the output on the $C_{s,next}$ sets an upper bound on the value of $\alpha$ for the full-delay integrator (Fig.2(a)).

3) The opamp is is unaffected from the operating speed limitations present in SO and PSO architecture, because both its input and a portion of its output transconductances are always active, due to this its turn-on time is shorter.

## IV. Circuit Design Of The Proposed Switchable Opamp

As we see in Fig.4, by using bias current sources and cascode current mirrors,consider a classical fully differential current-mirror opamp with the current gain of K [8].If the load capacitance limits the unity-gain frequency at a certain total bias current (power dissipation), then raising K increases the unity-gain bandwidth and the slew-rate at the cost of an increase in phase margin and input-referred thermal noise. K's practical limit might be approximately. the circuit in Fig.4 can be realize, in phase $\phi_2$ the $\alpha$ part with turn on and off in sampling phase $\phi_1$, the output current switched from $\alpha$KI to $(1-\alpha)KI$ in sampling phase.

It is important to remember that, as illustrated in Fig. 2, the cascode transistors in the output stage must be switched in sync with the other transistors in order to change the output resistance and preserve a steady opamp dc gain. One possible substitute is to maintain the cascode transistors operating continuously at full width, as illustrated in Fig.4, and modify the biasing conditions so that the dc gain varies little while switching, or at the very least, does not produce undesirable distortion.

## V. Power Reduction

In Fig.4, the supply current in the circuit at $\alpha$=0(classical current mirror opmp),

$$I_{tot|_{classic}} = 2I_B + 2KI_B \tag{2}$$

where $2I_B$ is the input differential-pair bias current. For 50%, the supply current of switchable opamp(i.e, $\alpha \neq 0$) is

$$I_{tot|_{proposed}} = 2I_B + (2-\alpha)KI_B \tag{3}$$

Hence, there is decrease in supply current in the switchable opamp is

$$\Delta I_{tot} = I_{tot|_{classic}} - I_{tot|_{proposed}} = \alpha KI_B \tag{4}$$

Hence the power reduction of

$$\frac{\Delta I_{tot}}{I_{tot|_{classic}}} = \frac{\alpha/2}{1+1/K} \tag{5}$$

The current-mirror gain K and the switching ratio $\alpha$ determine the possible power decrease. With a K = 4, a 30 % power reduction may be attained for an $\alpha$ of 0.75. The $C_S, next$ is connected in case of half-delay SC integrator during phase $\phi_2$(i.e, charge transfer phase), The opamp's turn-on time required to recover its output current sets a limit on $\alpha$. 0.75 or nearby value can be a practical limit for $\alpha$. On the other hand, the $C_{S,next}$ is connected in case of full-delay SC integrator during phase $\phi_1$(i.e, sampling phase), $C_{S,next}$ is the primary source for determining the maximum (optimal) value of $\alpha$.

Here, we will find the optimised $\alpha$ that gives the minimum settling error for a given value of supply current $I_{tot}$ and therefore needs the minimum $I_{tot}$ for required settling error in full delay SC integrator. Consider the gain of integrator is $K_I$= CS/CF. To concentrate on the settling errors brought on by the finite bandwidth, which is connected to the current

consumption,assume dc gain of opamp infinite. Also consider $G_{mf}$ is the transconductance of current-mirror opamp. Also neglect the paracitics, the feedback factors $\beta_1$,$\beta_2$ during phase $\phi_1$ and phase $\phi_1$ respectively are

$$\beta_1 = \frac{C_F}{C_F} = \beta C_S \quad \beta_2 = \frac{C_F}{C_F + C_S} \tag{6}$$

The load capacitance for the full-delay integrator in both phases can be written as

$$C_{Lf1} = C_{S,next} \quad C_{Lf2} = \frac{C_S C_F}{C_S + C_F} = 1 \tag{7}$$

On the other hand, the closed-loop time constant is given as

$$\tau_{f2} = \frac{C_{Lf2}}{\beta_2 G_{mf2}} \quad \tau_{f1} = \frac{C_{Lf1}}{\beta_1 G_{mf1}} \tag{8}$$

where

$$G_{mf2} = G_{mf} \quad G_{mf2} = (1-\alpha) G_{mf} \tag{9}$$

At the end of phase $\phi_2$, The output of an input step for a settling time $T_{set}$ that is available The input voltage sampled on $C_S$, represented by $V_{in,step}$, can be written as

$$V_{outf} = K_I V_{in,step}(1 - e^{-\frac{T_{set}}{\tau_{f2}}}) \tag{10}$$

The output sampled on $C_{S,next}$ at the end of the phase $\phi_1$ can be written as

$$V_{outf,sampled} = V_{outf}(1 - (\frac{C_{S,next}}{C_F + C_{S,next}})e^{-\frac{T_{set}}{\tau_{f1}}}) \tag{11}$$

$$= K_I V_{in.step}(1 - e^{-\frac{T_{set}}{\tau_{f2}}})(1 - (\frac{C_{S,next}}{C_F + C_{S,next}})e^{-\frac{T_{set}}{\tau_{f1}}})$$

from which the relative settling error can be expressed as

$$\epsilon_f = e^{-\frac{T_{set}}{\tau_{f2}}} + (\frac{C_{S,next}}{C_F + C_{S,next}})(1 - e^{-\frac{T_{set}}{\tau_{f2}}})e^{-\frac{T_{set}}{\tau_{f1}}} \tag{12}$$

Assuming that $\tau_{f1}$,$\tau_{f1}$¡$3T_{set}$,then

$$\epsilon_f \approx e^{-\frac{T_{set}}{\tau_{f2}}} + (\frac{C_{S,next}}{C_F + C_{S,next}})e^{-\frac{T_{set}}{\tau_{f1}}} \tag{13}$$

$$\epsilon_f \approx e^{-\frac{T_{set}\beta_2 G_{mf2}}{C_{Lf2}}} + (\frac{C_{S,next}}{C_F + C_{S,next}})(1 - e^{-\frac{T_{set}}{\tau_{f2}}})e^{-\frac{T_{set}\beta_1 G_{mf1}}{C_{Lf1}}} \tag{14}$$

Assume that $C_{S,next}$ = $\gamma C_S$ and $C_F$ = $\mu C_S$ where $\gamma$ is a capacitor ratio and $\mu = 1/K_I$ , $\epsilon_f$ can be written as

$$\epsilon_f \approx e^{-\frac{T_{set} G_{mf}}{C_S}} + (\frac{\gamma}{\mu + \gamma})e^{-\frac{T_{set}(1-\alpha) G_{mf}}{\gamma C_S}} \tag{15}$$

## VI. Conclusion

The proposed switchable opamp design are reducing the power of sc integrator. we can us the switchable opamp for both full and half delay SC integrators. additionally it can work on conventional common mode feedback and does not require special circuitry. It also provide higher operational speed as compared to switched opamp.Power saving optimization and comparison with the SO method are performed.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