EE537 Circuit Simulation Lab
Experiment 9

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1 Layout of an inverter

Create a Layout of an inverter with the PMOS transistor of (4u/1u) and NMOS transistor of (2u/1u).Present the pre-layout and post-layout simulation result of your inverter.

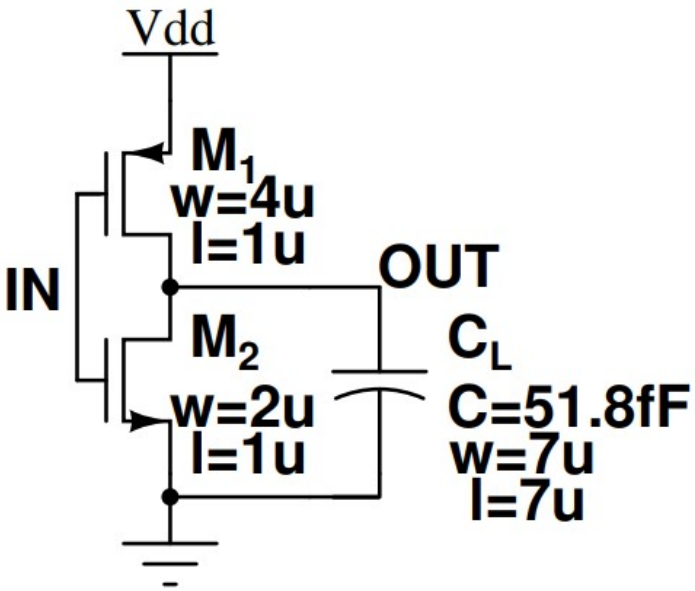

Figure 1: Schematic of an inverter

- schematic

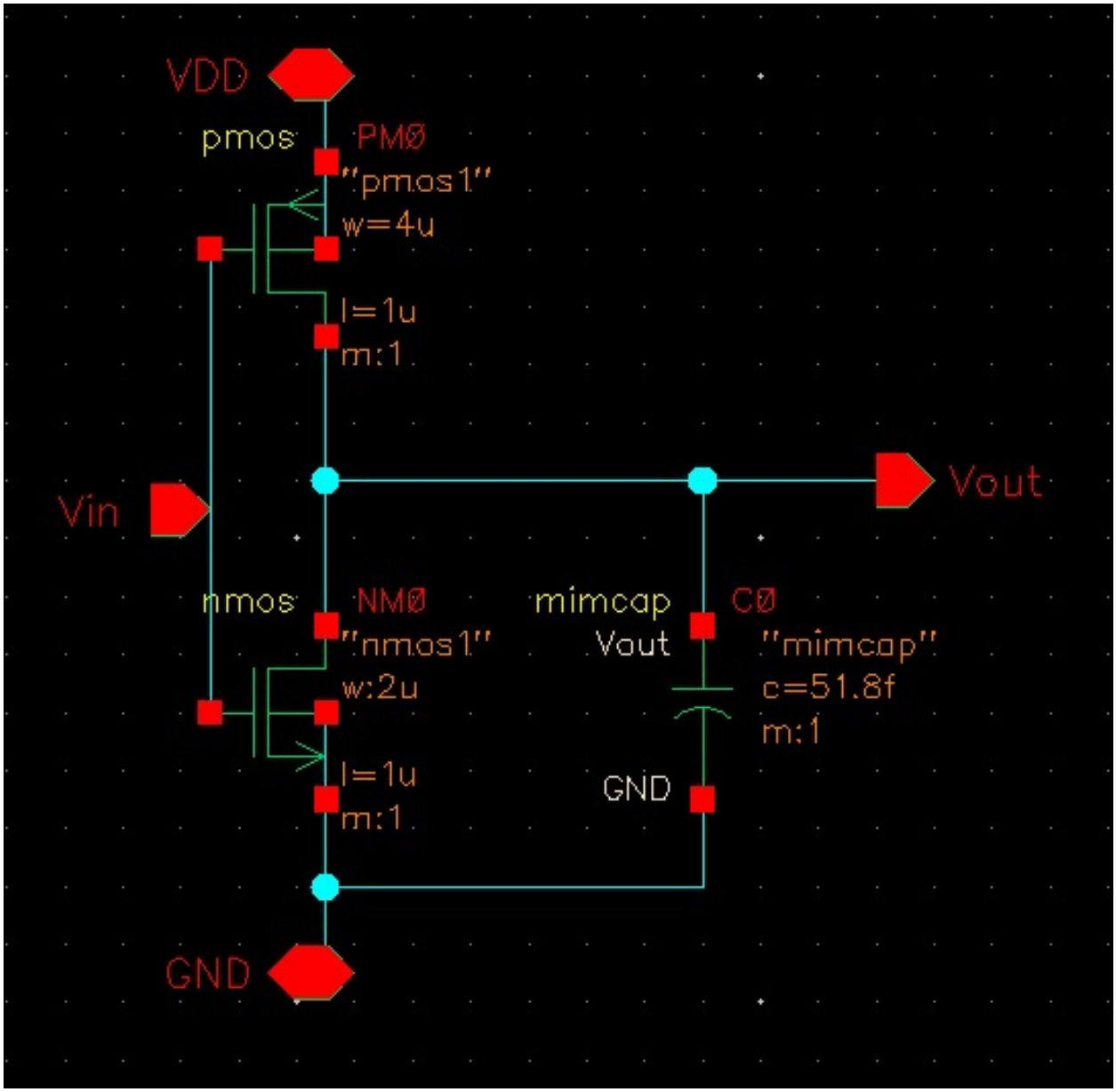

Figure 2: schematic of inveter

- testbench

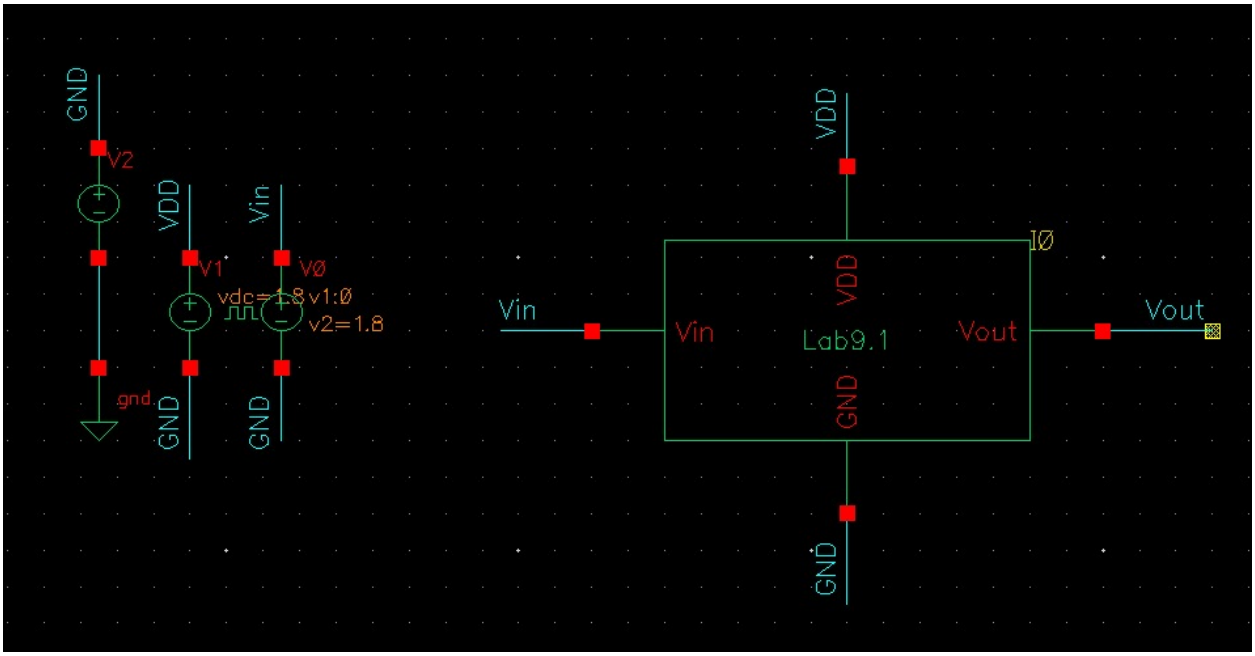

Figure 3: testbench of the inverter

- Layout

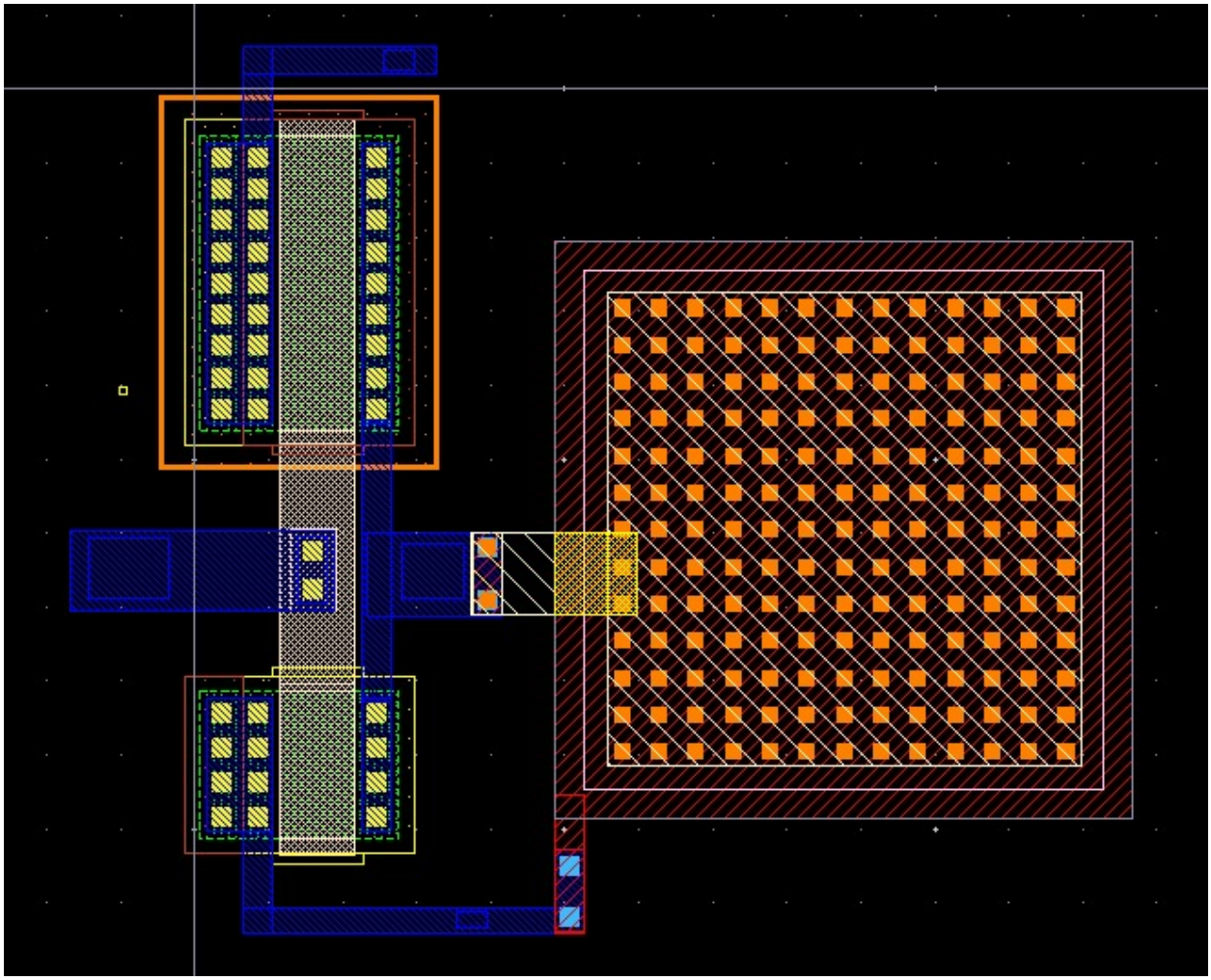

Figure 4: layout of the inverter

- AV extracted layout

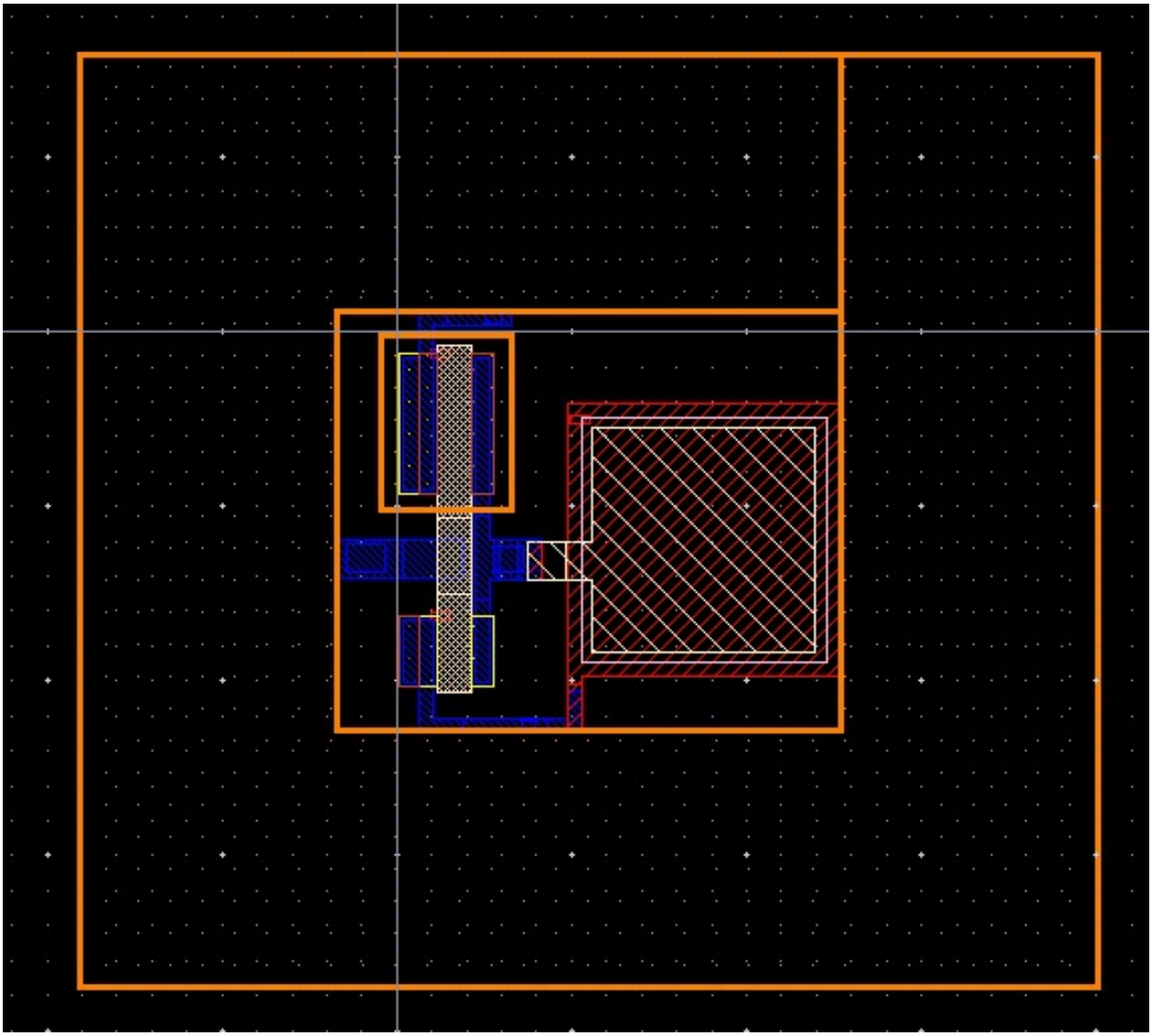

Figure 5: AV extracted layout of the inverter

- design run check

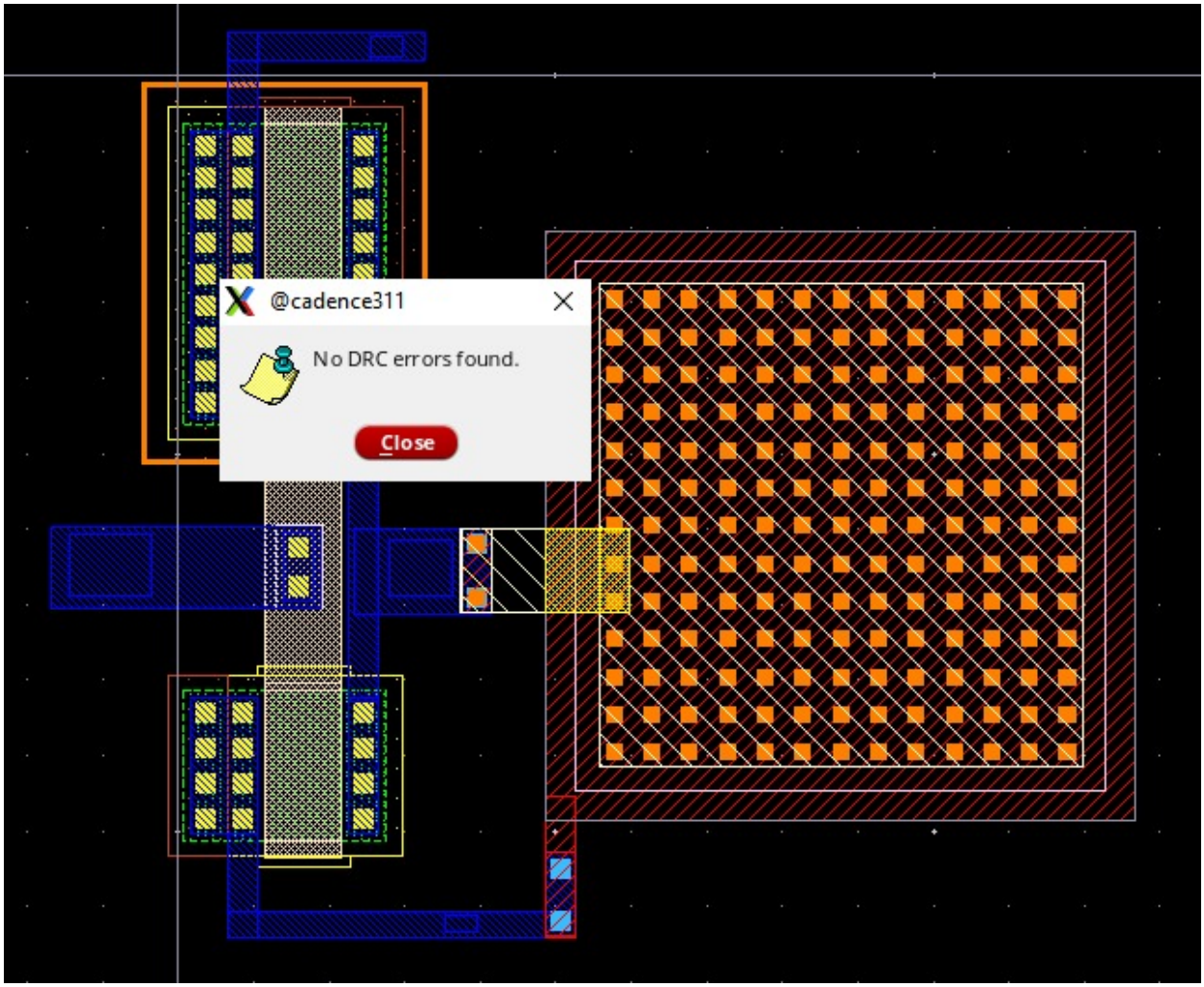

Figure 6: drc of the inverter

- layout vs schematic

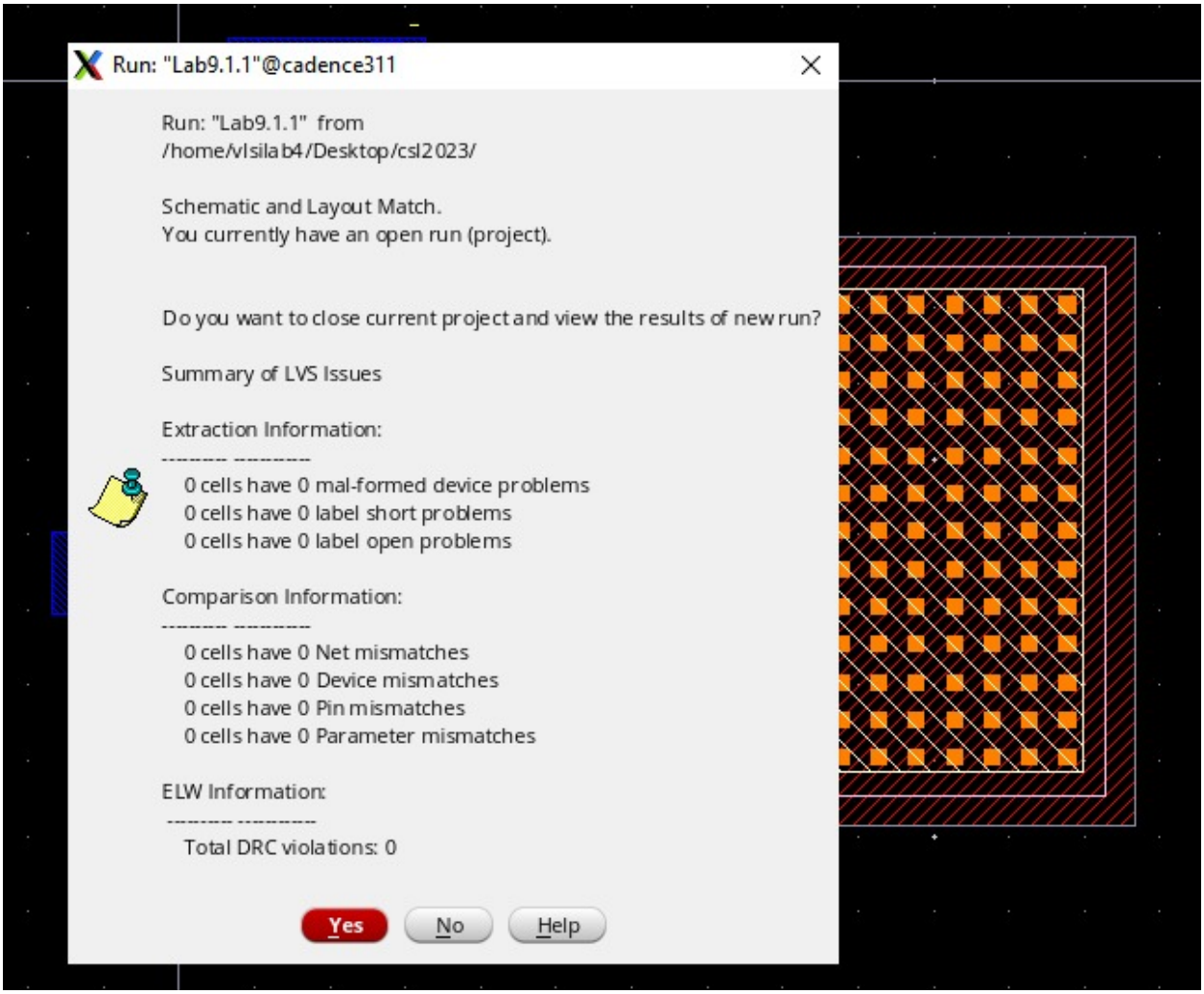

Figure 7: lvs of the inverter

- pre and post layout

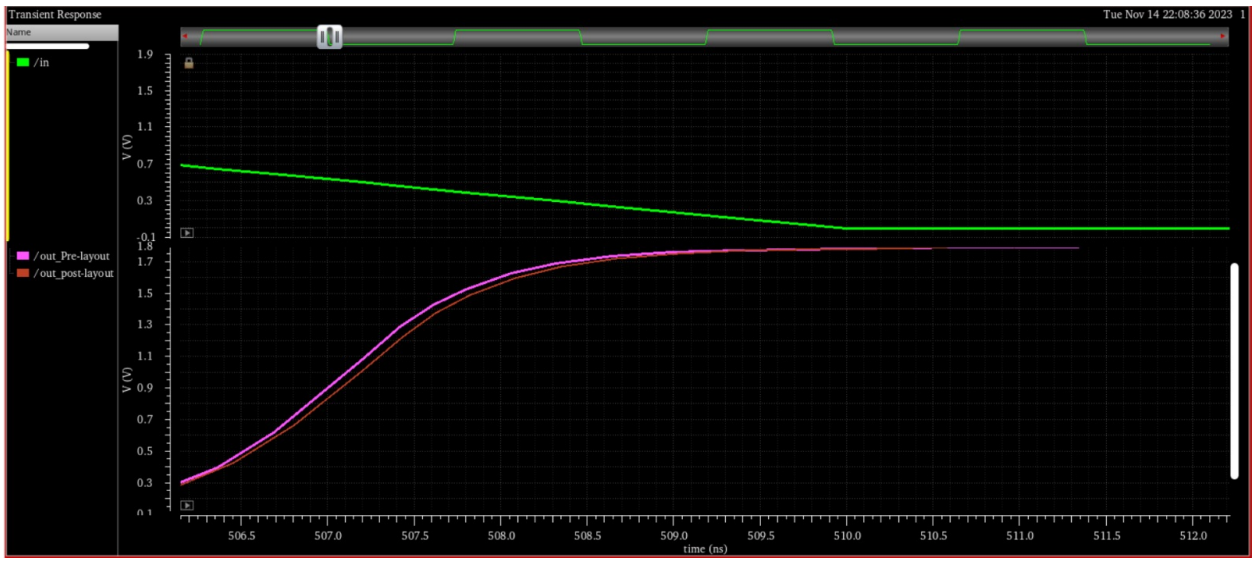

Figure 8: output of the pre layout and post layout

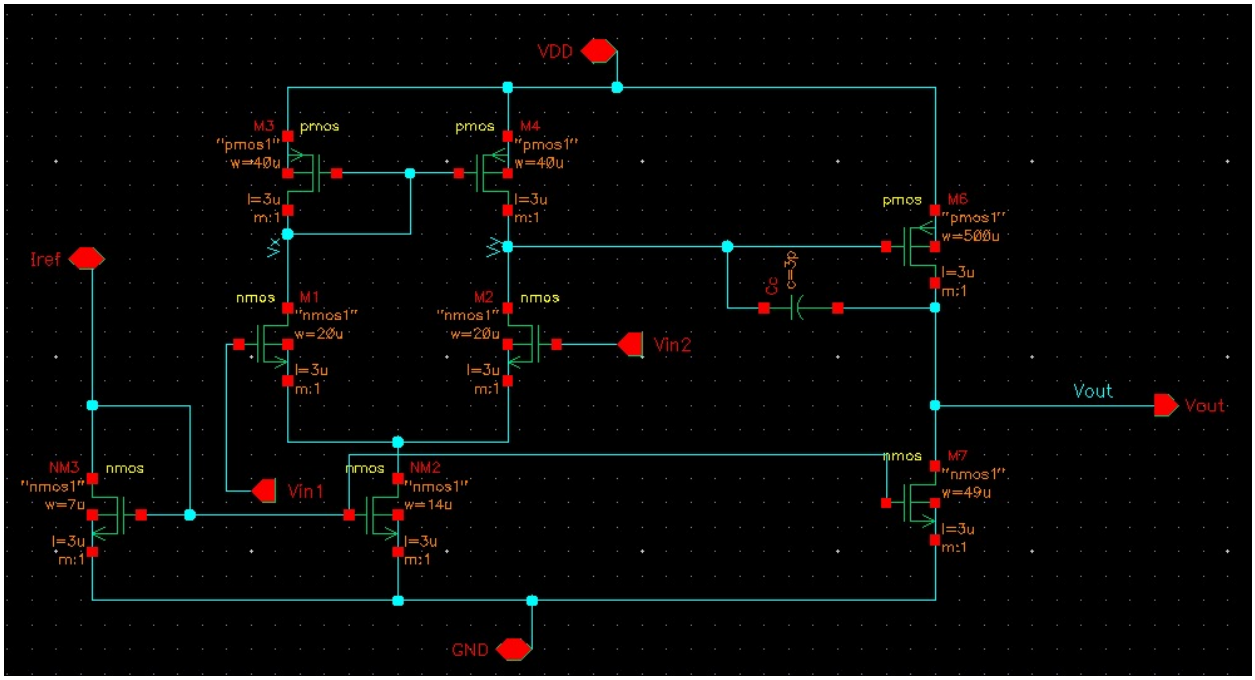

Figure 9: Ota schematic

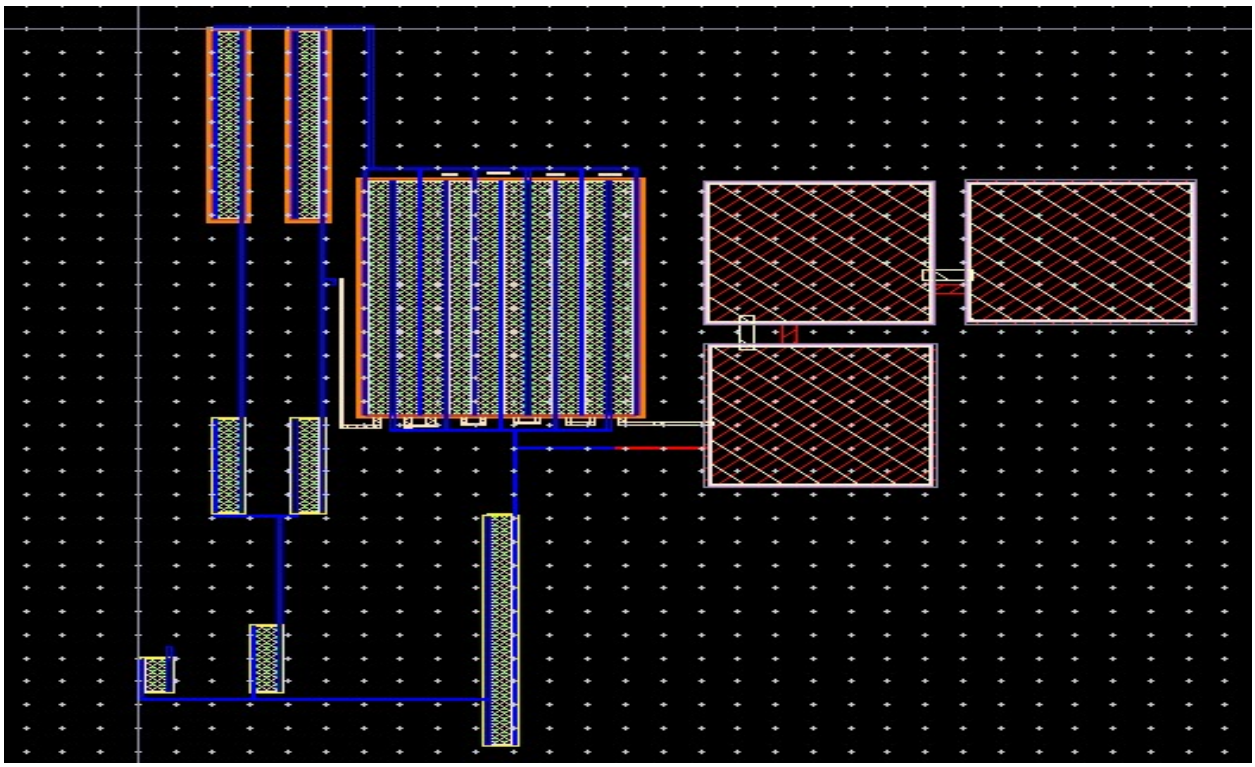

Figure 10: ota layout