

Name: - Gangadhara K

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Executive Summary

- Good Knowledge of Digital Electronics
- Good Knowledge of Digital CMOS
- Good Knowledge of Verilog
- Good knowledge of System Verilog
- Basics knowledge of STA and UVM

Skills Summary

HDLs : Verilog

HVLs : System Verilog

Tools : Xilinx Vivado, NG spice, Cadence, EDA Playground

Certification Courses

➤ **Company** : Yuvasaarathi

Course : Digital Design and Implementation (2023)

➤ **Company** : CoachED

Course : Digital Circuit Design and STA using Verilog & NGSpice (Ongoing)

Projects

1. Skitter Circuit for Delay Analysis under Voltage Fluctuation

- Designed a Skitter Circuit to study signal delay variation under voltage fluctuations.
- Used buffer chain and D flip-flops to track rising clock edge movement.
- Implemented XOR-based logic to detect the exact stage of edge transition.
- Enabled precise monitoring of voltage-sensitive delay shifts.

Tools Used: NGspice, Xilinx Vivado

2. Cache Memory Design using Verilog

- Designed a cache memory system using Verilog.
- Implemented LRU, LFU, and hybrid (LRU-LFU) replacement policies.
- Added logic for data migration between LRU and LFU based on a threshold.

Tools Used: Xilinx Vivado

Education

EDUCATION	Institution/ University	Year of Passing	Percentage / CGPA
Bachelors of engineering in ECE	Govt SKSJTI (VTU)	2025	8.5
II PUC	BGS PU COLLEGE	2021	94%
X	SBS High School	2019	93%

Hobbies

- Sports
- Listening Music
- Attending Hackathons
- Monitoring social impact news via online platforms

Extracurricular Activities:

- Participated in Design and Innovation Clinic (DIC) at CMTI with the project Nandhi Rover – an agricultural rover; secured 1st Runner-up position.
- Secured **1st Prize in Table Tennis** at the **college-level sports meet**, showcasing strong focus, reflexes, and competitive spirit in individual sports performance.

Personal Details

Date of Birth: 29-04-2003

Languages Known: English, Kannada

Nationality: Indian

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