AN5673

Application note

Getting started with STM32C0 Series hardware development

Introduction

This document is addressed to system designers who require an overview of the hardware implementation of development board features (such as power supply, clock management, reset control, boot mode settings and debug management). It shows how to use STM32C0 Series devices and describes the minimum hardware resources required to develop an application.

This document also includes detailed reference design schematics with the description of the main components, interfaces and modes.

1 Power supplies and reset sources

This section describes the power supply schemes and the reset and power supply supervisor on STM32C0 Series devices, based on an Arm® core.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Power supplies

The STM32C0 series devices require a 2.0 to 3.6 V operating supply voltage (V_{DD}). Several different power supplies are provided to specific peripherals:

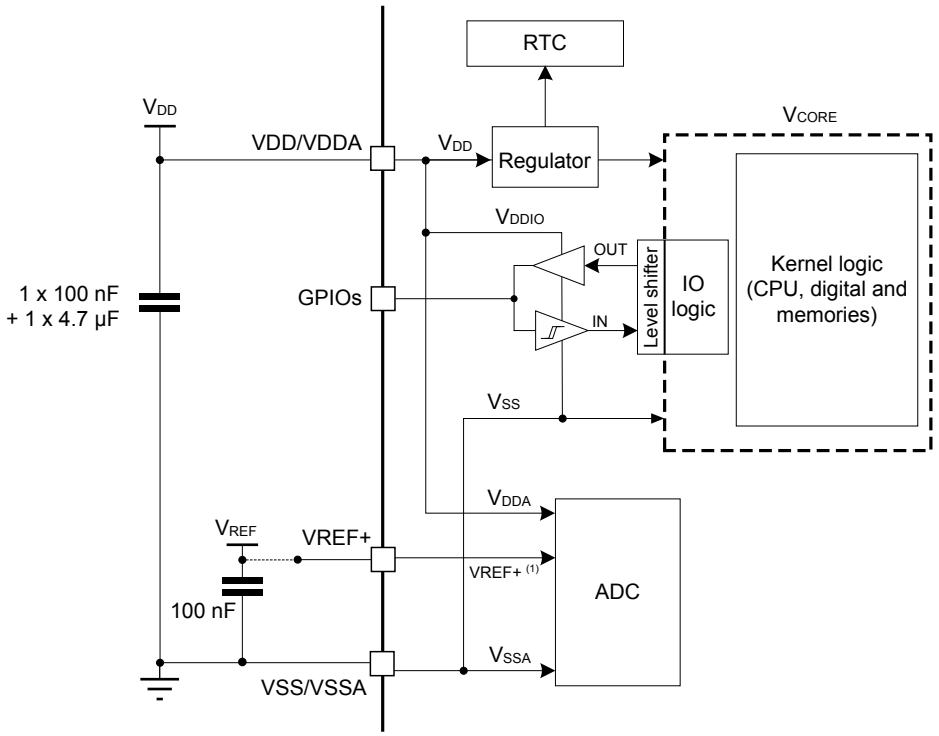
- V_{DD} = 2.0 to 3.6 V
  V_{DD} is the external power supply for the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pin.
  Note that the power-on reset happens when the $V_{POR(max)}$ = 1.94 V threshold is crossed by V_{DD} and that this value is below 2 V (V_{DD} recommended minimum value). Once this threshold is crossed, the functionality is guaranteed down to the power-down reset threshold $V_{PDR(min)}$ = 1.92 V.
- V_{DDA} = 2.0 to 3.6 V
  V_{DDA} is the analog power supply for the A/D converter. Its voltage level is identical to the V_{DD} voltage, as it is provided externally through VDD pin (V_{DD} and V_{DDA} are shorted due to the low number of pins on the packages proposed for the STM32C0 series).
- V_{DDIO} = V_{DD}
  V_{DDIO} is the power supply for the I/Os. Its voltage level is identical to V_{DD} voltage as it is provided externally through VDD pin (V_{DD} and V_{DDIO} are shorted due to the low number of pins on the packages proposed for the STM32C0 series).
- V_{REF+} is the input reference voltage for the ADC. Its voltage level is identical to the V_{DD} voltage as it is provided externally through VDD pin (V_{DD} and V_{DDIO} are shorted due to the low number of pins on the packages proposed for STM32C0 series). Package with separate V_{REF+} pin, V_{REF+} must be between 2 V and V_{DDA} or can be grounded when the ADC is not active. V_{REF-} is bonded to V_{SS} and V_{SSA}, whatever the package.
- V_{CORE}
  An embedded linear voltage regulator is used to supply the V_{CORE} internal digital power, the power supply for digital peripherals, SRAM, and flash memory. The flash memory is also supplied by V_{DD}.

Table 1. Power supplies of STM32C0 series

Power supply	STM32C0 series
V_{DD}	2.0 to 3.6 V
V_{REF+}	V_{REF+} must be between 2 V and V_{DDA}(1)

1. *This is only true for the packages where a dedicated V_{REF+} pin is present. In the other cases, V_{DD}, V_{DDA} and V_{REF+} are shorted and correspond to the same voltage.*

Figure 1. STM32C0 series power supply



(1): Internally connected to the V_{DD}/V_{DDA} pin on packages without VREF+ pin.

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Note: Power supply pin pairs (VDD/VDDA and VSS/VSSA) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

1.2 Power supply supervisor

1.2.1 Power-on reset (POR) / power-down reset (PDR) / brown-out reset (BOR)

The devices feature an integrated power-on reset (POR) / power-down reset (PDR), coupled with a brown-out reset (BOR) circuitry. The POR/PDR is active in all power modes.

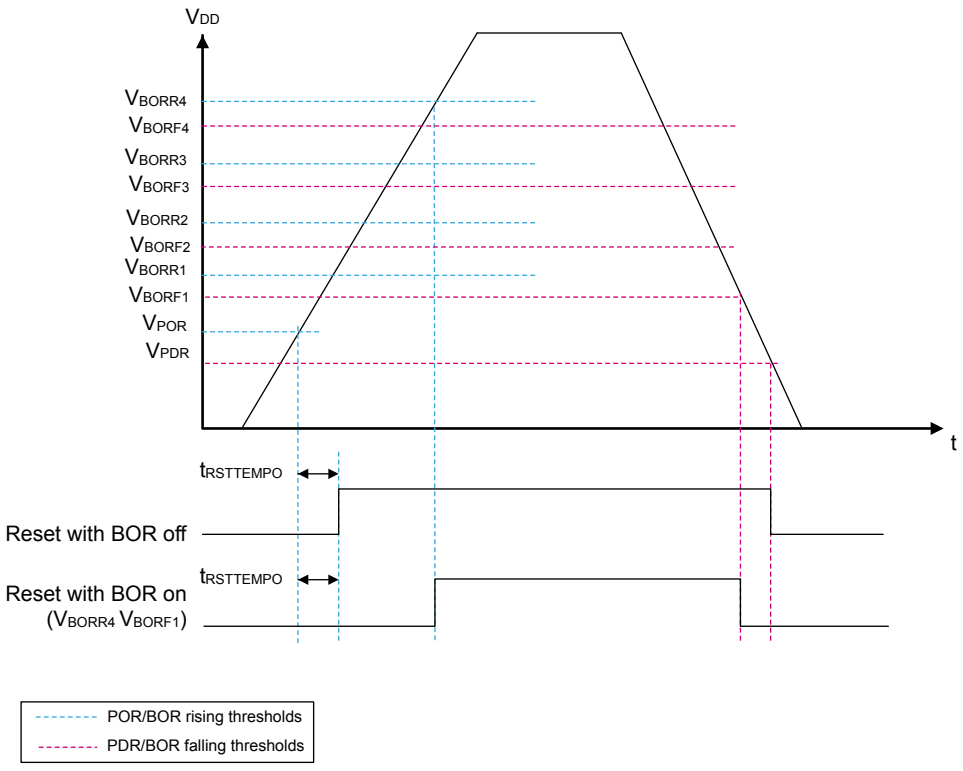
The BOR can be enabled or disabled only through option bytes. It is not available in Shutdown mode.

When the BOR is enabled, four BOR levels can be selected through option bytes, with independent configuration for rising and falling thresholds. During power-on, the BOR keeps the device under reset until the V_{DD} supply voltage reaches the specified BOR rising threshold (V_{BORRx}). At this point, the device reset is released and the system can start.

During power-down, when V_{DD} drops below the selected BOR falling threshold (V_{BORFx}), the device is put under reset again.

Note: It is not allowed to configure BOR falling threshold (V_{BORFx}) to a value higher than BOR rising threshold (V_{BORRx}).

Figure 2. POR, PDR, and BOR thresholds



Note: The reset temporization $t_{RSTTEMPO}$ starts when V_{DD} crosses V_{POR} threshold, indifferently from the configuration of the BOR option bits.

For more details on the brown-out reset thresholds, refer to the electrical characteristics section in the corresponding datasheet.

1.3 Reset

This section describes the three types of reset on microcontrollers of the STM32C0 series, namely power reset, system reset and RTC domain reset.

1.3.1 Power reset

A power reset is generated when one of the following events occurs:

- power-on reset (POR) or brown-out reset (BOR)
- exit from Standby mode
- exit from Shutdown mode

Power and brown-out reset set all registers to their reset values.

When exiting Standby mode, all registers in the V_{CORE} domain are set to their reset value. Registers outside the V_{CORE} domain (back up register, WKUP, IWDG, and Standby/Shutdown mode control) are not impacted.

When exiting Shutdown mode, the brown-out reset is generated, resetting all registers.

1.3.2 System reset

System reset sets all registers to their reset values, except for the reset flags in the RCC control/status register 2 (RCC_CSR2) and the registers in the RTC domain.

System reset is generated when one of the following events occurs:

- low level on the NRST pin (external reset)
- window watchdog event (WWDG reset)
- independent watchdog event (IWDG reset)
- software reset (SW reset)
- low-power mode security reset
- option byte loader reset
- power-on reset

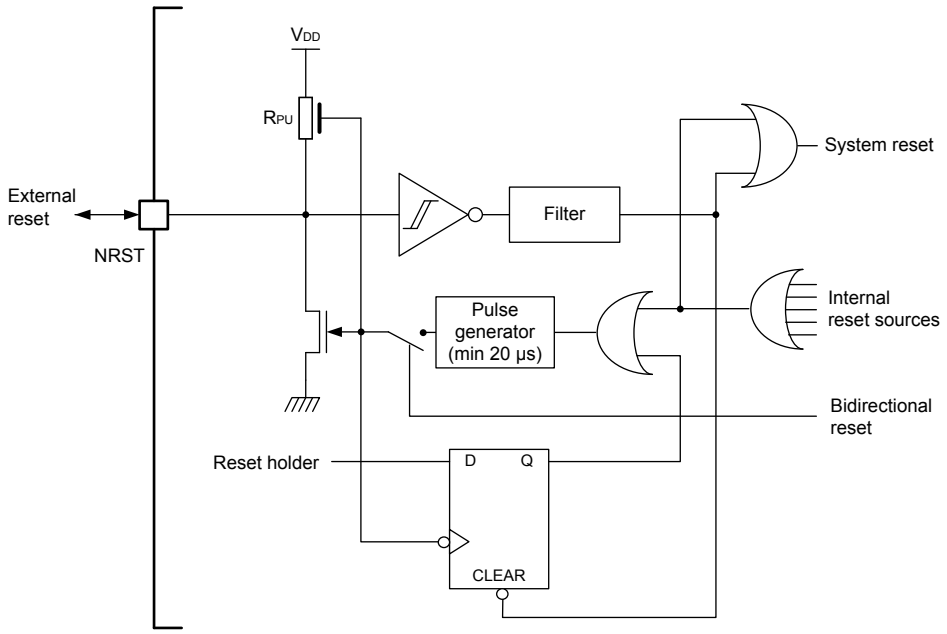
The reset source can be identified by checking the reset flags in the RCC_CSR2 register.

NRST pin (external reset)

Through specific option bits, the NRST pin is configurable to operate as:

- **Reset input/output** (default at device delivery)
  Valid reset signal on the pin is propagated to the internal logic. Each internal reset source is led to a pulse generator, whose output drives this pin. The GPIO functionality (PF2) is not available. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source to be output on the NRST pin. An internal reset holder option can be used, if enabled in the option bytes, to ensure that the pin is pulled low until its voltage meets V_{IL} threshold. This function makes possible the detection of internal reset sources by external components when the line faces a significant capacitive load.
- **Reset input**
  In this mode, any valid reset signal on the NRST pin is propagated to the device internal logic. Resets generated internally by the device are not visible on the pin. In this configuration, GPIO functionality (PF2) is not available.
- **GPIO**
  In this mode, the pin can be used as PF2 standard GPIO. The reset function of the pin is not available. Reset is only possible from device internal reset sources and it is not propagated to the pin.

Figure 3. **Simplified diagram of the reset circuit**



Note: Upon power reset or wake up from shutdown mode, the NRST pin is configured as Reset input/output and driven low by the system until it is reconfigured to the expected mode when the option bytes are loaded, in the fourth clock cycle after the end of $t_{rstempo}$.

Software reset

The SYSRESETREQ bit in the Cortex®-M0+ application interrupt and the reset control register must be set to force a software reset on the device (refer to the programming manual PM0223).

Low-power mode security reset

To prevent critical applications from mistakenly enter a low-power mode, three low-power mode security resets are available. If enabled in option bytes, the resets are generated in the following conditions:

- **Entering Standby mode**
  This type of reset is enabled by resetting nRST_STDBY bit in user option bytes. In this case, whenever a Standby mode entry sequence is successfully executed, the device is reset instead of entering Standby mode.
- **Entering Stop mode**
  This type of reset is enabled by resetting nRST_STOP bit in user option bytes. In this case, whenever a Stop mode entry sequence is successfully executed, the device is reset instead of entering Stop mode.
- **Entering Shutdown mode**
  This type of reset is enabled by resetting nRST_SHDW bit in user option bytes. In this case, whenever a Shutdown mode entry sequence is successfully executed, the device is reset instead of entering Shutdown mode.

Option byte loader reset

The option byte loader reset is generated when the OBL_LAUNCH bit (bit 27) is set in the FLASH_CR register. This bit is used to launch the option byte loading by software.

1.3.3 RTC domain reset

The RTC domain has two specific resets. An RTC domain reset is generated when one of the following events occurs:

- software reset, triggered by setting the RTCRST bit in the register RCC_CSR1
- V_{DD} power on

An RTC domain reset only affects the LSE oscillator, the RTC, and the register RCC_CSR1.

2 Clocks

The microcontrollers of the STM32C0 series provide the following clock sources producing primary clocks:

- **HSI48 RC**, a high-speed fully integrated RC oscillator producing HSI48 clock (48 MHz)
- **HSE OSC**, a high-speed oscillator with external crystal/ceramic resonator or external clock source, producing HSE clock (4 to 48 MHz)
- **LSI RC**, a low-speed fully integrated RC oscillator producing LSI clock (about 32 kHz)
- **LSE OSC**, a low-speed oscillator with external crystal/ceramic resonator or external clock source, producing LSE clock (accurate 32.768 kHz or external clock up to 1 MHz)
- **I2S_CKIN**, a pin for direct clock input for the I2S1 peripheral

Each oscillator can be switched on or off independently when it is not used, to optimize power consumption. Check the subsections of this section for more functional details. For electrical characteristics of the internal and external clock sources, refer to the device datasheet.

The device produces secondary clocks by dividing or/and multiplying the primary clocks:

- **HSISYS**, a clock derived from HSI48 through division by a factor programmable from 1 to 128.
- **SYSCLK**, a clock obtained through selecting one of the LSE, LSI, HSE, and HSISYS clocks.
- **HSIKER**, a clock derived from HSI48 through division by a factor programmable from 1 to 8.
- **HCLK**, a clock derived from SYSCLK through division by a factor programmable from 1 to 512.
- **HCLK8**, a clock derived from HCLK through division by eight.
- **PCLK**, a clock derived from HCLK through division by a factor programmable from 1 to 16.
- **TIMPCLK**, a clock derived from PCLK, running at PCLK frequency if the APB prescaler division factor is set to 1, or at twice the PCLK frequency otherwise.

Additional secondary clocks are generated by fixed division of HSE, HSI48, and HCLK clocks.

The HSISYS is used as a system clock source after startup from reset, with the division by four (producing 12 MHz frequency).

The HCLK clock and PCLK clock are used for clocking the AHB and the APB domains, respectively. Their maximum allowed frequency is 48 MHz.

The peripherals are clocked with the clocks from the bus that they are attached to (HCLK for AHB, PCLK for APB) except:

- **TIMx**, with:
  - TIMPCLK running at PCLK frequency if the APB prescaler division factor is set to 1, or at twice the PCLK frequency otherwise
- **USARTx**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSIKER
  - LSE
  - PCLK (APB clock)

  The wake-up from Stop mode is supported only when the clock is HSI48 or LSE.
- **ADC**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSIKER

  The wake-up from Stop mode is supported only when the clock is HSI48.
- **I2Cx**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSIKER
  - PCLK (APB clock)

  The wake-up from Stop mode is supported only when the clock is HSI48.
- **I2Sx**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSIKER
  - I2S_CKIN pin

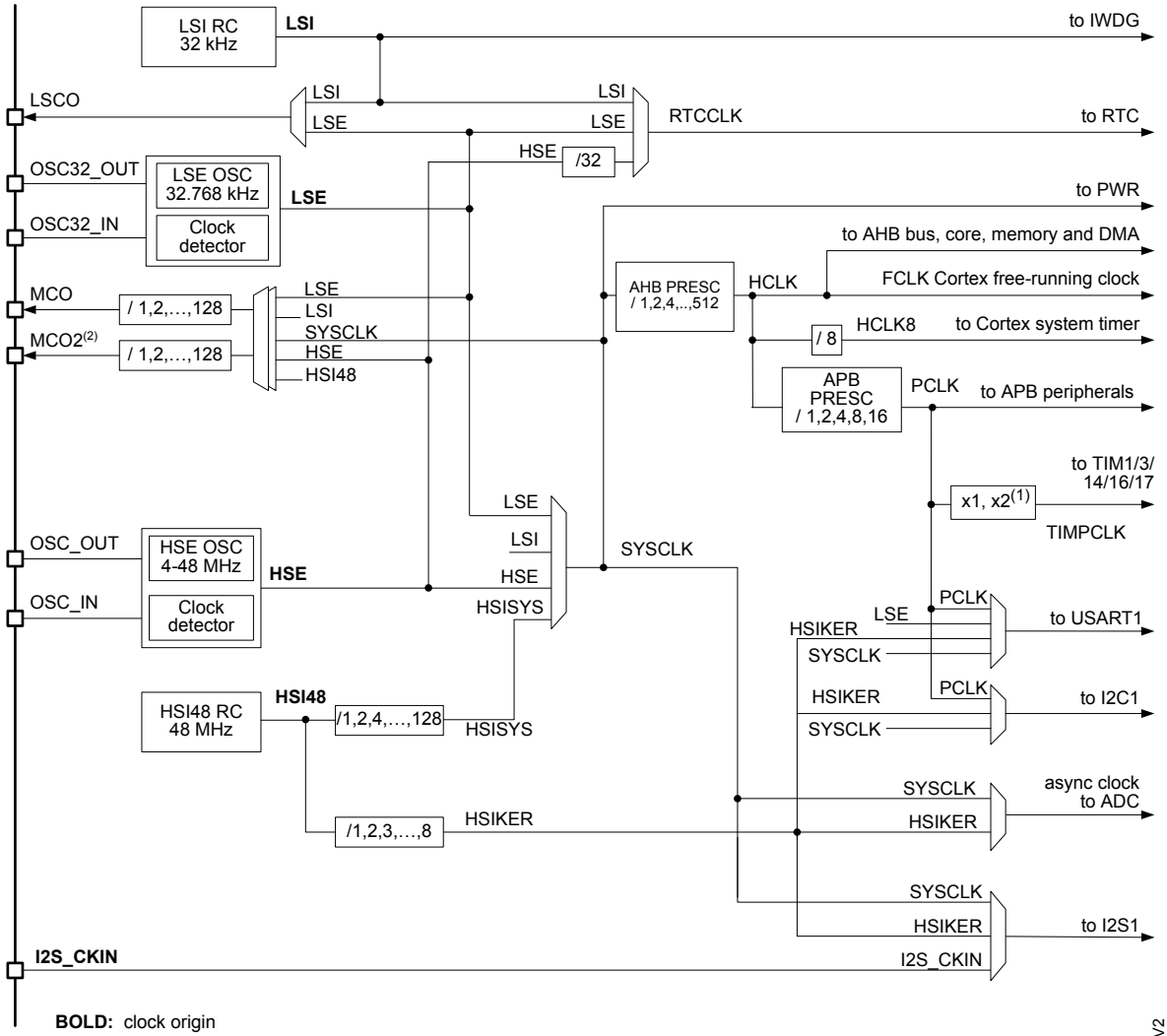
- **RTC**, with these clock sources to select from:
  - LSE
  - LSI
  - HSE clock divided by 32

  The functionality in Stop mode (including wake-up) is supported only when the clock is LSI or LSE.
- **IWDG**, always clocked with LSI clock.
- **SysTick** (Cortex® core system timer), with these clock sources to select from:
  - HCLK (AHB clock)
  - HCLK clock divided by 8

  The selection is done through SysTick control and status register.

HCLK is used as Cortex®-M0+ free-running clock (FCLK). For more details, refer to the programming manual PM0223.

Figure 4. Clock tree



BOLD: clock origin

(1) TIMPCLK is running at PCLK frequency if the APB prescaler division factor is set to 1, or at twice the PCLK frequency otherwise

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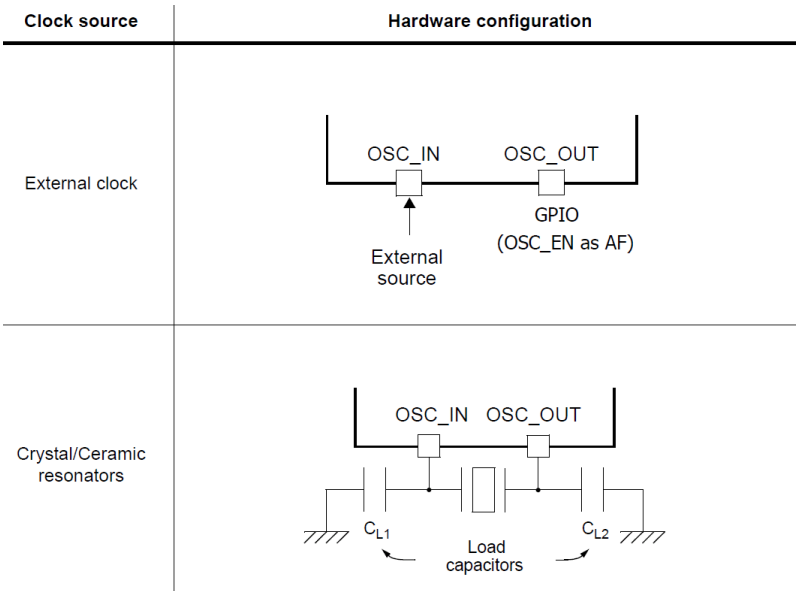
2.1 HSE clock

The high speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock

The resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Figure 5. HSE / LSE clock sources



External crystal/ceramic resonator (HSE crystal)

The 4 to 48 MHz external oscillator has the advantage of producing a very accurate rate on the main clock.

The associated hardware configuration is shown in Figure 5. Refer to the electrical characteristics section of the datasheet for more details.

The HSERDY flag in the clock control register (RCC_CR) indicates if the HSE oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the clock interrupt enable register (RCC_CIER).

The HSE crystal can be switched on and off using the HSEON bit in the clock control register (RCC_CR).

External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 48 MHz. This mode is selected by setting the HSEBYP and HSEON bits in the clock control register (RCC_CR). The external clock signal (square, sinus, or triangle) with around 40 to 60% duty cycle depending on the frequency (refer to the datasheet) must drive the OSC_IN pin, on devices where OSC_IN and OSC_OUT pins are available (see Figure 5).

The OSC_OUT pin can be used as a GPIO or it can be configured as OSC_EN alternate function, to provide an enable signal to the external clock synthesizer. It makes possible to stop the external clock source when the device enters low power modes.

Note: For details on pin availability, refer to the pinout section in the corresponding device datasheet.

To minimize the consumption, it is recommended to use the square signal.

2.2 HSI48 clock

The HSI48 clock signal is generated from an internal 48 MHz RC oscillator.

The HSI48 RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a startup time faster than the HSE crystal oscillator. However, even after calibration, it is less accurate than an oscillator using a frequency reference such as quartz crystal or ceramic resonator.

The HSISYS clock derived from HSI48 can be selected as system clock after wake up from Stop mode. It can also be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails.

Calibration

RC oscillator frequencies can vary from one chip to another due to manufacturing process variations. To compensate for this variation, each device is factory calibrated at T_A = 25°C.

After reset, the factory calibration value is loaded in the HSICAL[7:0] bits in the Internal clock source calibration register (RCC_ICSCR).

Voltage or temperature variations in the application may affect the HSI48 frequency of the RC oscillator. It can be trimmed using the HSITRIM[6:0] bits in the Internal clock source calibration register (RCC_ICSCR).

The HSIRDY flag in the Clock control register (RCC_CR) indicates if the HSI48 RC is stable or not. At startup, the HSI48 RC output clock is not released until this bit is set by hardware.

The HSI48 RC can be switched on and off using the HSION bit in the Clock control register (RCC_CR).

The HSI48 signal can also be used as a backup source (auxiliary clock) if the HSE crystal oscillator fails.

2.3 LSE clock

The LSE crystal is a 32.768 kHz crystal or ceramic resonator. It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The LSE crystal is switched on and off using the LSEON bit in the Control register 1 (RCC_CSR1). The crystal oscillator driving strength can be changed. It can be changed at runtime using the LSEDRV bit in the Control register 1 (RCC_CSR1) to obtain the best compromise between low-power-consumption on one side, and robustness and short startup time on the other side. The LSE drive can be decreased to its lower capability (LSEDRV cleared) when the LSE is ON. However, once LSEDRV is selected, the drive capability cannot be increased if LSEON = 1.

The LSERDY flag in the Control register 1 (RCC_CSR1) indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the clock interrupt enable register (RCC_CIER).

External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. This mode is selected by setting the LSEBYP and LSEON bits in the AHB peripheral clock enable in the Sleep/Stop mode register (RCC_AHBSMENR). The external clock signal (square, sinus, or triangle) with around 50% duty cycle has to drive the OSCX_IN pin while the OSCX_OUT pin can be used as GPIO. See Figure 5.

2.4 LSI clock

The LSI RC acts as a low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG) and RTC. The clock frequency is 32 kHz. For more details, refer to the electrical characteristics section of the datasheets.

The LSI RC can be switched on and off using the LSION bit in the Control/status register 2 (RCC_CSR2).

The LSIRDY flag in the Control/status register 2 (RCC_CSR2) indicates if the LSI oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the clock interrupt enable register (RCC_CIER).

2.5 System clock (SYSCLK) selection

One of the following clocks can be selected as system clock (SYSCLK):

- LSI
- LSE
- HSISYS
- HSE

The maximum frequency of the system clock is 48 MHz. Upon system reset, the HSISYS clock derived from the HSI48 oscillator is selected as system clock. When a clock source is used as a system clock, it is not possible to stop it.

A switch from one clock source to another occurs only if the target clock source is ready (clock stable after startup delay). If a clock source that is not yet ready is selected, the switch occurs when the clock source becomes ready. Status bits in the internal clock sources calibration register (RCC_ICSCR) indicate which clock(s) is (are) ready and which clock is currently used as a system clock.

2.6 Clock security system (CSS)

Software can activate the clock security system. In this case, the clock detector is enabled after the HSE oscillator startup delay. It is disabled when this oscillator is stopped.

If a failure is detected on the HSE clock:

- the HSE oscillator is automatically disabled
- a clock failure event is sent to the break input of TIM1, TIM16, and TIM17 timers
- CSSI (clock security system interrupt) is generated

The CSSI is linked to the Cortex®-M0+ NMI (nonmaskable interrupt) exception vector. It makes the software aware of an HSE clock failure to allow it to perform rescue operations.

Note: If the CSS is enabled and the HSE clock fails, the CSSI occurs and an NMI is automatically generated. The NMI is executed infinitely unless the CSS interrupt pending bit is cleared. It is therefore necessary that the NMI ISR clears the CSSI by setting the CSSC bit in the clock interrupt clear register (RCC_CICR).

If HSE is selected directly or indirectly as system clock, and a failure of the HSE clock is detected, the system clock switches automatically to HSISYS and the HSE oscillator is disabled.

2.7 Clock security system for LSE clock (LSECSS)

A clock security system on LSE can be activated by setting the LSECSSON bit in Control register 1 (RCC_CSR1). This bit can be cleared only by a hardware reset or RTC software reset, or after LSE clock failure detection. LSECSSON must be written after LSE and LSI are enabled (LSEON and LSION enabled) and ready (LSERDY and LSIRDY flags set by hardware), and after selecting the RTC clock by RTCSEL.

The LSECSS works in all modes except Standby and Shutdown. It keeps working also under system reset (excluding power-on reset). If a failure is detected on the LSE oscillator, the LSE clock is no longer supplied to the RTC, but its registers are not impacted.

Note: If the LSECSS is enabled and the LSE clock fails, the LSECSSI occurs and an NMI is automatically generated. The NMI is executed infinitely unless the LSECSS interrupt pending bit is cleared. It is therefore necessary that the NMI ISR clears the LSECSSI by setting the LSECSSC bit in the clock interrupt clear register (RCC_CICR).

If LSE is used as system clock, and a failure of LSE clock is detected, the system clock switches automatically to LSI. In low-power modes, an LSE clock failure generates a wake-up. The interrupt flag must then be cleared within the RCC registers.

The software must then disable the LSECSSON bit, stop the defective 32 kHz oscillator (by clearing LSEON), and change the RTC clock source (no clock, LSI or HSE, with RTCSEL), or take any appropriate action to secure the application.

The frequency of the LSE oscillator must exceed 30 kHz to avoid false positive detections.

2.8 ADC clock

The ADC clock (refer to the device datasheet for maximum frequency) is derived from the system clock or from the kernel clock output. It can be prescaled by 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128 or 256, by configuring the ADC1_CCR register. This clock is asynchronous to the AHB clock. Alternatively, the ADC clock can be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). This programmable factor is configured using the CKMODE bitfields in the ADC1_CCR.

If the programmed factor is 1, the AHB prescaler must be set to 1.

2.9 RTC clock

The RTCCLK clock source can be either the HSE/32, LSE or LSI clock. It is selected by programming the RTCSEL[1:0] bits in the Control register 1 (RCC_CSR1). This selection cannot be modified without resetting the RTC domain. The system must always be configured so as to get a PCLK frequency greater than or equal to the RTCCLK frequency for proper RTC operation.

RTC does not operate if the V_{DD} supply is powered off or if the internal voltage regulator is powered off (removing power from the V_{CORE} domain). When the RTC clock is LSE or LSI, the RTC remains clocked and functional under system reset.

When the RTC clock is LSE or LSI, the RTC remains clocked and functional under system reset.

2.10 Timer clock

The timer clock TIMPCLK is derived from PCLK (used for APB). If the APB prescaler is set to 1, the TIMPCLK frequency is equal to the PCLK frequency. Otherwise, the TIMPCLK frequency is set to twice the PCLK frequency.

2.11 Watchdog clock

If a hardware option or software access starts the independent watchdog (IWDG), the LSI oscillator is forced ON, and cannot be disabled. After the LSI oscillator temporization, the clock is provided to the IWDG.

2.12 Clock-out capability

MCO and MCO2

These pins output, independently of each other, the clock selected from:

- LSI
- LSE
- SYSCLK
- HSI48
- HSE

The multiplexers for MCO and MCO2 are controlled, respectively, by the MCOSEL[2:0] and MCO2SEL[2:0] bitfields of the Clock configuration register (RCC_CFGR). Their outputs are further divided by a factor set through the MCOPRE[2:0] and MCO2PRE[2:0] bitfields of the Clock configuration register (RCC_CFGR).

LCO

The LSCO pin allows outputting of low-speed clocks:

- LSI
- LSE

The selection is controlled by the LSCOSEL bit, and enabled with the LSCOEN bit of the Control register 1 (RCC_CSR1). The configuration registers of the corresponding GPIO port must be programmed in alternate function mode. This function remains available in Stop mode.

2.13 Internal / external clock measurement with TIM14 / TIM16 / TIM17

It is possible to indirectly measure the frequency of all on-board clock sources with the TIM14, TIM16, and TIM17 channel 1 input capture, as shown in the figures in each of the corresponding subsections.

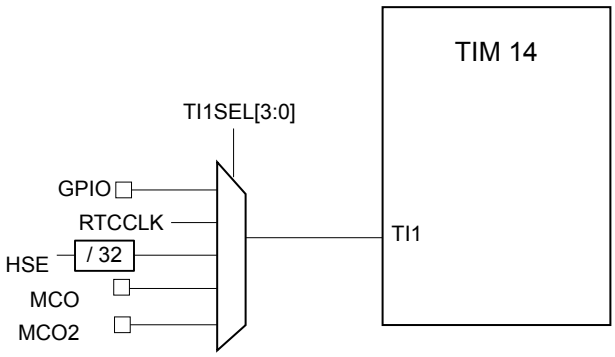
TIM14

By setting the TI1SEL[3:0] field of the TIM14_TISEL register, the clock selected for the input capture channel1 of TIM14 can be one of the following:

- GPIO (refer to the alternate function mapping in the device datasheets)
- RTC clock (RTCCLK)
- HSE clock divided by 32
- MCO (MCU clock output)
- MCO2 (MCU clock output)

MCO and MCO2 are controlled, respectively, by the MCOSEL[3:0] and MCO2SEL[3:0] bitfields of the clock configuration register (RCC_CFGR). All clock sources can be selected for the MCO and MCO2 pins.

Figure 6. Frequency measurement with TIM14 in capture mode



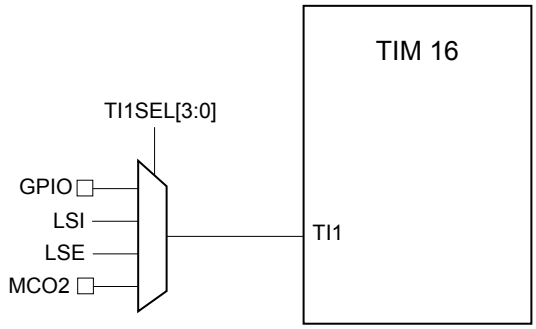
TIM16

By setting the TI1SEL[3:0] field of the TIM16_TISEL register, the clock selected for the input capture channel1 of TIM16 can be one of the following:

- GPIO (refer to the alternate function mapping in the device datasheets)
- LSI clock
- LSE clock
- MCO2

MCO2 is controlled by the MCO2SEL[3:0] bitfield of the clock configuration register (RCC_CFGR). All clock sources can be selected for the MCO2 pin.

Figure 7. Frequency measurement with TIM16 in capture mode



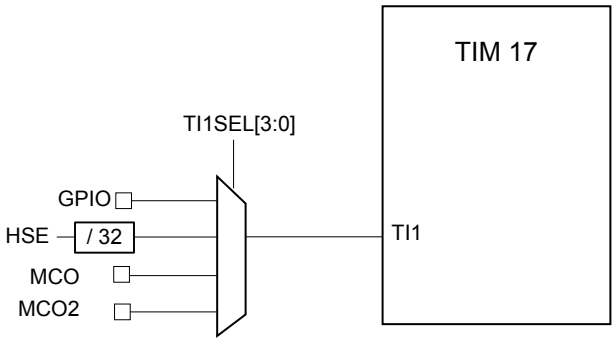
TIM17

By setting the TI1SEL[3:0] field of the TIM17_TISEL register, the clock selected for the input capture channel1 of TIM17 can be one of the following:

- GPIO (refer to the alternate function mapping in the device datasheets)
- HSE divided by 32
- MCO (MCU clock output)
- MCO2 (MCU clock output)

MCO and MCO2 are controlled, respectively, by the MCOSEL[3:0] and MCO2SEL[3:0] bitfields of the clock configuration register (RCC_CFGR). All clock sources can be selected for the MCO and MCO2 pins.

Figure 8. Frequency measurement with TIM17 in capture mode



Calibration of the HSI48 oscillator

For TIM14, TIM16 and TIM17, the primary purpose of connecting the LSE to the channel 1 input capture is to be able to precisely measure the HSISYS clock (derived from HSI48) selected as system clock. Counting HSISYS clock pulses between consecutive edges of the LSE clock (the time reference) allows measuring the HSISYS (and HSI48) clock period. Such measurement can determine the HSI48 oscillator frequency with nearly the same accuracy as the accuracy of the 32.768 kHz quartz crystal used with the LSE oscillator (typically a few tens of ppm). The HSI48 oscillator can then be trimmed to compensate for deviations from target frequency, due to manufacturing, process, temperature and/or voltage variation.

The HSI48 oscillator has dedicated user-accessible calibration bits for this purpose.

The basic concept consists in providing a relative measurement (for example, the HSISYS/LSE ratio): the measurement accuracy is therefore closely related to the ratio between the two clock sources. Increasing the ratio improves the measurement accuracy.

Generated by the HSE oscillator, the HSE clock (divided by 32) used as time reference is the second best method for reaching a good HSI48 frequency measurement accuracy. It is recommended in the absence of the LSE clock.

To further improve the precision of the HSI48 oscillator calibration, it is advised to employ one, or a combination of the following measures, to increase the frequency measurement accuracy:

- set the HSISYS divider to 1 for HSISYS frequency to be equal to HSI48 frequency,
- average the results of multiple consecutive measurements,
- use the input capture prescaler of the timer (1 capture every up to eight periods).

Calibration of the LSI oscillator

The calibration of the LSI oscillator uses the same principle as that for calibrating the HSI48 oscillator. TIM16 channel1 input capture must be used for LSI clock, and HSE selected as the system clock source. The number of HSE clock pulses between consecutive edges of the LSI signal, counted by TIM16, is then representative of the LSI clock period.

2.14 Peripheral clock enable registers

Each peripheral clock can be enabled by the corresponding enable bit of the RCC_AHBENR or RCC_APBENRx registers.

When the peripheral clock is not active, the peripheral registers read or write accesses are not supported.

Note: The enable bit has a synchronization mechanism to create a glitch-free clock for the peripheral. After the enable bit is set, there is a 2-clock-cycle delay for the clock to be active. The software must take into account this delay.

3 Boot configuration

Three different boot modes can be selected through the BOOT0 pin, the BOOT_LOCK bit in the FLASH_SECR register, and the boot configuration bits nBOOT1, BOOT_SEL, and nBOOT0 in the user option byte, as shown in the following table.

Table 2. Boot modes

Boot mode configuration					Selected boot area
BOOT_LOCK	nBOOT1 bit	BOOT0 pin	nBOOT_SEL bit	nBOOT0 bit	
0	X	0	0	X	Main flash memory
0	1	1	0	X	System memory
0	0	1	0	X	Embedded SRAM
0	X	X	1	1	Main flash memory
0	1	X	1	0	System memory
0	0	X	1	0	Embedded SRAM
1	X	X	X	X	Main flash memory

The boot mode configuration is latched on the fourth rising edge of SYSCLK after a reset. It is up to the user to set the boot mode configuration related to the required boot mode.

The boot mode configuration is also resampled when exiting from Standby mode. Consequently, they must be kept in the required Boot mode configuration in Standby mode.

After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, then starts code execution from the boot memory at 0x0000 0004.

Depending on the selected boot mode, main flash memory, system memory or SRAM is accessible as follows:

- Boot from main flash memory: the main flash memory is aliased in the boot memory space (0x0000 0000). But it is still accessible from its original memory space (0x0800 0000). In other words, the flash memory content can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from system memory: the system memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space 0x1FFF0000.
- Boot from the embedded SRAM: the SRAM is aliased in the boot memory space (0x0000 0000), but it is still accessible from its original memory space (0x2000 0000).

Forcing boot from the user flash memory

The BOOT_LOCK bit enables forcing a unique entry point in the main flash memory for boot, regardless of the other boot mode configuration bits.

Empty check

Internal empty check flag (the EMPTY bit of the flash access control register (FLASH_ACR)) is implemented to allow easy programming of virgin devices by the bootloader. This flag is used when BOOT0 pin is defining Main flash memory as the target boot area. When the flag is set, the device is considered as empty. System memory (bootloader) is selected, instead of the Main Flash, as a boot area to allow the user to program the flash memory.

This flag is updated only during Option bytes loading: it is set when the content of the address 0x08000 0000 is read as 0xFFFF FFFF, otherwise it is cleared. It means a power reset or setting of the OBL_LAUNCH bit in the FLASH_CR register is needed to clear this flag after programming of a virgin device to execute the user code after the system reset. The software can also directly write the EMPTY bit.

Note: If the device is programmed for a first time but the option bytes are not reloaded, the device still selects the system memory as a boot area after a system reset.

Physical remap

Once the boot mode is selected, the application software can modify the memory accessible in the code area. This modification is performed by programming the MEM_MODE bits in the SYSCFG configuration register 1 (SYSCFG_CFGR1).

Embedded bootloader

The embedded bootloader is located in the system memory, programmed by STMicroelectronics during production. It is used to reprogram the flash memory using one of the following serial interfaces:

- USART1
- I2C1

For further details, refer to application note *STM32 microcontroller system memory boot mode* (AN2606 available on).

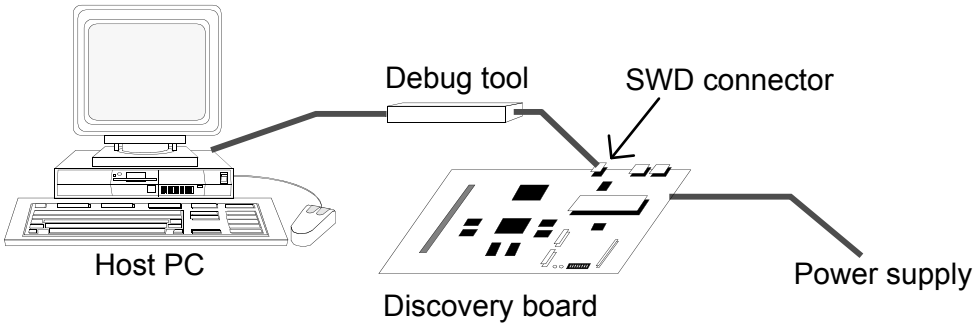
4 Debug management

4.1 Introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, an SWD connector and a cable connecting the host to the debug tool.

Figure 9 shows the connection of the host to the discovery board (STM32C0316-DK), which embeds the debug tools (ST-LINK). Consequently, it can be directly connected to the PC through a USB cable.

Figure 9. Host-to-board connection



4.2 SWD (serial wire debug) port

The STM32C0 series core integrates the serial wire debug port (SW-DP), an Arm®standard CoreSight™ debug port with a 2-pin (clock + data) interface to the debug access port.

4.3 Pinout and debug port pins

The microcontrollers of the STM32C0 series are offered in packages with varying numbers of pins.

4.3.1 Serial wire debug (SWD) pin assignment

The same SWD pin assignment is available on all STM32C0 Series packages.

Table 3. SWD port pins

SWD pin name	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	I/O	Serial wire data input/output	PA13
SWCLK	I	Serial wire clock	PA14

After reset (SYSRESETn or PORESETn), the pins used for the SWD are assigned as dedicated pins, immediately usable by the debugger host.

The MCU offers the possibility to disable the SWD, therefore releasing the associated pins for general-purpose I/O (GPIO) usage. For more details on how to disable SWD port, refer to the RM0490 section on I/O pin alternate function multiplexer and mapping.

4.3.2 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of these pins. The reset states of the GPIO control registers put the I/Os in the equivalent states:

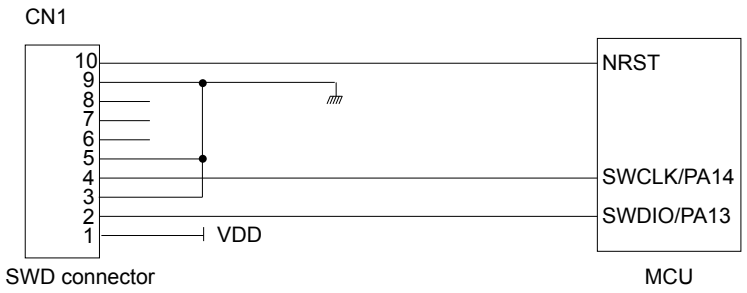
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

4.3.3 SWD port connection with standard SWD connector

Figure 10 shows the connection between the MCU and a standard SWD connector.

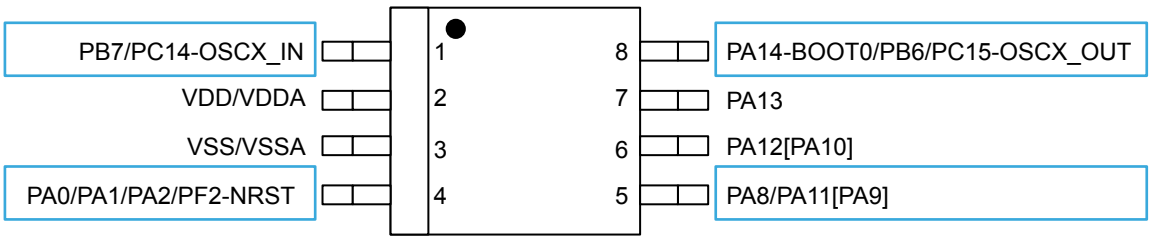
Figure 10. SWD port connection



4.3.4 Multi bonding on small packages

A multi-bonding approach is used on the small packages to offer a maximum of alternate functions and analog inputs. This approach results in multiple die pads connected internally to a single package pin. As an example, in Figure 11 there are four pads bonded to each of the pins 1, 4, 5 and 8. Multi bonding for pin 1 means that each of the alternate functions (PB7 and PC14) is accessible on this pin if respectively configured at I/O port level.

Figure 11. Multi bonding example



A design protection is implemented to avoid pad interferences due to multi-bonding. This protection is achieved through a dedicated SYSCFG_CFGR3 register in the System controller, which makes possible to select which IO of a multi-bonding group is active. The other IOs are in digital input mode to avoid conflicts with the selected IO. This register is taken into account if SECURE_MUXING_EN bit of the FLASH_OPTR register is set to 1.

This protection can be deactivated by resetting the bit SECURE_MUXING_EN in the FLASH_OPTR register. In this case, to ensure correct functionalities and avoid electrical damages, software must cautiously program all pads bonded to the same package pin. If the SECURE_MUXING_EN bit in the FLASH_OPTR register is reset (protection bypassed), all the pads linked to one pin are active and can be set in the mode specified by the corresponding GPIOx_MODER register. The user has to ensure that there are no conflicts between GPIOs.

By default, all GPIOs (except PA14 in this example) are configured in analog input; this must be taken into consideration before modifying the analog input configuration for another configuration state.

The multi bonding approach offers not only more versatility for the product configuration, but also offers an extended drive strength on the multi bonded pads. By configuring multiple devices pad in output mode (with the same output level), the transistor drive resistance is decreased and consequently the voltage drop (V_{OL} and V_{OH}) at the device pin is reduced. The transition from high to low level must be done with caution to guarantee that no short circuits are produced between the internal die pads.

5 Recommendations

5.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

5.2 Component position

A preliminary layout of the PCB must make separate circuits:

- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution. This reduces cross-coupling on the PCB that introduces noise.

5.3 Ground and power supply (V_{DD})

Every block (noisy, low-level sensitive or digital) must be grounded individually and all ground returns must be to a single point. Loops must be avoided or their area has to be minimized. To improve analog performance, the decoupling capacitors must be placed as close as possible to the device.

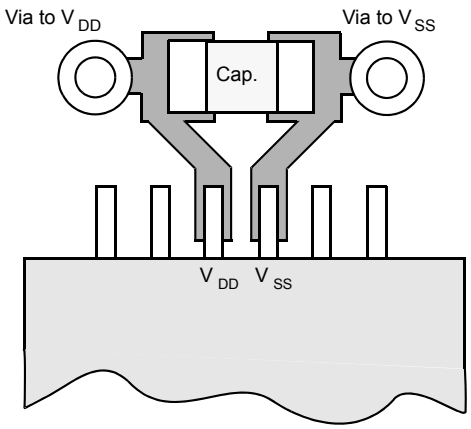
The power supply must be implemented close to the ground line to minimize the area of supply loops. This is because the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a shield (especially when using single-layer PCBs).

5.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks, and vias must have the lowest possible impedance. This is typically achieved with thick track widths and, preferably, with the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair must be decoupled with 100 nF filtering ceramic capacitor and a chemical capacitor of about 4.7 µF connected between the supply pins of the device. These capacitors need to be placed as close as possible to or below the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. Figure 12 shows the typical layout of such a pair.

Figure 12. Typical layout for VDD / VSS pair



5.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently. Such as interrupts and handshaking strobe signals, but not LED commands. For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve the EMC performance.
- Digital signals: the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (such as clock)
- Sensitive signals (such as high-Z)

5.6 Unused I/O and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

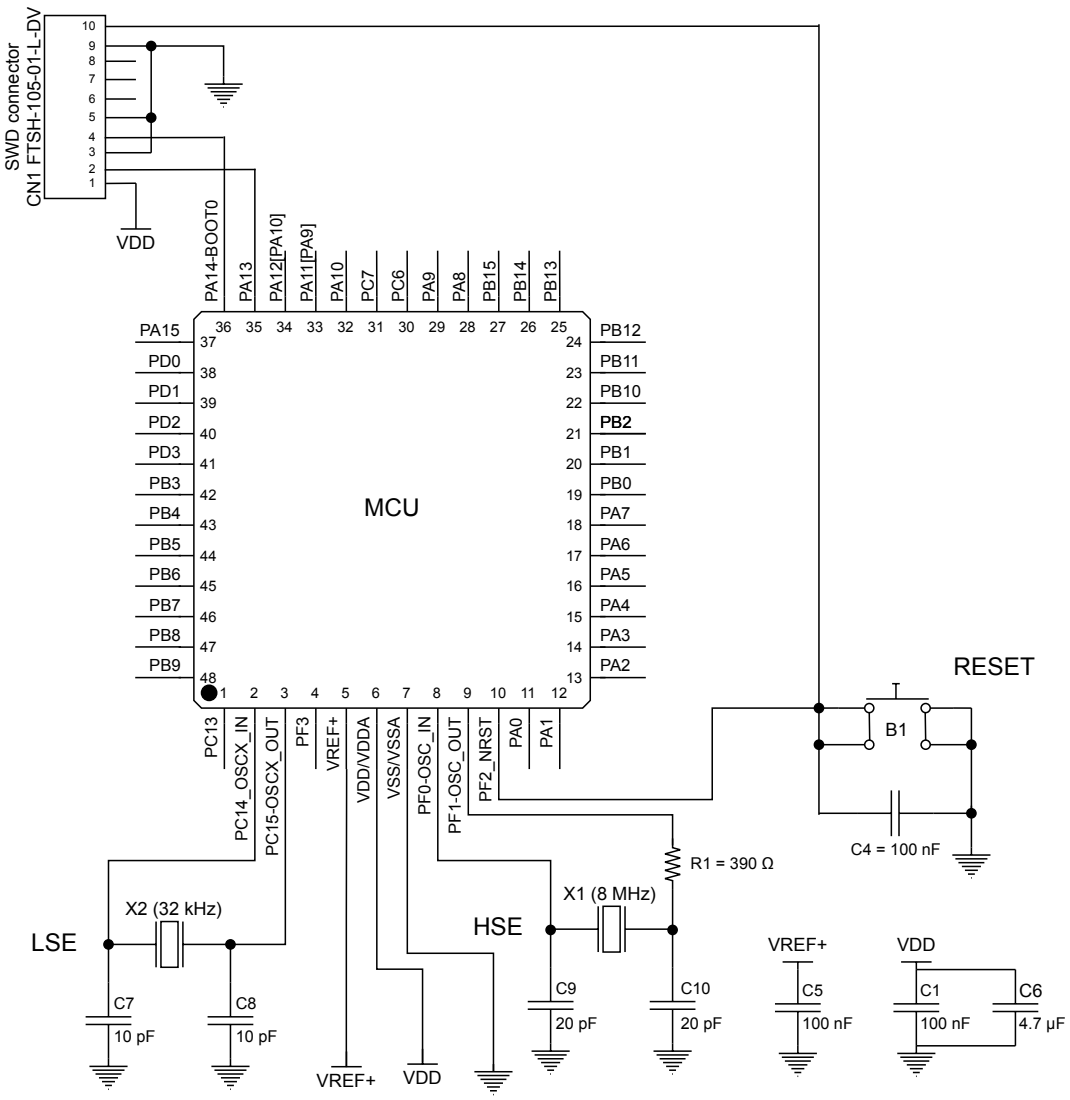
To increase EMC performance and avoid extra power consumption, unused clocks, counters, or I/Os, should not be left free. I/Os should be connected to a fixed logic level of 0 or 1 by an external or internal pull-up or pull-down on the unused I/O pin. The other option is to configure GPIO as output mode using software. Unused features should be frozen or disabled, which is their default value.

6 Reference design

6.1 Description of reference design

The reference design shown in the figure below is based on STM32C031, a highly integrated microcontroller running at 48 MHz, combining the Cortex®-M0+ 32-bit RISC CPU core with 32 Kbytes of embedded flash memory and 12 Kbytes of SRAM.

Figure 13. STM32C0 series reference schematic



The values of capacitors used in combination with X1 and X2 must be chosen according to crystal specifications (the values indicated for C7, C8, C9, and C10 are given only as an example). To keep a stable NRST signal, the PCB layout must feature C4 as close as possible to pin 10 (PF2_NRST).

Note: On packages where both OSC_IN/OSC_OUT and OSCX_IN/OSCX_OUT are available, if both LSE and HSE need to be implemented, the HSE_NOT_REMAPPED bit of the FLASH_OPTR register must be set (default case).

6.1.1 Clock

Two clock sources are used:

- HSE: X1, an 8 MHz crystal for the microcontroller
- LSE: X2, a 32.768 kHz crystal for the embedded RTC

Refer to Section 2 Clocks.

6.1.2 Reset

The reset signal in Figure 13 is active low. The reset sources include the reset button (B1) and the debugging tools via the connector CN1. Refer to Section 1.3 Reset.

Note: By default the reset holder is activated on STM32C0 series devices. Any internal reset results in pulling down NRST pin until it reaches its V_{IL} threshold, ensuring that the capacity on this line is fully discharged.

6.1.3 Boot mode

The boot option is configured by default through option bytes. BOOT0 pin can be used if user wants to have a physical control on boot entry point after reprogramming the option byte.

6.1.4 SWD interface

The reference design shows the connection between an MCU of the STM32C0 Series and a standard SWD connector. Refer to Section 4 Debug management.

Note: It is recommended to connect the reset pin to be able to reset the application from the tool.

6.1.5 Power supply

Refer to Section 1.1 Power supplies.

6.1.6 Pinouts and pin description

Refer to the datasheets available on *www.st.com* for the pinout information and pin description of each device.

6.2 Component references

Table 4. Mandatory components

Component	Reference	Value	Quantity	Comments
Microcontroller	U1	STM32C031CxT	1	48-pin package
Capacitor	C1	100 nF	1	Ceramic capacitors (for decoupling)
Capacitor	C6	4.7 µF	1	Used for VDD

Table 5. Optional components

Component	Reference	Value	Quantity	Comments
Resistor	R1	390 Ω	1	Used for HSE, the value depends on the crystal characteristics
Capacitor	C4	100 nF	1	Ceramic capacitor for RESET button
Capacitor	C5	100 nF	1	Ceramic capacitors (for decoupling)
Capacitor	C7/C8	10 pF	2	Used for LSE, the value depends on the crystal characteristics
Capacitor	C9/C10	20 pF	2	Used for HSE, the value depends on the crystal characteristics
Quartz	X1	8 MHz	1	Used for HSE
Quartz	X2	32 kHz	1	Used for LSE
Push-button	B1	-	1	Used as reset button
SWD connector	CN1	FTSH-105-01-L-DV	1	Used for program/debug

Revision history

Table 6. **Document revision history**

Date	Version	Changes
06-Jun-2022	1	Initial release.
14-Dec-2022	2	• Updated the Table 1. Power supplies of STM32C0 series Updated the Figure 1. STM32C0 series power supply Updated the Section 2 Clocks Updated the Figure 4. Clock tree • Generated a public version of the document.

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