ZYNQ-7000 SOM B'd (Rev.A)

[1] Index

Rev	Date	Designer	Description
A	24.05.03	Ganghyeok Lim	Create design project

Index

Title	ZYNQ-7000 SOM Bd.PrjPcb	Rev *
Doc	01_Index.SchDoc	
Sheet # 1 of 9	Author *	
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[2] Overview

Title	**ZYNQ-7000 SOM Bd.PrjPcb**	Rev *****
Doc	**02_Overview.SchDoc**	
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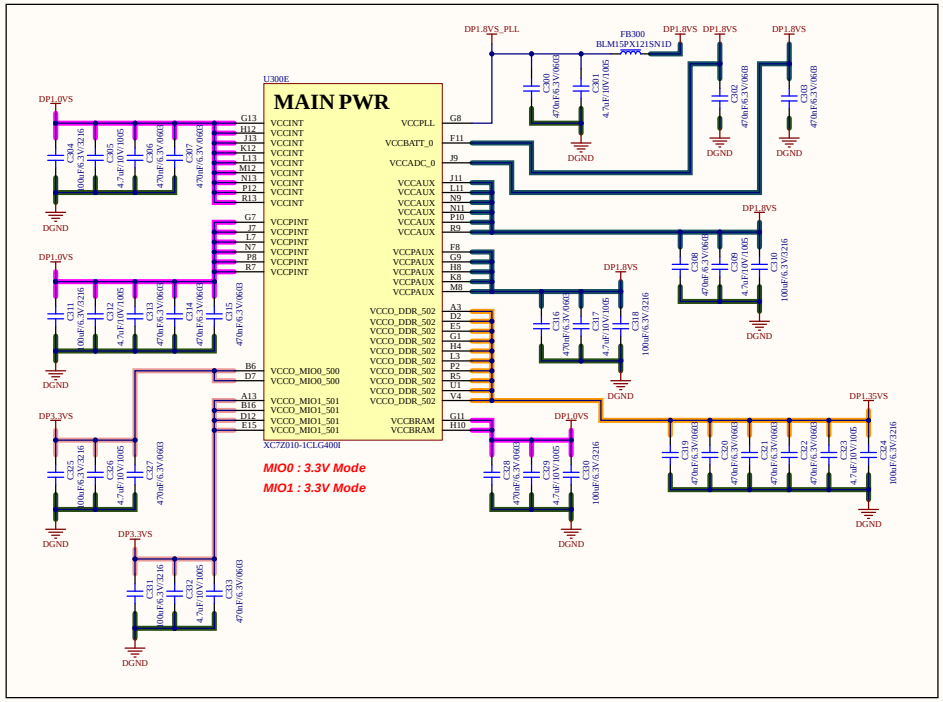
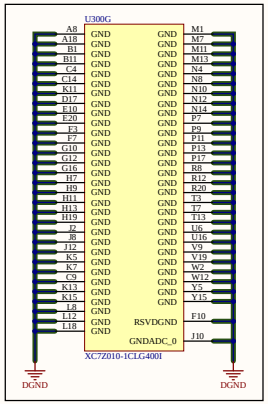
[3] ZYNQ Power & Decoupling

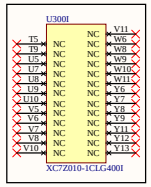
Main Supplies (INT, AUX, DDR, MIO)



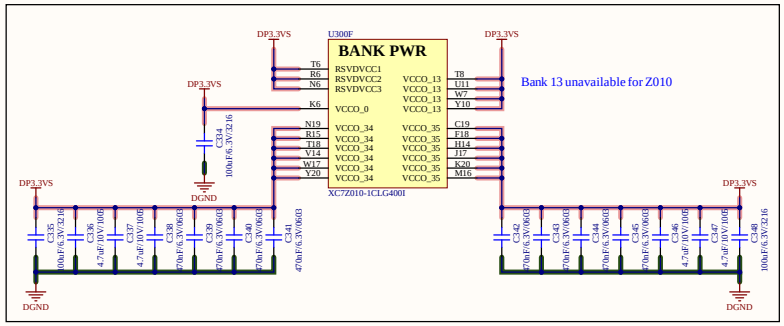
GND Connections



Unused Pins



Bank Supplies (0, 34, 35)



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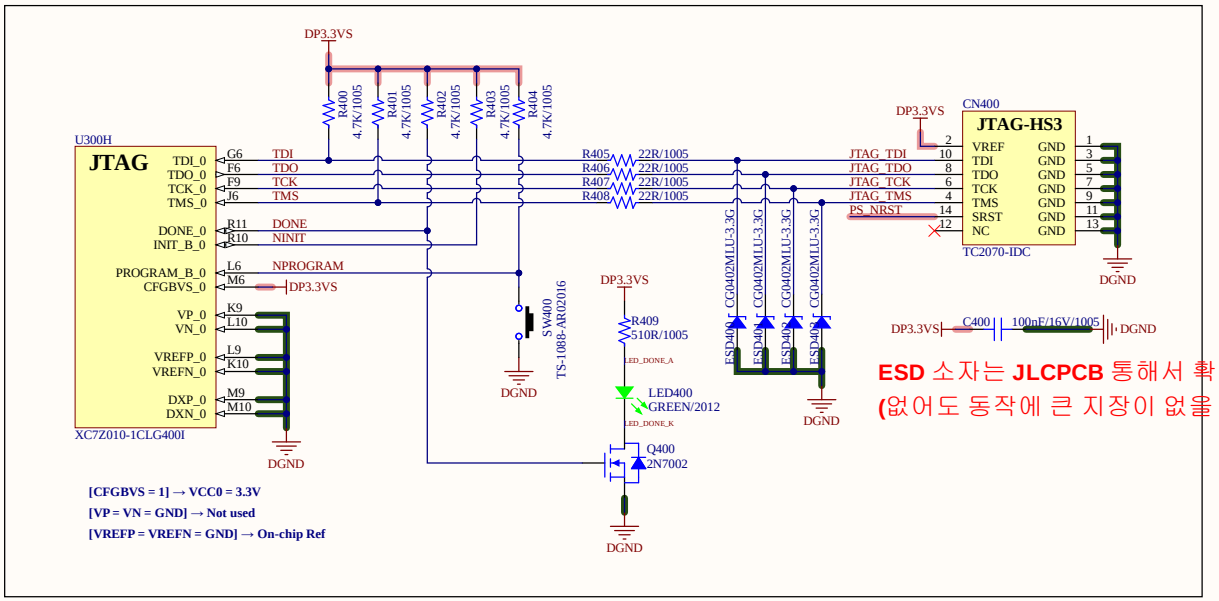
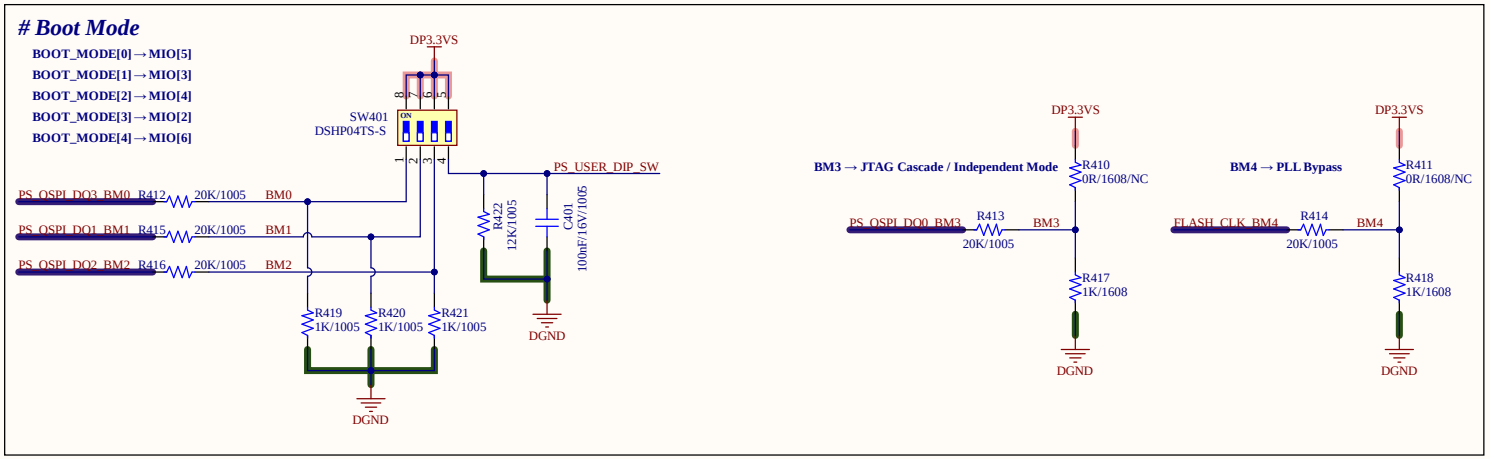
[4] ZYNQ Config

Zynq Config, JTAG



ESD 소자는 **JLCPCB** 통해서 확보중인데, 예상 확보 일자는 **5/10** 이다.
(없어도 동작에 큰 지장이 없을 것으로 판단됨**/ Digilent CMOD**에 **ESD** 소자 달려있는지 확인해볼 것**.** 거가는 **USB**로함**)**

Boot Mode MIO Strapping Pins (UG585 p167)



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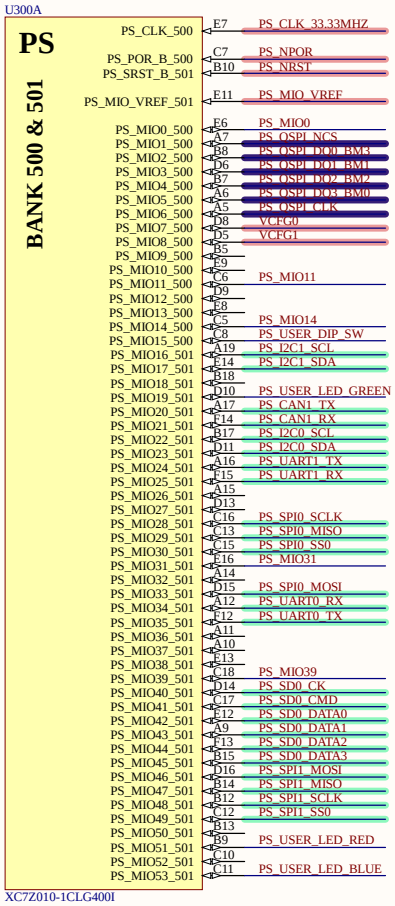
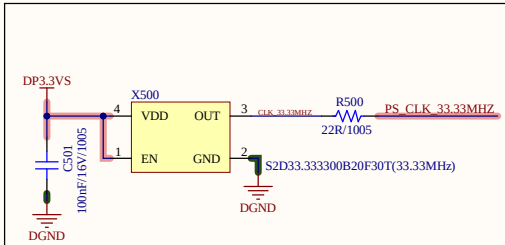
[5] ZYNQ Processing System (PS)

ZYNQ PS (BANK 500 / 501)

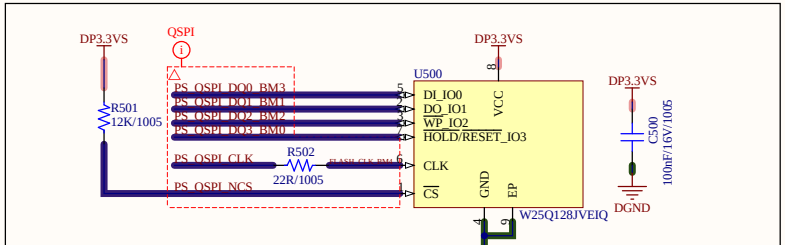


PS Clock (33.33 MHz)



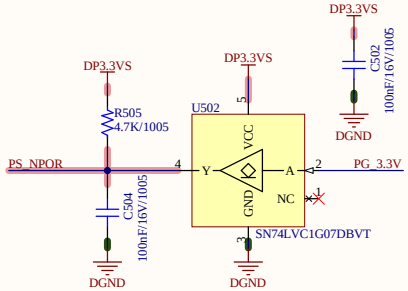
Pin Description : Refer to UG865 p14 (PS_CLK)

QSPI Flash Memory (128Mbit)



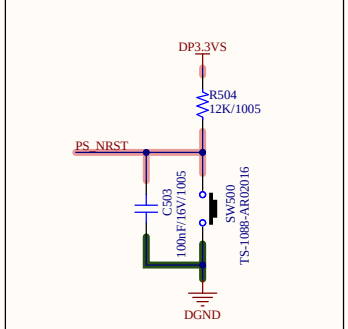
16 MByte

Power on Reset



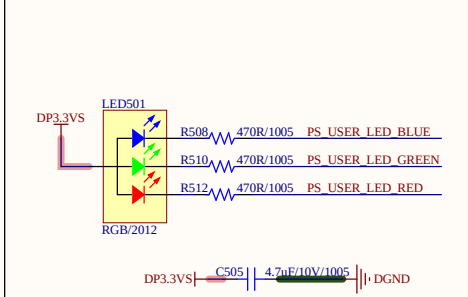
Pin Description : Refer to UG865 p14 (PS_POR_B)

System Reset Switch



Pin Description : Refer to UG865 p14 (PS_SRST_B)

PS Status LED

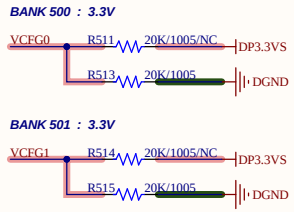


Pin Description : Refer to UG865 p14 (PS_MIO[53:0])

MIO Bank Voltage Mode Config

VCFG : 0 → BANK : 2.5V or 3.3V
VCFG : 1 → BANK : 1.8V

Pin Description : Refer to UG585 p167 (VMODE[1,0])



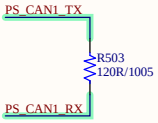
For Detail, Refer to UG933 p56-57

PS_MIO_VREF Config

"PS_MIO_VREF" is for RGMII interface.
Therefore if it is not used, the pin is safe to float

Pin Description : Refer to UG865 p14 (PS_MIO_VREF)
Refer to UG933 p57

PS_CAN Term. Resistor



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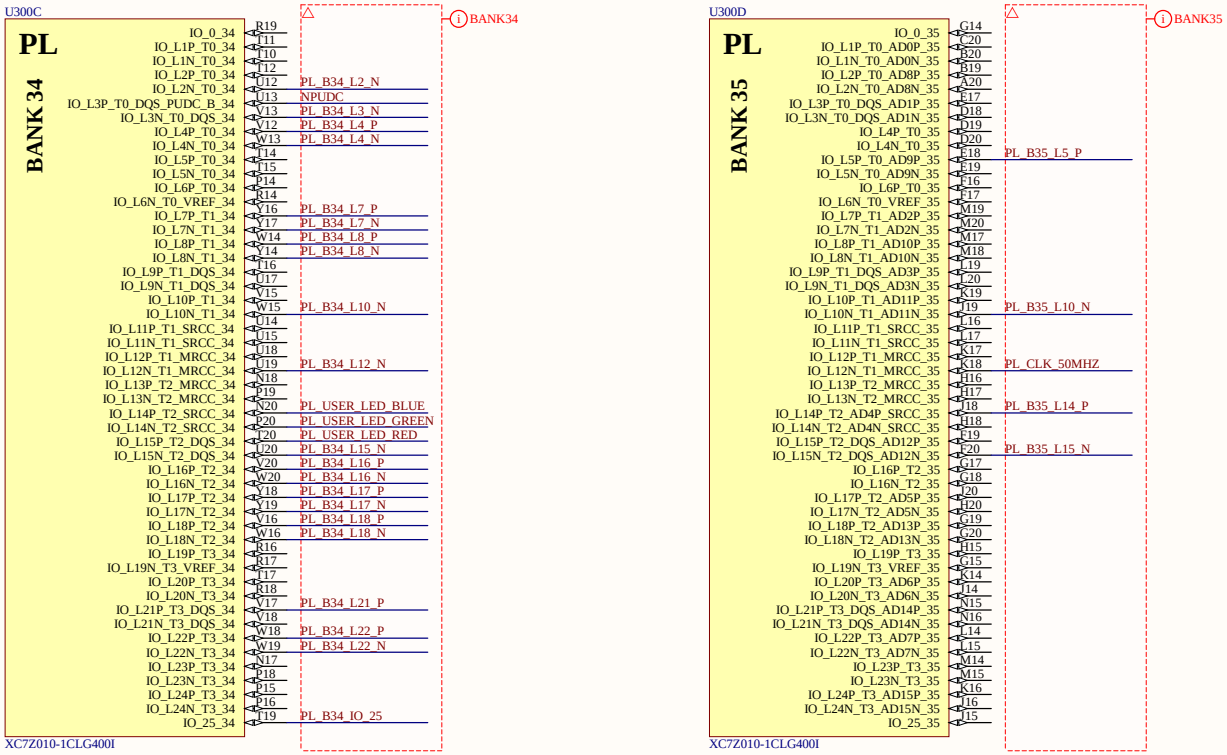
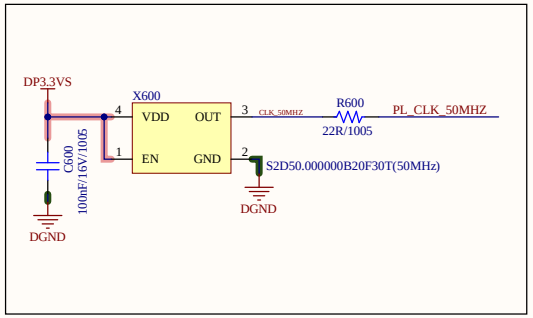
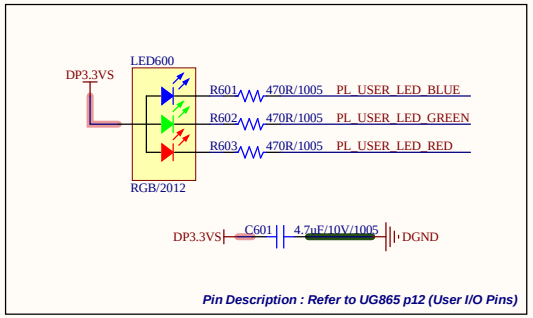
[6] ZYNQ Programmable Logic (PL)



PL Clock (50MHz)



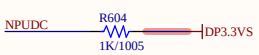
PL Status LED



Pin Description : Refer to UG865 p12 (User I/O Pins)

PL PUDC Config

"PUDC_B" is for Pull-UP During Configuration (bar)
if "PUDC_B" is Low, Internal pull-up resistors are enabled
else if "PUDC_B" is High, Internal pull-up resistors are disabled



Pin Description : Refer to UG865 p13 (PUDC_B)

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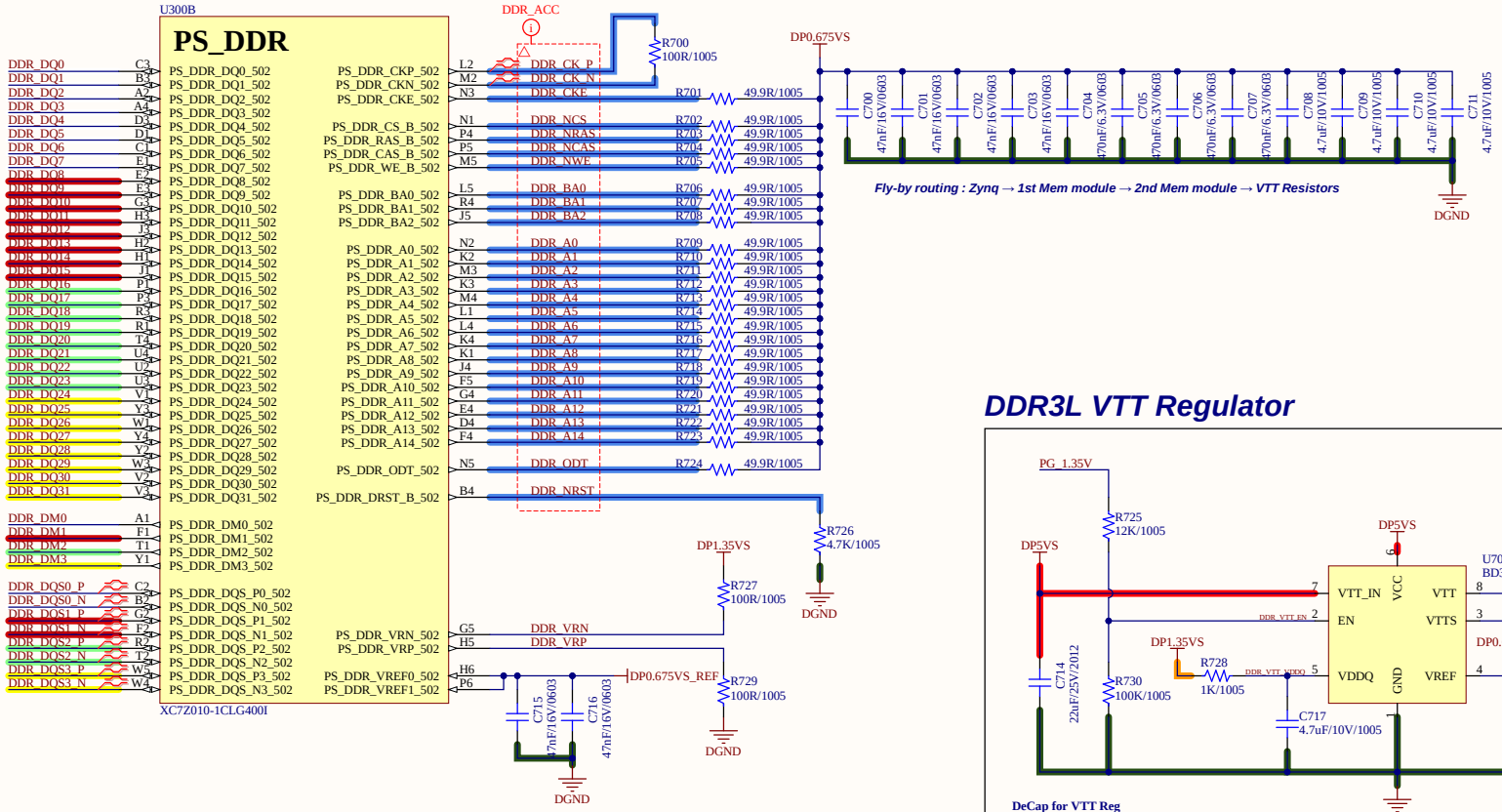
[7] ZYNQ DDR Interface



DDR3L VTT Regulator

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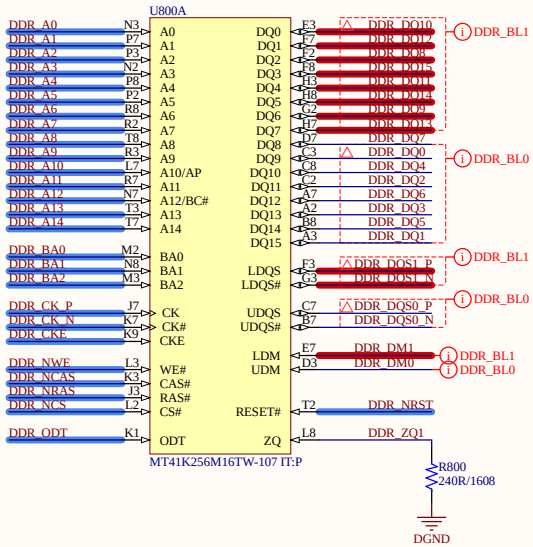
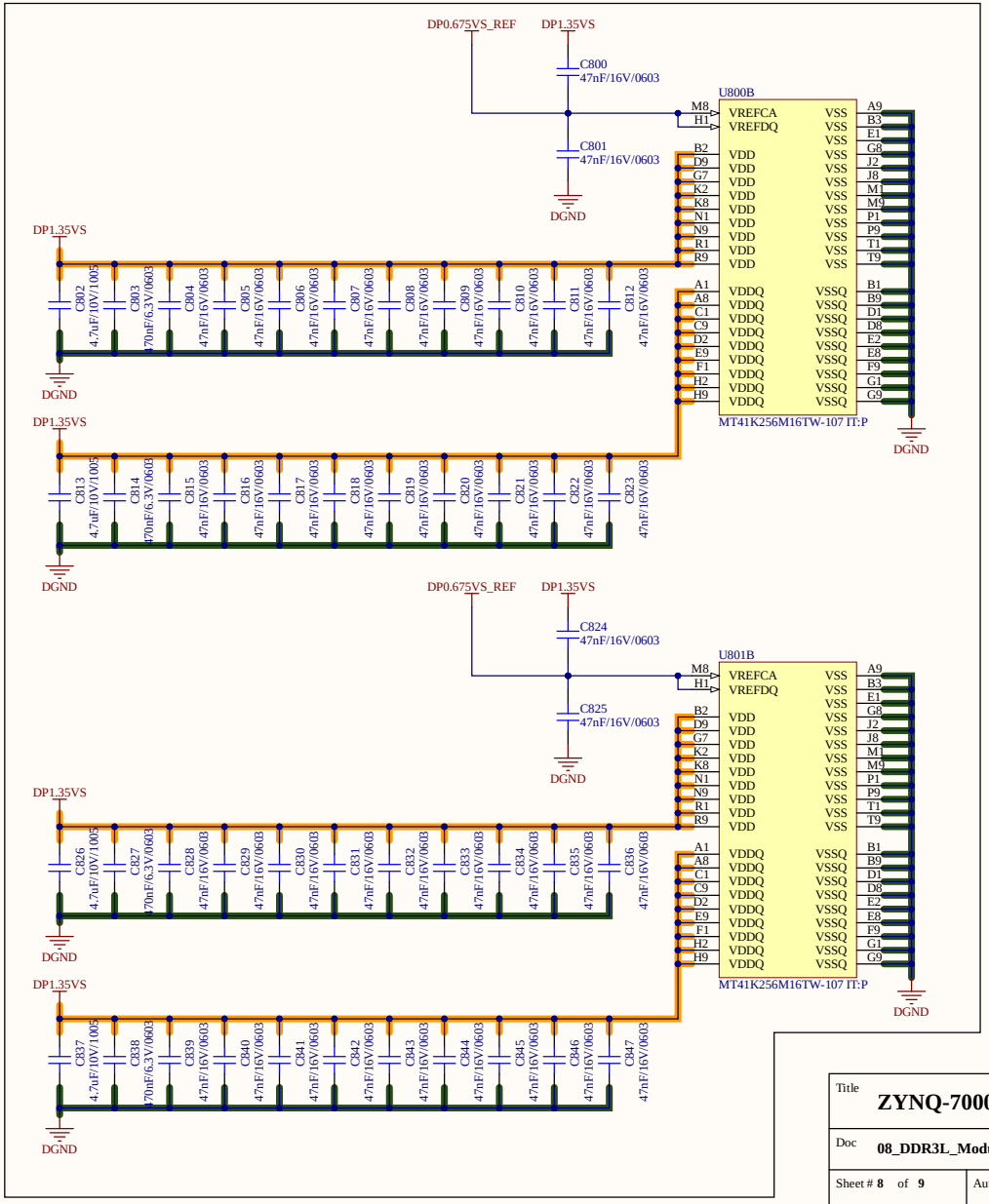
[8] DDR3L Memory Modules

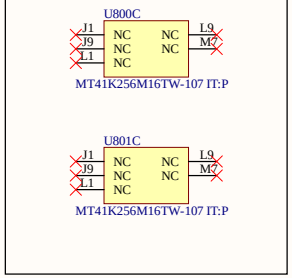
ACC & DATA Connections



DDR Power & Decoupling



Unused Pins



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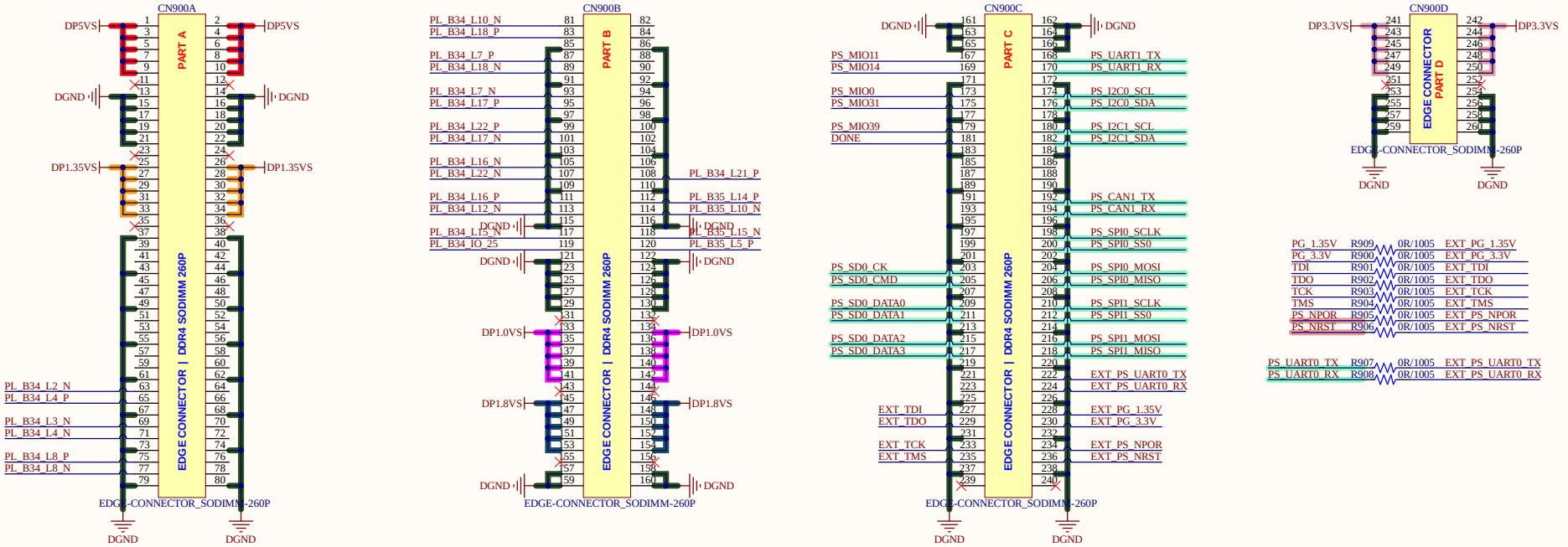
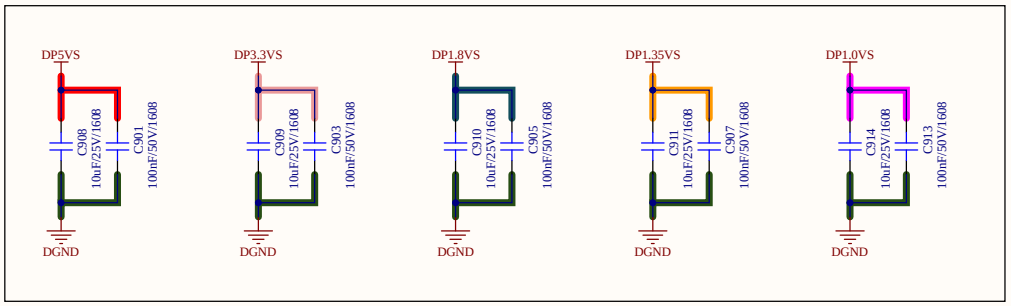
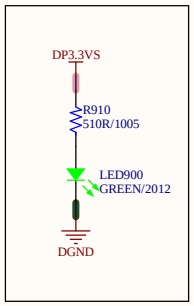
[9] Connectors



Decoupling Capacitors



Power LED



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