

XC7Z010 Test B'd (Rev.A)

[1] Index

Rev	Date	Designer	Description
A	24.02.20	Ganghyeok Lim	Create design project
B			
C			
D			

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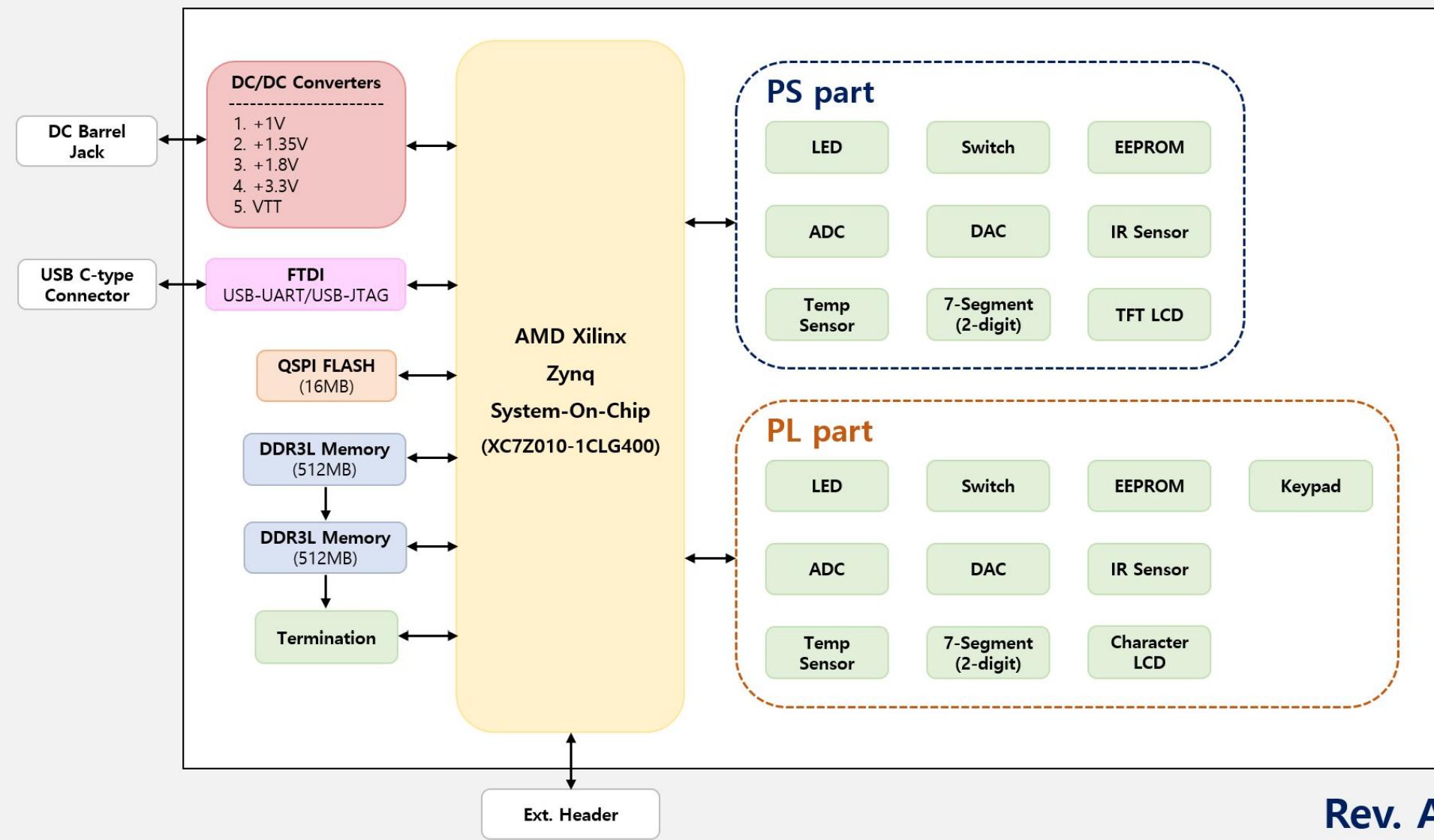
- #1 Index
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[2] Overview

XC7Z010 Test B'd (Rev.A)



Rev. A

XC7Z010 Test B'd (Rev.A)

[3] Power Budget

A

A

B

B

C

C

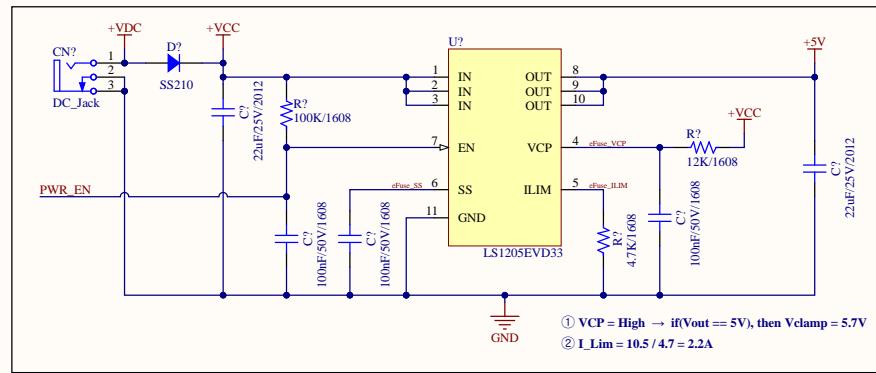
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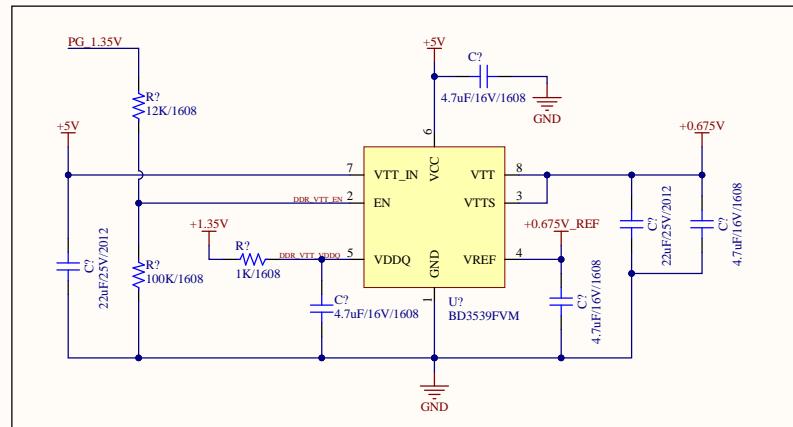
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[4] Power

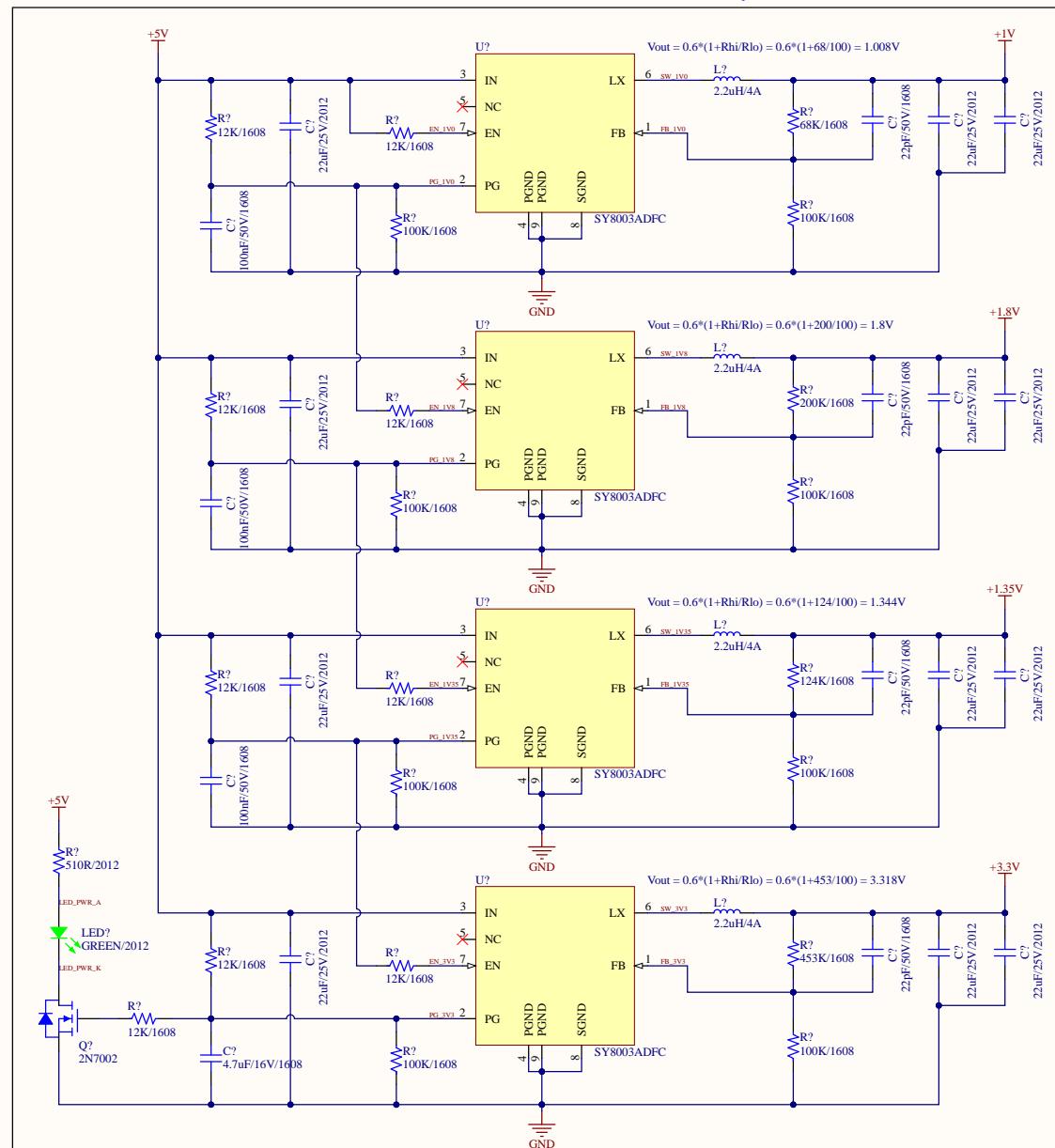
Input Power & eFuse



DDR3L VTT Regulator



Buck Converters



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XC7Z010 Test Bd (Rev.A)

[5] Zynq Power & Decoupling

Main Supplies (INT, AUX, DDR, MIO)

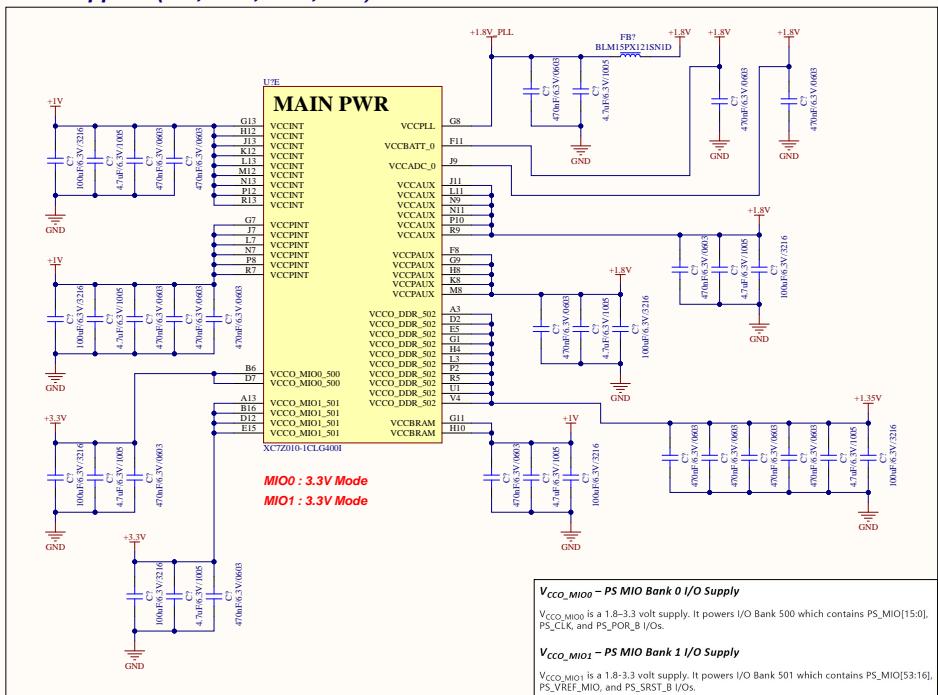


Table 3-2: Required PCB Capacitor Quantities per Device (PS)

Package	Device	V _{CCPINT}			V _{CCPAUX} ^[1]			V _{CCO_DBR}			V _{CCO_MIO0}			V _{CCO_MIO1}			V _{CCPU} ^{[2][3]}		
		100 μF	100 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF
CLG225	Z-70075	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1
CLG400	Z-70075	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1
CLG225	Z-7010	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1
CLG400	Z-7010	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1
CLG485	Z-70125	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1
CLG400	Z-70145	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1
CLG484	Z-70145	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1
CLG485	Z-7015	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1
CLG400	Z-7020	1	1	3	1	1	1	1	1	1	4	1	1	1	1	1	1	1	1

V_{CCO_MIO0} – PS MIO Bank 0 I/O Supply

V_{CCO_MIO0} is a 1.8-3.3 volt supply. It powers I/O Bank 500 which contains PS_MIO[15:0], PS_CLK, and PS POR_B I/Os.

V_{CCO_MIO1} – PS MIO Bank 1 I/O Supply

V_{CCO_MIO1} is a 1.8-3.3 volt supply. It powers I/O Bank 501 which contains PS_MIO[53:16], PS_VREF_MIO, and PS_SRST_B I/Os.

V_{CCPINT} – PS Internal Logic Supply

V_{CCPINT} is a 1.0 nominal supply that powers all of the PS internal logic circuits. This supply can be combined with V_{CCMIO} if the system does not require the PL supply to be powered down independent of the PS.

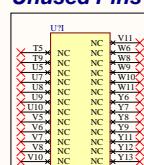
V_{CCPAUX} – PS Auxiliary Logic Supply

V_{CCPAUX} is a 1.8 nominal supply that powers all of the PS auxiliary logic circuits. One of the 0.47 μF capacitors must have less than a 200 mil (5.1 mm) total PCB trace length from the capacitor to the adjacent V_{CCPAUX} and GND BGA pins. This supply can be combined with V_{CCMIO} if the system does not require the PL supply to be powered down independent of the PS.

Table 3-1: Required PCB Capacitor Quantities per Device (PL)

Package	Device	V _{CCINT}			V _{CCBRAM}			V _{CCAux}			V _{CCAO_Io}			V _{CCO_per Bank} ^{[3][4]}			Bank 0			
		680 μF	330 μF	100 μF	4.7 μF	0.47 μF	100 μF	47 μF	4.7 μF	0.47 μF	47 μF	4.7 μF	0.47 μF	47 μF	4.7 μF	0.47 μF				
CLG225	Z-70075	0	0	1	1	2	NA	NA	NA	NA	1	1	1	NA	NA	NA	1	2	4	
CLG400	Z-70075	0	0	1	1	2	0	1	1	1	1	1	1	NA	NA	NA	1	2	4	
CLG225	Z-7010	0	0	1	1	2	NA	NA	NA	NA	1	1	1	NA	NA	NA	1	2	4	
CLG400	Z-7010	0	0	1	1	2	0	1	1	1	1	1	1	NA	NA	NA	1	2	4	
CLG485	Z-70125	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	
CLG400	Z-70145	0	1	0	2	4	1	0	1	1	1	1	1	2	NA	NA	NA	1	2	4
CLG484	Z-70145	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	
CLG485	Z-7015	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	
CLG400	Z-7020	0	1	0	2	4	1	0	1	1	1	1	1	NA	NA	NA	1	2	4	
CLG484	Z-7020	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	

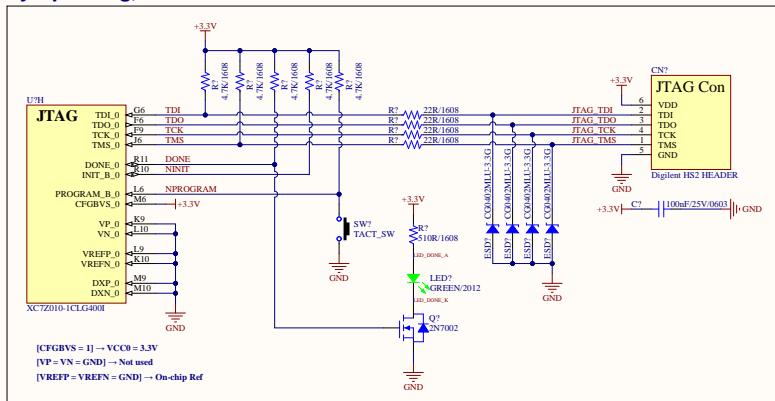
Unused Pins



XC7Z010 Test Bd (Rev.A)

[6] Zynq Config, JTAG, Debug

Zynq Config, JTAG



Boot Mode MIO Strapping Pins (UG585 p167)

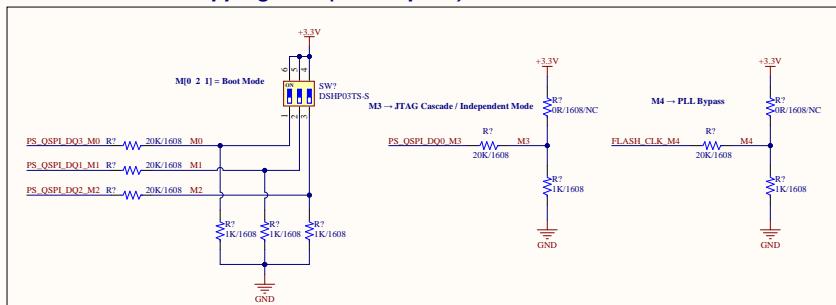


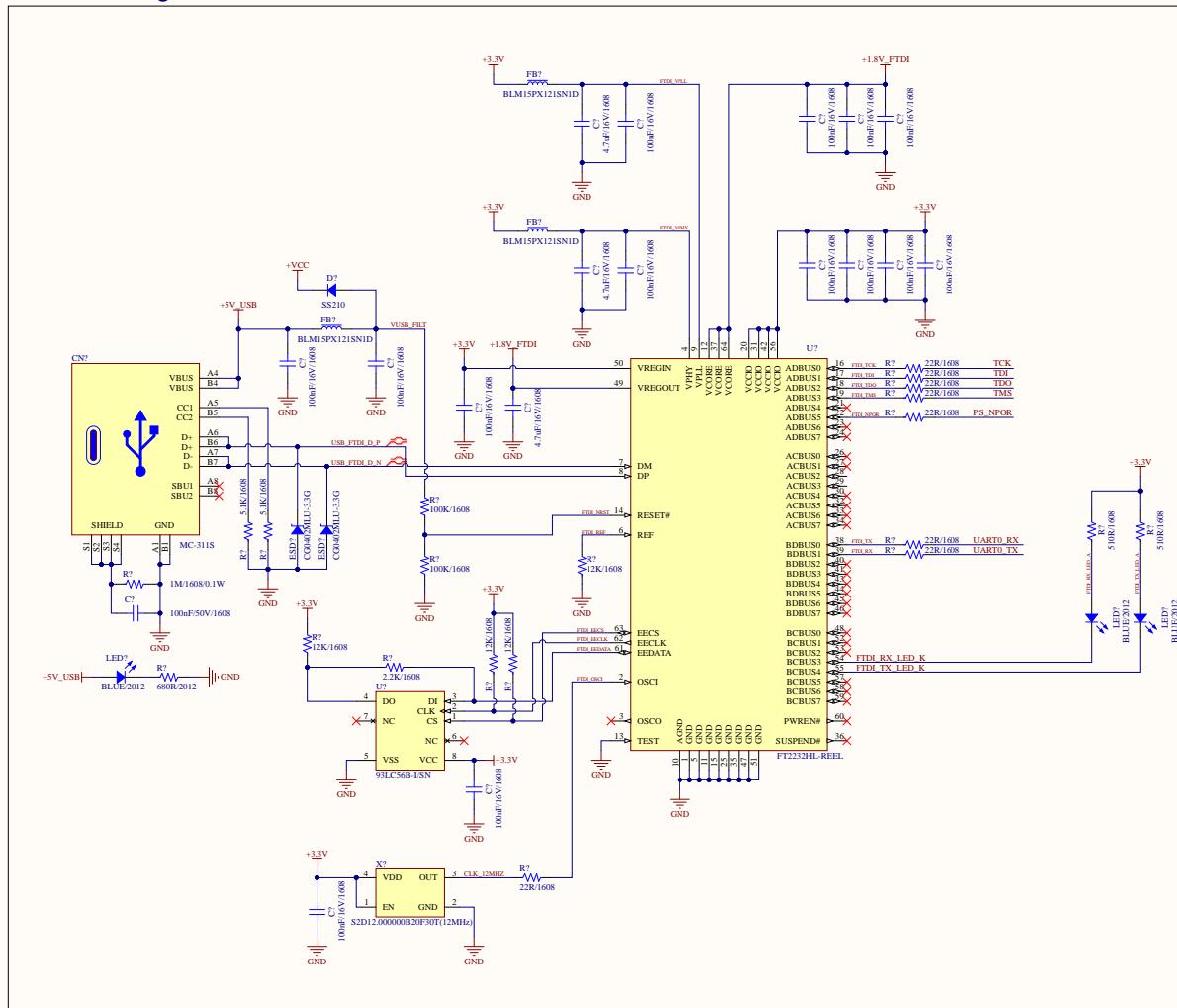
Table 6-4: Boot Mode MIO Strapping Pins

Pin-Signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]	
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[3]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[0]	
Boot Devices								
JTAG Boot Mode; cascaded is most common ^[1]	0	0	0					
NOR Boot ^[3]	0	0	1					
NAND	0	1	0					
Quad-SPI ^[3]	1	0	0					
SD Card	1	1	0					
Mode for all 3 PLLs								
PLL Enabled		0	Hardware waits for PLL to lock, then executes BootROM.					
PLL Bypassed		1	Allows for a wide PS_CLK frequency range.					
MIO Bank Voltage^[4]								
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.					
2.5 V, 3.3 V	0	0						
1.8 V	1	1						

Notes:

- JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
- In secure mode, JTAG is not enabled and MIO[2] is ignored.
- The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure).
- Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

FTDI JTAG Programmer and USB-to-UART



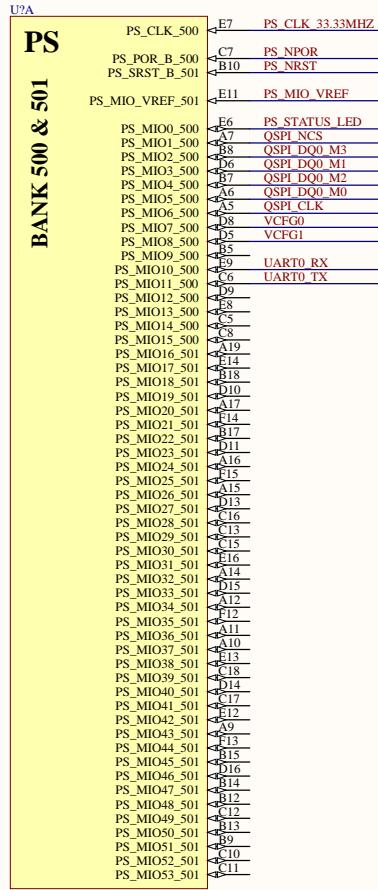
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Doc	05_Zynq_Config.SchDor		
Sheet #	6 of 11	Author	*
Date	2024-03-02		

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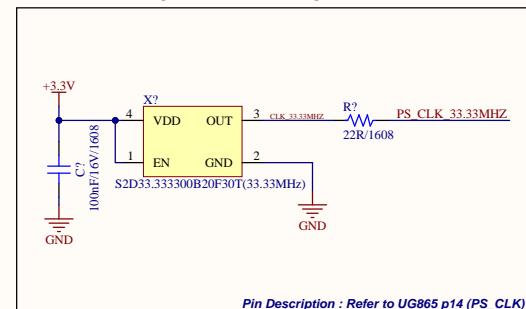
XC7Z010 Test Bd (Rev.A)

[7] Zynq Processing System (PS)

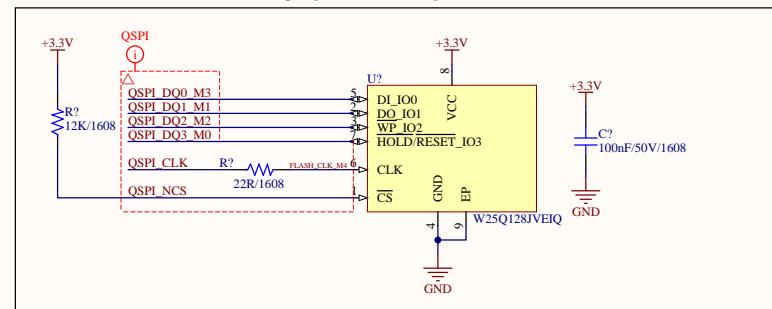
ZYNQ PS (BANK 500 / 501)



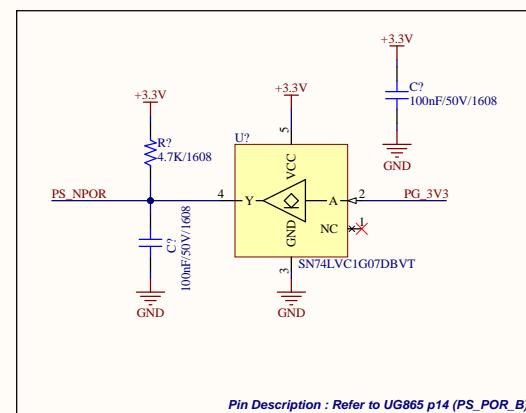
PS Clock (33.33 MHz)



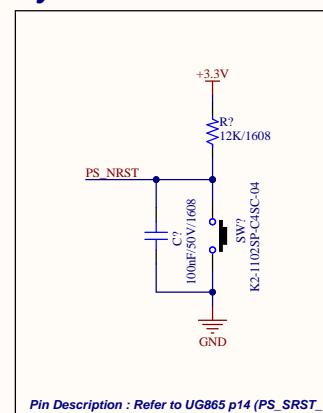
QSPI Flash Memory (128Mbit)



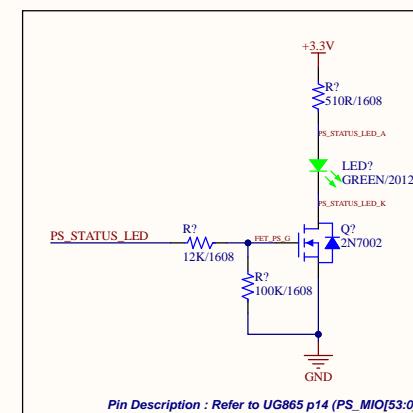
Power on Reset



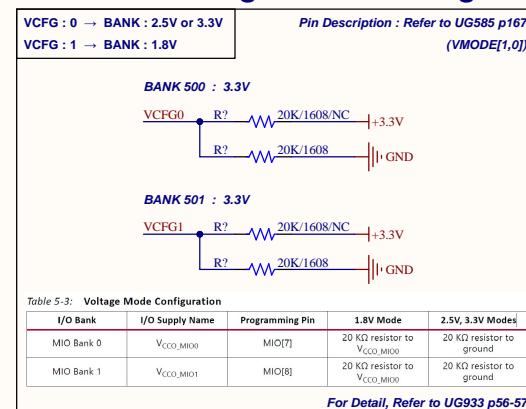
System Reset Switch



PS Status LED



MIO Bank Voltage Mode Config



PS_MIO_VREF Config



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Reference

[1] Processing System (PS) Power and Signaling

Zynq-7000 SoC's Power domain Overview

Power

Zynq-7000 SoC devices are divided into several power domains. Figure 5-1 shows an overview of those domains.

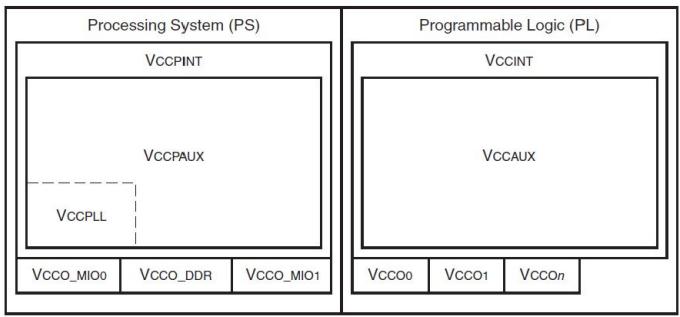


Figure 5-1: Power Domains

Required PCB Capacitor Quantities

Table 3-2: Required PCB Capacitor Quantities per Device (PS)

Package	Device	V _{CCPINT}			V _{CCPAUX} ⁽¹⁾			V _{CCO_DDR}			V _{CCO_MIO0}			V _{CCO_MIO1}			V _{CCPLL} ⁽²⁾⁽³⁾		
		100 μ F	4.7 μ F	0.47 μ F	100 μ F	4.7 μ F	0.47 μ F	100 μ F	4.7 μ F	0.47 μ F	100 μ F	4.7 μ F	0.47 μ F	100 μ F	4.7 μ F	0.47 μ F	100 μ F	4.7 μ F	0.47 μ F
CLG225	Z-7007S	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1
CLG400	Z-7007S	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1
CLG225	Z-7010	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1
CLG400	Z-7010	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1
CLG485	Z-7012S	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1
CLG400	Z-7014S	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1
CLG484	Z-7014S	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1
CLG485	Z-7015	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1
CLG400	Z-7020	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1	1

Table 3-1: Required PCB Capacitor Quantities per Device (PL)

Package	Device	V _{CCINT}				V _{CCBRAM}				V _{CCAUX}				V _{CCAUX_IO}				V _{CCO} Per Bank ⁽³⁾⁽⁴⁾				Bank 0	
		680 μ F	330 μ F	100 μ F	4.7 μ F	0.47 μ F	100 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F or 100 μ F	4.7 μ F	0.47 μ F	47 μ F	Bank 0		
CLG225	Z-7007S	0	0	1	1	2	NA	NA	NA	NA	1	1	1	NA	NA	NA	1	2	4	1			
CLG400	Z-7007S	0	0	1	1	2	0	1	1	1	1	1	1	NA	NA	NA	1	2	4	1			
CLG225	Z-7010	0	0	1	1	2	NA	NA	NA	NA	1	1	1	NA	NA	NA	1	2	4	1			
CLG400	Z-7010	0	0	1	1	2	0	1	1	1	1	1	1	NA	NA	NA	1	2	4	1			
CLG485	Z-7012S	0	1	0	2	4	1	0	1	1	1	2	NA	NA	NA	1	2	4	1				
CLG400	Z-7014S	0	1	0	2	4	1	0	1	1	1	1	1	NA	NA	NA	1	2	4	1			
CLG484	Z-7014S	0	1	0	2	4	1	0	1	1	1	2	NA	NA	NA	1	2	4	1				
CLG485	Z-7015	0	1	0	2	4	1	0	1	1	1	2	NA	NA	NA	1	2	4	1				
CLG400	Z-7020	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	1			
CLG484	Z-7020	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	1			

Main Power Supplies

V_{CCPINT} – PS Internal Logic Supply

V_{CCPINT} is a 1.0V nominal supply that powers all of the PS internal logic circuits. This supply can be combined with V_{CCINT} if the system does not require the PL supply to be powered down independent of the PS.

V_{CCPAUX} – PS Auxiliary Logic Supply

V_{CCPAUX} is a 1.8V nominal supply that powers all of the PS auxiliary circuits. One of the 0.47 μ F capacitors must have less than a 200 mil (5.1 mm) total PCB trace length from the capacitor to the adjacent V_{CCPAUX} and GND BGA vias. This supply can be combined with V_{CCAUX} if the system does not require the PL supply to be powered down independent of the PS.

V_{CCPLL} – PS PLL Supply

V_{CCPLL} is a 1.8V nominal supply that provides power to the three PS PLLs and additional analog circuitry. It can be powered separately or derived from the V_{CCPAUX} supply. If powered by V_{CCPAUX}, V_{CCPLL} must be filtered through a 120 Ω @ 100 MHz, size 0603 ferrite bead and a 10 μ F or larger, size 0603 decoupling capacitor. In both cases a 0.47 μ F to 4.7 μ F 0402 capacitor must be placed near the V_{CCPLL} BGA via.

The PCB construction of the V_{CCPLL} power supply must be carefully managed. The recommended connection between the 10 μ F 0603 capacitor and the V_{CCPLL} BGA ball is a planelet with a minimum width of 80 mil (2 mm) and a length of less than 3,000 mil (76 mm). If a planelet cannot be used then a trace with a maximum impedance of 40 Ω and a length of less than 2,000 mil (50.8mm) must be used. The 0.47 μ F to 4.7 μ F 0402 or 0201 capacitor must have a less than a 200 mil (5.1 mm) total PCB trace length from the capacitor to the adjacent V_{CCPLL} and GND BGA vias.

Figure 5-2 shows an example of the filtering and local capacitor circuit used when V_{CCPLL} is derived from V_{CCPAUX}. Figure 5-3 shows an example of the layout of the same filtering circuit for the CLG484 package.

The recommended components are:

- Ferrite bead – Murata BLM18SG121TN1
- 10 μ F capacitor – Murata GRM188R60G106ME47
- 0.47 μ F-4.7 μ F capacitor – Murata GRM155R60J474KE19

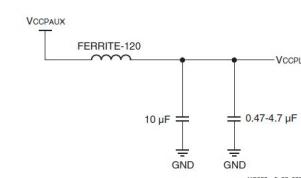


Figure 5-2: Connecting V_{CCPLL}

PS DDR Power Supplies

V_{CCO_DDR} – PS DDR I/O Supply

V_{CCO_DDR} is a 1.2V–1.8V nominal supply that supplies the DDR I/O bank input and output drivers. This supply sources the DDR output drivers, input receivers and termination circuitry. Its requirements are defined by the type of interface (DDR2, DDR3/3L or LPDDR2), memory speed, and the data bus width. Table 5-1 shows the supply voltages for the different memory types.

Table 5-1: PS DDR Interface I/O Supply

DDR Interface	DDR2	DDR3/3L	LPDDR2
Voltage	1.8V	1.5V/1.35V	1.2V

PS_DDR_VREF0, PS_DDR_VREF1 – PS DDR Reference Voltage

PS_{_}DDR_{_}VREF0 and PS_{_}DDR_{_}VREF1 provide a voltage reference for the PS_{_}DDR_{_}DQ and PS_{_}DDR_{_}DQS input receivers. They need to be tied to a termination voltage (V_{tr}) equal to V_{CCO_DDR}/2. For example, for DDR3, V_{CCO_DDR} is set to 1.5V, then V_{REF} shall be set to 0.75V. A resistor divider can be used to generate PS_{_}DDR_{_}VREF0 and PS_{_}DDR_{_}VREF1. A 0.01 μ F – 0.47 μ F capacitor shall be added for decoupling. The PS DDR reference voltage can also be generated internally. For LPDDR2, PS_{_}DDR_{_}VREF0/1 shall be set to VDDQ/2 in accordance with the HSUL_12 I/O standard. See section 2.5.7 (MIO Pin Electrical Parameters) in [UG585, Zynq-7000 SoC Technical Reference Manual](#).

Note: PS_{_}DDR_{_}VREF0/1 should be left floating when DDR is not used or if the internal V_{REF} is in use.

PS_{_}DDR_{_}VRN, PS_{_}DDR_{_}VRP – PS DDR Termination Voltage

PS_{_}DDR_{_}VRN and PS_{_}DDR_{_}VRP provide a reference for digitally controlled impedance (DCI) calibration. For memory types that require termination (DDR2, DDR3) VRP must be pulled Low to GND and VRN needs to be pulled High to V_{CCO_DDR}. For DDR3/3L, the resistor value on VRP and VRN should be twice the memory's trace and termination impedance. For example, for a DDR3 memory with a 400 termination and board impedance, an 80 Ω resistor must be used to pull-up/down VRP and VRN. For LPDDR2, the DCI tones the output impedance of the driver and therefore the resistor value on VRP and VRN should be equal to the transmission line impedance, typically set to 40 Ω .

Table 5-2: DCI VRN and VRP Values

	LPDDR2	DDR2	DDR3/3L
VRP/VRN	40 Ω	100 Ω	80 Ω
(type I DCI trace impedance 40 Ω)	(type III DCI trace impedance 50 Ω)	(type III DCI trace impedance 40 Ω)	(type III DCI trace impedance 40 Ω)

Unused DDR Memory

When no PS DDR memory is used, V_{CCO_DDR} should be tied to V_{CCPAUX}. PS_{_}DDR_{_}VREF0/1 and PS_{_}DDR_{_}VRN/P should be left floating.

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Reference

[1] Processing System (PS) Power and Signaling

DDR Interface Pins

Dynamic Memory

Zynq-7000 SoC devices support DDR2, DDR3/3L, and LPDDR2 (mobile DDR) dynamic memory. The memory is connected to dedicated pins in I/O Bank 502. This bank has dedicated I/O, termination, and reference voltage supplies.

DDR runs at very high speeds and special care need to be taken in board layout to ensure signal integrity. The following sections show the recommendations for DDR memory designs for Zynq-7000 SoC devices.

DDR Interface Signal Pins

Table 5-4 lists all dynamic memory interface signals in Bank 502.

Table 5-4: DDR Interface Signal Pins

Pin Name	Direction	Description
DDR_CK_P	O	Differential clock output positive
DDR_CK_N	O	Differential clock output negative
DDR_CKE	O	Clock enable
DDR_CS_B	O	Clock select
DDR_RAS_B	O	RAS row address select
DDR_CAS_B	O	CAS column address select
DDR_WE_B	O	Write enable
DDR_BA[2:0]	O	Bank address
DDR_A[14:0]	O	Address
DDR_ODT	O	Output dynamic termination
DDR_DRST_B	O	Reset

Table 5-4: DDR Interface Signal Pins (Cont'd)

Pin Name	Direction	Description
DDR_DQ[31:0]	I/O	Data
DDR_DM[3:0]	O	Data mask
DDR_DQS_P[3:0]	I/O	Differential data strobe positive
DDR_DQS_N[3:0]	I/O	Differential data strobe negative
DDR_VRP	I/O	Used to calibrate input termination
DDR_VRN	I/O	Used to calibrate input termination
DDR_VREF[1:0]	I/O	Reference voltage

Unused DDR pins should be connected as shown in Table 5-5.

Note: For PS_DDR_DQxx, ensure that byte lines are kept together. PS_DDR_ADDR0 should always be used. If bits must be omitted for chip select or other functionality, omit upper bit (PS_ADDR14) instead.

For designs utilizing single-ended DQS, connect the DQS signal to DQS_P. DQS_N can either be connected to the DQS_B I/O of the SDRAM, or via resistor divider to VCCO/2.

Table 5-5: DDR Unused Pins

Unconnected Pins	Comments
DDR Unused Pins, x16 non-ECC	
O	Unconnected
DQ/DQS IO	Unconnected, internal pull-up by software
IO	Unconnected, internal pull-up by software
DDR Unused Pins, x16 ECC	
O	Unconnected
DQ/DQS IO	Connect to SDRAM
Other IO	Unconnected, internal pull-up by software

DDR Memory Implementation

Figure 5-5, Figure 5-6 and Figure 5-7 show examples of implementing DDR memory on typical boards.

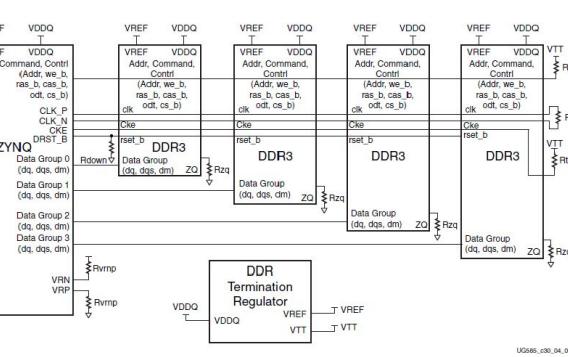


Figure 5-5: DDR3/3L Board Implementation

DDR Supply Voltages

DDR Supply Voltages

Table 5-6 lists the different supply, reference and termination voltages required for LPDDR2/DDR2/DDR3 memory. These voltages are also required to power the DDR I/O bank, reference, and termination voltages.

Note: V_{REF} should track the midpoint of the VDD supplied to the DRAM and ground via low-impedance paths. This can be done with a resistive divider or by a regulator that tracks this midpoint. If resistive dividers are used, a separate divider and high-frequency decoupling capacitor is recommended for each IC. If a regulator is used, a low impedance plane or planelet is recommended for distribution.

Table 5-6: DDR Voltage

Voltage	LPDDR2	DDR2	DDR3	DDR3L	Comments
V _{CCO_DDR} V _{DDQ}	1.2V	1.8V	1.5V	1.35V	LPDDR2 devices also require V _{DD1} (1.8V) and V _{DD2} (1.2V)

Table 5-6: DDR Voltage (Cont'd)

Voltage	LPDDR2	DDR2	DDR3	DDR3L	Comments
V _{TT}	V _{DDQ} /2	V _{DDQ} /2	V _{DDQ} /2	V _{DDQ} /2	
PS_DDR_VREF0 PD_DDR_VREF1	V _{DDQ} /2	V _{DDQ} /2	V _{DDQ} /2	V _{DDQ} /2	Use a DDR termination regulator or a resistor voltage divider to generate V _{TT} and V _{REF}
V _{REF}					

DDR Termination

DDR Termination

For better signal integrity, DDR2 and DDR3 clock, address, command and control signals need to be terminated. For DDR2, ODT and CKE are not terminated and should be pulled down during memory initialization with a 4.7 kΩ resistor to GND. For DDR3, the DRST_B signal is not terminated and should be pulled down during memory initialization with a 4.7 kΩ resistor to GND.

LPDDR2 does not require termination.

Table 5-7 shows the DDR termination requirements.

Table 5-7: DDR Termination

Termination	LPDDR2	DDR2	DDR3/3L	Comments
Rterm	N/A	50Ω	40Ω	
Rclk	N/A	100Ω	80Ω	
Rdown	4.7 kΩ	4.7 kΩ	4.7 kΩ	There is no DDR_DRST_B in LPDDR2/DDR2 device side

Note: DDR3 memory also supports terminated DQS signals through the TDOQS_P and TDQS_N pins. This feature is not supported on Zynq-7000 SoC devices and those pins should be left floating.

DDR Trace Length

DDR Trace Length

All DDR memory devices should be placed as closely to the Zynq-7000 SoC device as possible. Table 5-8 shows the maximum recommended trace lengths for DDR signals.

Table 5-8: DDR Max Trace Length

Signal Group	LPDDR2	DDR2	DDR3/3L
Data Group	1.5"	8.55"	8.55"
Address, Command, Control	1.5"	8.55"	8.55"

In addition, DDR signals also require matched trace delays, which include package delays. Table 5-9 shows the recommended delay matching for DDR. Differential traces should be delay matched such that the signal crossing point occurs in the linear region of the rising and falling edges.

The skew limits can be increased if the memory interface is not operated at the maximum frequency, and/or if a faster memory device is utilized. See Appendix A, Processing System Memory Derating Tables for derating tables for DDR3, DDR3L, and LPDDR2.

Table 5-9: DDR Delay Match

Signal Group	LPDDR2	DDR2	DDR3/3L
DQ/DM to DQS_P/N in data group	±10 ps	±20 ps	±10 ps
Address/Control to CK_P/N	±10 ps	±25 ps	±10 ps

Route the CK traces to be equal to or longer than the DQS traces per byte lane. This is necessary because:

- The write leveling is capable of adjusting the clock to write DQS alignment over a wide range, assuming the clock trace length is longer than the DQS traces.
- The read leveling is capable of adjusting the read data eye to read DQS over a wide range. The adjustment is per byte, so board skew between bits (DQ, DM) should be minimized, as indicated in Table 5-9.
- There is no automatic training for aligning command/address to clock, but a fixed offset is programmable and can be used if necessary. Skew between CK and address/control should be minimized, as indicated in Table 5-9.

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Reference

[1] Processing System (PS) Power and Signaling

PS MIO Power Supplies

V_{CCO_MIO0} – PS MIO Bank 0 I/O Supply

V_{CCO_MIO0} is a 1.8–3.3 volt supply. It powers I/O Bank 500 which contains PS_MIO[15:0], PS_CLK, and PS_POR_B I/Os.

V_{CCO_MIO1} – PS MIO Bank 1 I/O Supply

V_{CCO_MIO1} is a 1.8–3.3 volt supply. It powers I/O Bank 501 which contains PS_MIO[53:16], PS_VREF_MIO, and PS_SRST_B I/Os.

Configuring the V_{CCO_MIO0} , V_{CCO_MIO1} Voltage Mode

The PS I/O banks can operate in two different voltage modes, low (1.8V) mode and high (2.5V – 3.3V) mode. Before powering on, the banks must be configured for the correct mode otherwise, damage might occur. The I/O bank voltage is set by pulling pins MIO[7] and MIO[8] either High or Low. Table 5-3 shows the voltage mode configuration (VMODE) for MIO Bank 0 and Bank 1.

MIO[7] and MIO[8] are dual use pins that are shared with the high-speed QSPI/NAND/SRAM interface signals. Special care needs to be taken to avoid signal integrity issues.

Table 5-3: Voltage Mode Configuration

I/O Bank	I/O Supply Name	Programming Pin	1.8V Mode	2.5V, 3.3V Modes
MIO Bank 0	V_{CCO_MIO0}	MIO[7]	20 kΩ resistor to V_{CCO_MIO0}	20 kΩ resistor to ground
MIO Bank 1	V_{CCO_MIO1}	MIO[8]	20 kΩ resistor to V_{CCO_MIO1}	20 kΩ resistor to ground

CAUTION! If the MIO bank voltage is incorrectly set, the I/O behaves unpredictably and damage might occur. For example, avoid setting the MIO voltage to 3.3V while using HSTL18. Any pull-up resistors should only connect to V_{CCO_MIO0} . An exception to this requirement are temporary Boundary Scan EXTEST operations which require 1.8V MIO banks to use a 2.5/3.3V VMODE setting for correct EXTEST operation.

PS_MIO_VREF – RGMII Reference Voltage

PS_MIO_VREF provides a reference voltage for the RGMII input receivers. If RGMII is being used, this pin should be tied to a voltage equal to one half V_{CCO_MIO1} . For example, when using a HSTL18 RGMII interface, V_{CCO_MIO1} is set to 1.8V then PS_MIO_VREF shall be set to 0.9V. A resistor divider can be used to generate PS_MIO_REF. A 0.01 μF capacitor shall be added for decoupling. If RGMII is not being used, PS_MIO_VREF is safe to float.

PS Clock & Reset

PS_CLK – Processor Clock

PS_CLK shall be connected to a clock generator providing a 30–60 MHz clock. The clock must be a single-ended LVCMOS signal, using the same voltage level as the V_{CCO_MIO0} I/O voltage for bank MIO0. Refer to [DS187](#), Zynq-7000 SoC (Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015, and Z-7020); DC and AC Switching Characteristics and [DS191](#), Zynq-7000 SoC (Z-7030, Z-7035, Z-7045, and Z-7100); DC and AC Switching Characteristics for further PS_CLK requirements.

PS_POR_B – Power on Reset

IMPORTANT: The PS_POR_B input is required to be asserted to GND during the power-on sequence until V_{CCPINT} , V_{CCPAUX} and V_{CCO_MIO0} have reached minimum operating levels. Before V_{CCPINT} reaches 0.80V at least one of the four following conditions is required during the power-off stage: the PS_POR_B input is asserted to GND, the reference clock to the PS_CLK input is disabled, V_{CCPAUX} is lower than 0.70V, or V_{CCO_MIO0} is lower than 0.90V. The condition must be held until V_{CCPINT} reaches 0.40V to ensure PS eFUSE integrity.

PS_SRST_B – External System Reset

The PS system reset (PS_SRST_B) is an active-Low signal that is mostly used for debugging proposes. PS_SRST_B must be High to begin the boot process. If PS_SRST_B is not used it can be pulled High to V_{CCO_MIO1} .

Boot Mode Pins

MIO[8:2] is used to configure the boot mode, PLL bypass, and MIO voltage. All designs must include a 20 kΩ pull-up or pull-down resistor on these pins to set the required setting.

MIO[8] is a dual use pin that is shared with the high-speed QSPI/NAND/SRAM interface signals. Special care needs to be taken to avoid signal integrity issues. To avoid signal integrity issues, limit the stub length to the pull-up or pull-down resistor to < 10 mm.

When system design requires the modes to be changeable, it is recommended to not use a resistor tree to set the mode but instead connect one pull-up/down resistor to the mode pin and place a jumper on the other side of the resistor to select between pull-up or pull-down. See [Figure 5-4](#) for an example.

Note: PROGRAM_B, INIT_B, and DONE should not be left floating. Refer to [UG470](#), 7 Series FPGAs Configuration User Guide for more information on how to treat these pins.

Note: The PL system JTAG interface, PL_JTAG, should have its signals TDI, TMS, and TCK pulled-up.

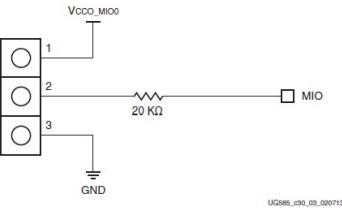


Figure 5-4: Setting Mode Pins

Title	XC7Z010_Test_Bd_(Rev.A).PrjPcb	Rev *
Doc	Ref.01_Zynq_Power_Config_2.SchDoc	
Sheet #	9 of 11	Author *
Date	2024-03-04	
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Reference

[1] Processing System (PS) Power and Signaling

DDR Trace Impedance

DDR Trace Impedance

All DDR signals except DDR_DRST_B require controlled impedance. DDR_CKE also requires controlled impedance in DDR3/3L. [Table 5-10](#) shows the required trace impedance for DDR signals.

[Table 5-10: DDR Trace Impedance](#)

Signal Group	LPDDR2	DDR2	DDR3/3L	Comments
Single-ended	40Ω	50Ω	40Ω	±10% tolerance
Differential	80Ω	100Ω	80Ω	±10% tolerance

DDR3 and LPDDR2 memory also require an additional resistor connected to the ZQ pin to calibrate the device's output impedance. [Table 5-11](#) shows the required RZQ values.

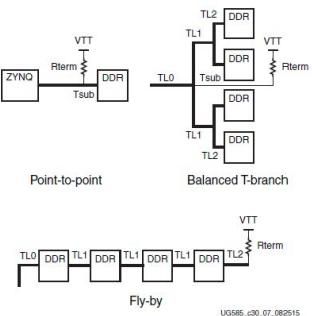
[Table 5-11: DDR ZQ](#)

ZQ	LPDDR2	DDR2	DDR3/3L
Rzq	240Ω	N/A	240Ω

DDR Routing Topology

DDR Routing Topology

Based on the chosen memory type, the number of memory devices and layout requirements, different routing topologies can be used for DDR memory. [Figure 5-8](#) shows three different topologies.



[Figure 5-8: DDR Routing Topologies](#)

In the fly-by topology, TL0 should be 0.0-5.3 inches, with TL1 0.35-0.75 inches, and TL2 0.0-1.0 inches. The total length should be 0.0-8.55 inches.

In a point-to-point configuration the total length should be 0.0-8.55 inches. Rterm should be placed close to the load.

In a balanced T-branch configuration, TL0 should be 0.0-3.0 inches, with trace lengths TL1, TL2, and Tsub kept as short as possible; Rterm should be close to the intersection of TL0 and the TL1 split. All TL1 branches must be the same electrical length and routed on the same layer. Pay attention to crosstalk-induced noise due to serpentine routing. This also applies to all TL2 branches.

RECOMMENDED: Fly-by and point-to-point routing is recommended for optimal memory performance.

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