Lab 2 – Binary Coded Decimal ALU

Introduction

The goal of this lab is to implement a simple BCD ALU in VHDL that augments the binary ALU you have implemented in the previous lab.

- The A and B inputs are both of the same size (N bits). They hold N/4 unsigned BCD digits or (N/4 - 1) signed digits.
- The most significant 4-bits are used for the sign when the value is signed otherwise they are 0000. A negative value is 0001.
- The result for the BCD operations has one additional BCD digit.
- The operations supported are signed/unsigned additions and subtractions.

For example if N = 32 bits. Unsigned values will have 8 digits, signed values will have 7 digits. The results will be 9 and 8 digits respectively.

Deliverables

For this lab you are expected to build an ALU that supports 4 BCD arithmetic operations. The ALU should be designed in such a way that the user can specify the operation's width without modifying the VHDL code. In addition to the ALU you are also expected to build a test-bench that sufficiently verifies it's correctness.

- The entity name should be named "my_alu"
- The entity should use a generic, called "NUMBITS", that specifies the operation's width
- The entity should have input/output ports with the **EXACT** names listed below
- The entity should support the operations listed below
- The carryout port is the MSb's (Most Significant Bit's) carry out.
- The zero port should be '1' when the result port is all zeros.
- The overflow port should be '1' when the available bits are not enough to represent the result. It occurs in the following situations.

Port Name	Size
A	N bit
B	N bit
Opcode	4 bit
Result	N+4 bit
Carry_out	1 bit
Overflow	1 bit
Zero	1 bit

	A	B	Result
signed add	>= 0	>= 0	< 0
	< 0	< 0	>= 0
signed sub	>= 0	< 0	< 0
	< 0	>= 0	>= 0
unsigned add	MSb's carryout is '1'		
unsigned sub	MSb's carryout is '0'		

Turn-In

Each group should turn in one tar file to iLearn. The contents of which should be:

- A README file with the group members names, and any incomplete or incorrect functionality
- A VHDL file with the ALU design
- A VHDL file with the test cases

Operation	Opcode
BCD unsigned add	1000
BCD unsigned subtract	1001
BCD signed add	1100
BCD signed subtract	1101