CS313: Computer Architecture Lab-5

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For this assignment, we have built a discrete event simulator for theprocessor we built so far.

Observations show that the latency caused by various events like MemoryReadEvent, MemoryWriteEvent, MemoryResponseEvent, ExecutionCompleteEvent increased the CPI and thereby decreased the IPC drastically in every benchmark. Whenever a requesting element requests for an event, the processing element stays busy until the event is done. This accounts for the delay.

Results And Observations:

Program	No. of Instructions	NO. of Cycles	Instructions per cycle (IPC)
evenorodd.asm	6	246	0.02439
prime.asm	30	1218	0.02463
fibonacci.asm	86	3464	0.02482
palindrome.asm	56	2274	0.02462
descending.asm	329	13196	0.02493