BASIC LOGIC GATES

**PROGRAM:**

module project\_1(a,b,y,c,d,e,f,g,h):

input a,b;

output y, c, d, e, f, g, h;

and (y, a,b);

or (c, a,b);

not(d, a);

nand (e, a,b);

nor (f, a,b);

xor (g, a,b);

xnor (h, a,b);

endmodule

**RTL SIMULATION:**

