LOGIC GATES USING VECTORS

**PROGRAM:**

module logic\_gates(a,b);

input a,b;

wire y[6:0];

and (y[0],a,b);

or (y[1],a,b);

not(y[2],a);

nand (y[3],a,b);

nor (y[4],a,b);

xor (y[5],a,b);

xnor (y[6],a,b);

endmodule

**WAVEFORMS:**

