HIGH SPEED / DENSITY 2-PORT SRAM
64 WORDS X 8 BITS, MUX 2
SMIC 65nm LL Logic Process

Version 1.7.0

OVERVIEW

The HIGH SPEED / DENSITY 2-PORT SRAM(BW) is designed for SMIC's 65nm CMOS Logic process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.08V to 1.32V and a temperature range of -40°C to 125°C.

The bit-write enable(BWEN[0:n]),chip enable (CENA,CENB), address (AA[0:i],AB[0:i]) and data in (DB[0:n]) signals are latched on the rising-edge of the clock. When CENA is low, the memory is in read-mode. Data is read from the memory location specified on the address bus AA[0:i] and appears on the data output bus QA[n:0].When CENB is low and BWENB[j] is low, the memory is on write-mode. DB[j] is write to the location specified on the address bus AB[i:0]. When CENB is low and BWENB[j] is high, DB[j] can’t be write in.When CENA is high, port A enters the standby mode. Data outputs remained stable.When CENB is high, port B enters the standby mode. Data stored in the memory is retained, but the new data writes is not allowed.

CONFIGURATION:

PARAMETER	VALUE
Mux	2
Words	64
Bits	8
Width	100.74um
Height	58.375um
Area	5880.697um^2

PIN DEFINITION:

PIN	DIRECTION	DEFINITION
AA[5:0]	Input	A Port Address Inputs
AB[5:0]	Input	B Port Address Inputs
DB[7:0]	Input	B Port Data Inputs
BWENB[7:0]	Input	B Port Bit-Write Enable
CENA	Input	A Port Enable
CENB	Input	B Port Enable
CLKA	Input	A Port Clock Input
CLKB	Input	B Port Clock Input
QA[7:0]	Output	Data Outputs

TIMING:

PARAMETER	DESCRIPTION	FF CORNER 1.32V, -40°C		FF CORNER 1.32V, 0°C		FF CORNER 1.32V, 125°C		SS CORNER 1.08V, -40°C		SS CORNER 1.08V, 125°C		TT CORNER 1.2V, 25°C	
(ns)		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Tcyc	Cycle Time	0.306		0.329		0.384		0.823		0.981		0.545	
Ta	Access Time[1]	0.278		0.299		0.349			0.749		0.892		0.495
Tah	Address Hold	0.096		0.095		0.093		0.185		0.101		0.098	
Tas	Address Setup	0.366		0.404		0.415		0.642		0.646		0.420	
Tbwh	Bwen Hold	0.193		0.188		0.193		0.374		0.265		0.211	
Tbws	Bwen Setup	0.308		0.333		0.412		0.538		0.546		0.368	
Tch	Cen Hold	0.041		0.038		0.028		0.027		0.000		0.016	
Tcs	Cen Setup	0.303		0.309		0.323		0.767		0.653		0.404	
Tdh	Data Hold	0.211		0.211		0.211		0.411		0.321		0.242	
Tds	Data Setup	0.289		0.321		0.370		0.781		0.781		0.323	
Tckh	Clock High	0.020		0.020		0.020		0.040		0.040		0.020	
Tckl	Clock Low	0.088		0.088		0.099		0.209		0.231		0.132	
Tckr	Clock Rise Skew	0.500		0.500		0.500		1.000		1.000		0.600	
Tcc	Clock Collision	0.306		0.329		0.384		0.823		0.981		0.545	

Timing simulation conditions:

1. Access time = best case for fast corner and worst case for slow/typical corners

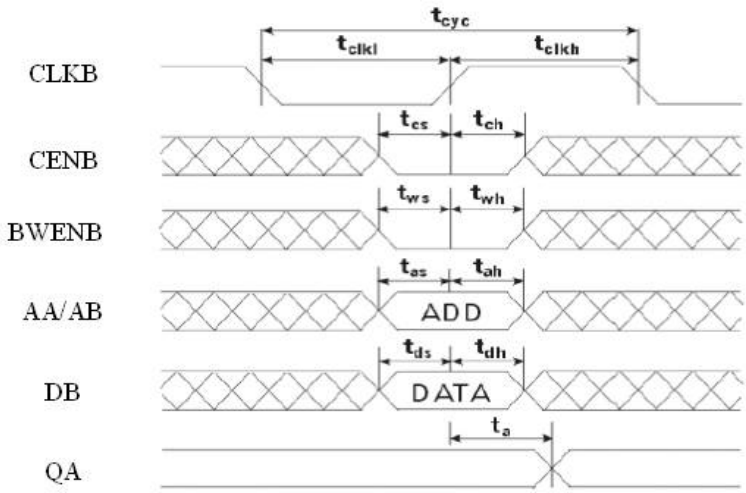
POWER:(UNITS=uA/Mhz)

PARAMETER	FF CORNER 1.32V, -40°C	FF CORNER 1.32V, 0°C	FF CORNER 1.32V, 125°C	SS CORNER 1.08V, -40°C	SS CORNER 1.08V, 125°C	TT CORNER 1.2V, 25°C
AC Current[2]	5.069	4.328	4.374	3.124	3.173	3.622
Read AC Current	5.973	4.449	4.269	3.094	3.074	3.523
Write AC Current	4.166	4.206	4.479	3.155	3.272	3.722
Standby Power (mW)	0.000446	0.000848	0.049571	0.000023	0.002574	0.000282
Deselect Power (mW)[3]	0.045410	0.046489	0.038616	0.026840	0.028040	0.036405

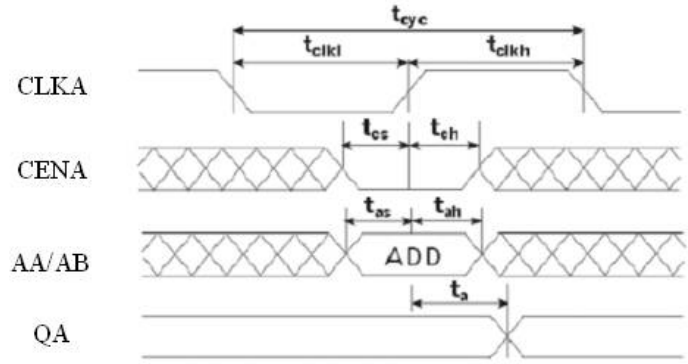
Power simulation conditions:

2. CEN is low, 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz
3. CEN is high, 50% of input pins toggle at 1Mhz

WRITE CYCLE TIMING:



READ CYCLE TIMING:



Datasheet Revision History

Date	Version	Changes
	null	

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