Title: Aging Capacitor Supported Cache Management Scheme for Solid State Drives

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Dissertation:

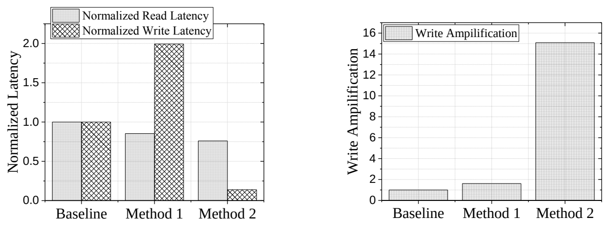
Solid state drives (SSDs) have adopted random access memory (RAM) as cache inside controller to achieve high performance. However, due to the volatility characteristic of RAM, there is a risk of data loss when sudden power supply interruption happens [1]. Capacitor has been suggested as one method by equipping it as interim power supplier to avoid the data loss issue [2][3]. During runtime, SSD's voltage supply is constantly monitored to determine the activation of capacitor. Once current voltage drops to a predefined threshold, the capacitor is activated to write dirty pages back to SSD. However, one of the key issues for the capacitor is the aging problem, which introduces decreased capacitance, especially from the impact of temperature [4]. With capacitor aging, once the remaining capacitance is not able to write all dirty pages back to flash memory, data loss happens.

The straightforward method to avoid the capacitor aging induced data loss is to bound the number of dirty pages in the cache. Two simple methods are able to achieve the bounding requirement based on two different dirty page synchronizing timings: The first method (Method 1) is to synchronize dirty pages back to SSD once the number of dirty pages reaches the capability of the capacitor. In this case, if write miss occurs, dirty pages should be synchronized based on least recently used (LRU) policy to release free space. That is, the missing request will be delayed. The second method (Method 2) is to synchronize dirty pages during idle time of SSDs to avoid the performance impact from above method. Once idle time is detected, dirty pages are synchronized as much as possible to minimize the number of dirty pages reside in the cache. However, in this case, it may introduce immaturely dirty page synchronization, and the lifetime of SSDs can be impacted. Figure 1 presents the normalized access latency and write amplification of abovementioned two methods. From the results, we have following observations: First, Method 1 has smaller write amplification, but introduces a high write access latency. Second, Method 2 has a much better access performance, but induces a high write amplification. In this case, we can find that the timing of synchronizing dirty pages should be carefully selected to improve both performance and lifetime.

In order to solve the above issue, an efficient cache management scheme for capacitor equipped SSDs is proposed. However, there are two challenges for this work: first, the number of dirty pages that the aged capacitor can synchronize back to SSDs, which is called dirty page budget, is unknown to the cache manager; second, the dirty page synchronizing timing is critical on the performance and lifetime of SSDs. As shown in Figure 2, there are two additional modules added in the SSD controller: Dirty Page Budget Detection (DPBD) and Smart Synchronizing Activation (SSA). In the framework, DPBD module is designed to acquire the dirty page budget, which is in charge of connecting power supply switch module and cache management module; SSA module is designed to smartly manage the dirty page synchronization, which connects with cache management module.

For DPBD module, the basic idea is to periodically synchronize the pages in the cache back to SSDs via interim power supplier. The process of the detection module is as follows: during the process of periodically synchronizing pages in the cache back to

SSDs, a page counter is used to record the number of synchronized pages. Once the capacitor is exhausted, the counter is determined as the dirty page budget. For SSA module, the basic idea is to synchronize dirty pages based on the acquired dirty page budget. If the number of dirty pages in the cache is approaching the budget, they should be synchronized as soon as possible. Otherwise, they are delayed to avoid immature synchronization. Based on the proposed scheme, not only the number of dirty pages can be bounded below the dirty page budget, but also the synchronization induced performance and lifetime degradation can be minimized.



(a)Normalized read/write latency. (b) Write amplification.

Figure 1: Normalized read/write latency and write amplification.

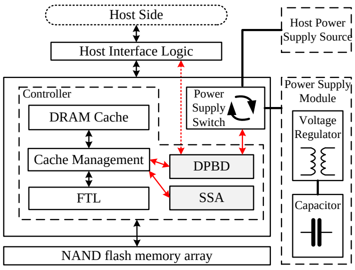


Figure 2: The framework of proposed approach.

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