## **Engineering Science Courses**

Course Code	21CSS201T	21CSS201T Course Name COMPUTER ORGANIZATION AND ARCHITECTURE				Course S Engineering Sciences					L T P C 3 0 0 3										
Pre-requisi Courses	IVII		Co-requisite Courses	Nil			ogressiv Courses		1												
Course Offer	ing Department	Computer	Science and Engineering	Data Book / Codes/Standards	٨	Vil															
Course Objectives: The purpose of learning this course is to:						Learning Program Learning Outcomes (PLO)															
CLR-1 Understand the Fundamentals of computers, Memory operations and Addressing Modes							1-6			2	3	4	5	6	7 8		10		12 1	3 14	15
CLR-2 Know about Functions of Arithmetic and Logic unit							۶.	Ħ	6	3	Ħ					Work		Finance			
CLR-3 Explore the Operations of Control Unit, Execution of Instruction and Pipelining						ing.	ienc	ae H	1	<u> </u>	J E		ge			×		au	Б		
CLR-4 Classify the Need for Parallelism, Multicore and Multiprocessor Systems						į a	Jeici.	⊒	Š	Sis	호	gu,	Sa	en l	. *	am	_	造	-		
CLR-5 Understand the Concepts and functions of Memory unit, I/O unit					<u>⊨</u> 8	Pr(%	₩ %	7	را الح اعل	e Ke	esi	9	Ħ :	& , ≝	<u>-</u>	atio	∞ ∞	ear			
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Course Outco	ourse Outcomes (CO): At the end of this course, learners will be able to:					Level of Thinking	Expected Proficiency (%)	Expected Attainment (%)	2 2	Problem Analysis	Design & Development	Analysis, Design,	Modern Tool Usage	Society & Culture	Environment & Control	Individual & Team	Communication	Project Mgt. &	Life Long Learning	PSO - 2	' I
CO-1   Identify the computer hardware and how software interacts with computer hardware				3	3	75 7	'0		3 2	-						-		1	-	-	
CO-2 Apply Boolean algebra as related to designing computer logic, through simple combinational and sequential logic circuits				3			'0		3 2	-	-				-	-		-	2	2 -	
CO-3 Examine the detailed operation of Basic Processing units and the performance of Pipelining				2	2	75 7	'0		} -	-					-	-		-	-	. 1	
CO-4 Analyze concepts of parallelism and multi-core processors.				3	3	75 7	'0		} -	-			-		-	-		-	2	2 -	
CO-5 Classify the memory technologies, input-output systems and evaluate the performance of memory system				3	3	75 7	'0		3 2	-					-	-		-	3	3 -	
compliment, 2	2's compliment, BCD	Arithmetic; Logic G	ates-AND, OR, NOT, NAND, NOR, E	al, Octal, Hexadecimal; Codes- Grey, BCD,Exce X-OR, EX-NOR.  res, Memory addresses and operations, assembly language							-				IOII, DIV	ision u	sing Si	gri ivia	mude	,15	
Unit 3: Design of ALU: De Morgan's Theorem, Adders, Multiplier – Unsigned, Signed, Fast, Carry Save Addition of summands; Division–Restoring and Non-Restoring; IEEE 754 Floating point numbers and operations.																					
Unit 4: Control Unit: Basic processing unit, ALU operations, Instruction execution, Branch instruction, Multiple bus organization, Hardwired control, Generation of control signals, Micro-programmed control; Pipelining: Basic concepts of pipelining, Performance, Hazards-Data, Instruction and Control, Influence on instruction sets.																					
	elism: Need, types , applica Case study: ARM 5 an			's classification; ARM Processor: The thumb ins	struction set, P	roce	ssor and	d CPU o	ores,	Instruc	tion E	ncodin	g form	nat, M	emory l	oad ar	d Stor	e instru	ction,	Basics	of I/O
Learning Resources	<ol> <li>KaiHwang,Faj</li> <li>GhoshT.K.,Co</li> </ol>	veA.Briggs,ComputerAr omputerOrganizationand	vatZaky, ComputerOrganization, 5 <sup>th</sup> ed.,McGr. chitectureandParallelProcessing", 3 <sup>rd</sup> ed., McGrav I.Architecture, 3 <sup>rd</sup> ed., TataMcGraw-Hill, 2011 panization, 3 <sup>rd</sup> ed., McGrawHill, 2015.	aw-Hill,2015 wHill,2016	6. David	dA.Pat	allings,Cor ttersonand n.2014	, ,													

Learning Assessment	Continuous Learning												
	Discovini and of Thinking	CLA - 1 (4	5%)	CLA - 2 (	(15%)	Final Examination(40%)							
	Bloom's Level of Thinking	Theory	Practice	Theory	Practice	Theory	Practice						
Level 1	Remember	30%	-	30%	-	30%	-						
Level 2	Understand	30%	-	30%	-	30%	-						
Level 3	Apply	20%	-	20%	-	20%	-						
Level 4	Analyze	20%	-	20%	-	20%	-						
Level 5	Evaluate	-	-	-	-	-	-						
Level 6	Create	-	-	-	-	-	-						
	Total 100%			100%	6	100%							

Course Designers								
Experts from Industry	Experts from Higher Technical Institutions	Internal Experts						
Mr.Saminath Sanjai, Borqs Technologies,Inc. Bengaluru		1.Dr.K.Vijaya, Dr.Anitha D, SRMIST						