

# SOC Design

한양대학교 공과대학 컴퓨터소프트웨어학부

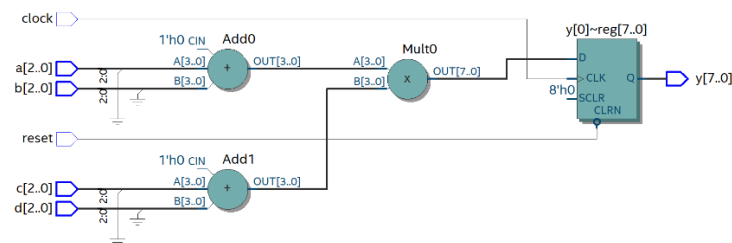
최가온(학번: 2019009261)

## [Homework 1] Non-Pipeline vs. Pipeline

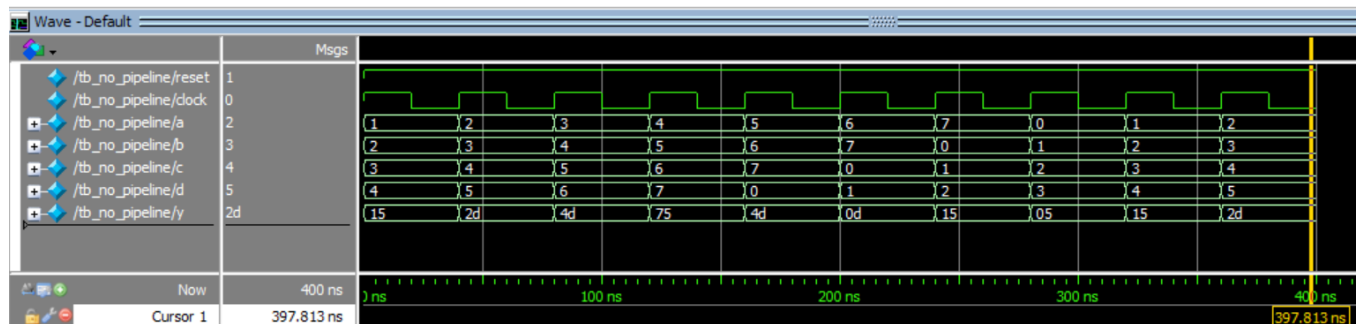
[Github Link] [https://github.com/Gaon-Choi/ITE4003/tree/main/Week07/no\\_pipeline](https://github.com/Gaon-Choi/ITE4003/tree/main/Week07/no_pipeline)

### [1] Non-Pipeline Structure

#### 1-1) RTL Viewer Schematics



#### 1-2) Waveform Result



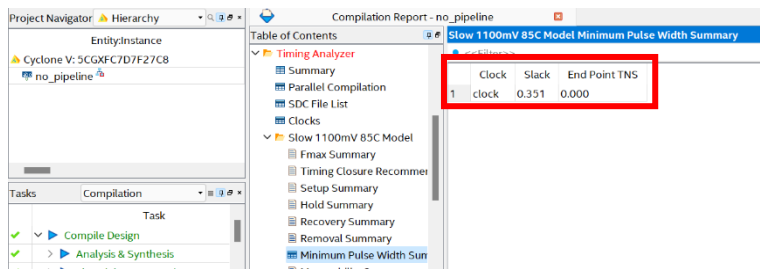
#### 1-3) SDC File

```
##
## DEVICE "5CGXFC7D7F27C8"
##

*****
# Time Information
*****
set_time_format -unit ns -decimal_places 3

*****
# Create Clock
*****
create_clock -name {clock} -period 5.000 -waveform {0.000 0.600} [get_ports {clock}]
```

## 1-4) Slack Value and Maximum Frequency



Slack value = 0.351

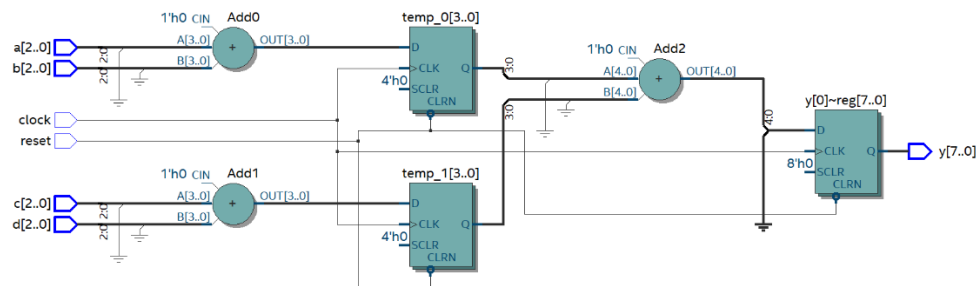
Chip Delay = Clock – Slack value =  $5.0 - 0.351 = 4.65$

Maximum Frequency =  $\frac{1}{\text{Chip Delay}} = \frac{1}{4.65} = 215\text{MHz}$

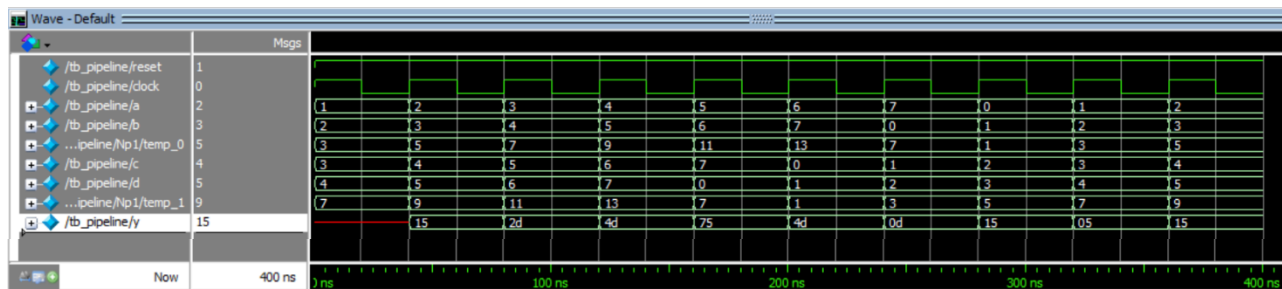
latency =  $0.5\text{ns} + 1.2\text{ns} + 10\text{ns} = 11.7\text{ns}$

## [2] Pipeline Structure

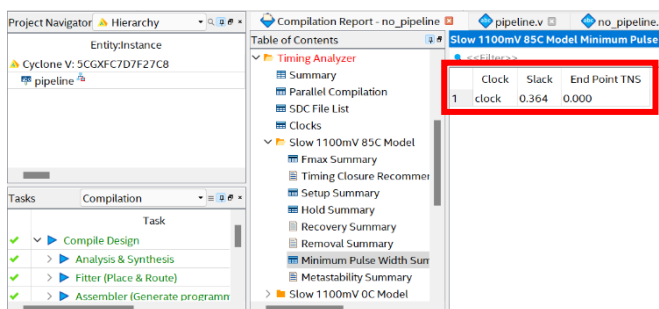
## 2-1) RTL Viewer Schematics



## 2-2) Waveform Result



## 2-3) Slack Value and Maximum Frequency



Slack value = 0.364

Chip Delay = Clock – Slack value =  $5.0 - 0.364 = 4.636$

Maximum Frequency =  $\frac{1}{\text{Chip Delay}} = \frac{1}{4.636} = 215.70\text{MHz}$

latency =  $\max(0.5\text{ns} + 1.2\text{ns} + 10\text{ns}) = 10.0\text{ns}$