Real-Time Adaptive Signal Conditioning System for Wide Dynamic Range Inputs

I. Plain explanation

The diagram represents a **Real-Time Adaptive Signal Conditioning System for Wide Dynamic Range Inputs**.
The system automatically regulates the amplitude of an input signal by applying level-dependent gain control.

It continuously monitors the input signal level, compares it to a predefined threshold, and dynamically adjusts the gain of a voltage-controlled amplification stage to maintain the output signal within a controlled range.

The system operates in real time using a feed-forward control architecture, enabling fast response to changes in input amplitude without directly feeding back the output signal.

II. Detailed explanation of how the system works

1. Signal Input

The system receives an analog input signal whose amplitude may vary significantly over time.

2. Voltage-Control

The input signal is fed directly into a Voltage-Controlled Amplifier.
This block applies a gain to the signal, where the gain value is controlled by an external control voltage. The VC is responsible for increasing or decreasing the signal amplitude in real time.
At this stage:

The signal path remains continuous

No frequency modification is intended

Only amplitude scaling is applied

3. Envelope Detector

In parallel with the main signal path, the input signal is routed to an Envelope Detector.

The purpose of this block is to extract a representation of the signal's amplitude (or level), independent of its frequency content. This is typically achieved through rectification followed by low-pass filtering, producing a slowly varying control signal.

This block provides the system with real-time information about how "strong" the input signal is.

4. Signal Comparator

The output of the Envelope Detector is fed into a Signal Comparator, where it is compared against a predefined reference threshold level.

If the detected signal level is below the threshold, no gain reduction is required.

If the detected signal level exceeds the threshold, the comparator generates a control signal indicating that gain reduction should be applied.

This block implements the decision logic of the system.

5. Control Signal Generation

The output of the Signal Comparator is converted into a control voltage that determines how much gain reduction is applied by the VC.

The magnitude and timing of this control signal govern:

How quickly the system responds to increases in input level

How smoothly the gain returns to normal when the input level decreases

This behavior defines the system's dynamic response characteristics.

6. Signal Output

The processed signal exits the system through the output block.
As a result of the adaptive gain control, the output signal exhibits a reduced dynamic range compared to the input, remaining within a controlled amplitude range even when the input varies significantly.

7. System block illustration

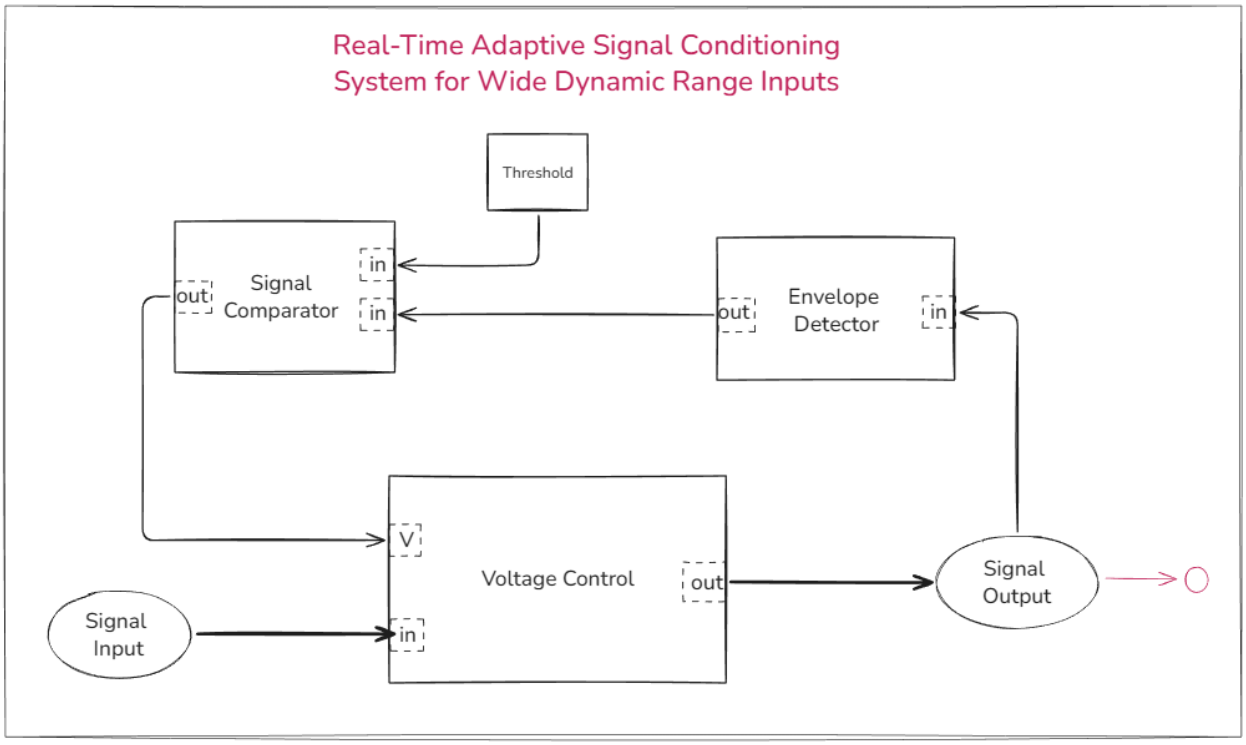

Fig. 1. block diagram

III. Deployment

1. Voltage-Control

Available methods

-Multi Variable Resistors Low Pass filtering

-Diode ladder filtering

Chosen Method:

Diode ladder filtering this method consists combining a multi set 1N4138 diodes in series will act as a variable resistance in function of the control-voltage applied to the input of the CV (V).

this method will cause less distortion and more control of the CV and its generally more cost-effective and easy to assemble.

1.1 functioning

I have selected the diode technique, which involves utilizing many diodes as resistors. It functions by supplying symmetric voltages to the diode ladder's beginnings and a non-inverted buffered input at the center. This is the fundamental idea behind the diode ladder. The output signal is picket as is from the middle of the ladder if the symmetric voltages are zero. If the symmetric voltages are not equal to zero, there will be a current flowing from the positive rail to the negative rail and simultaneously dragging some of the current from the input signal, so the output signal will be the same as the input but lower in amplitude (volume). Therefore, the more the symmetric voltages increase, the lower the input will become.

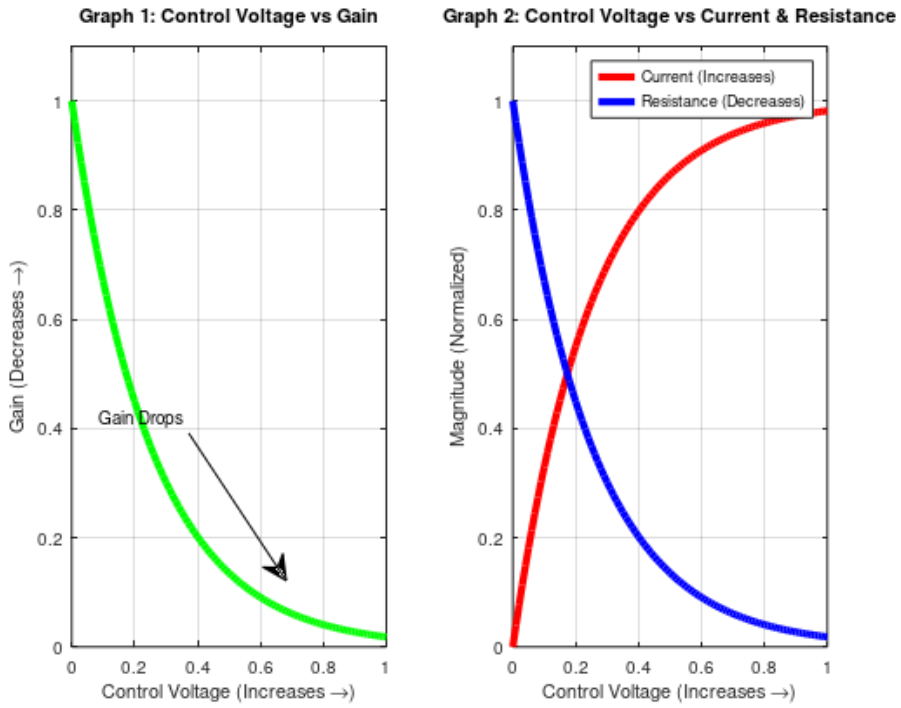

Fig.2,3. Diode Ladder Control Characteristics

1.2 Schematic

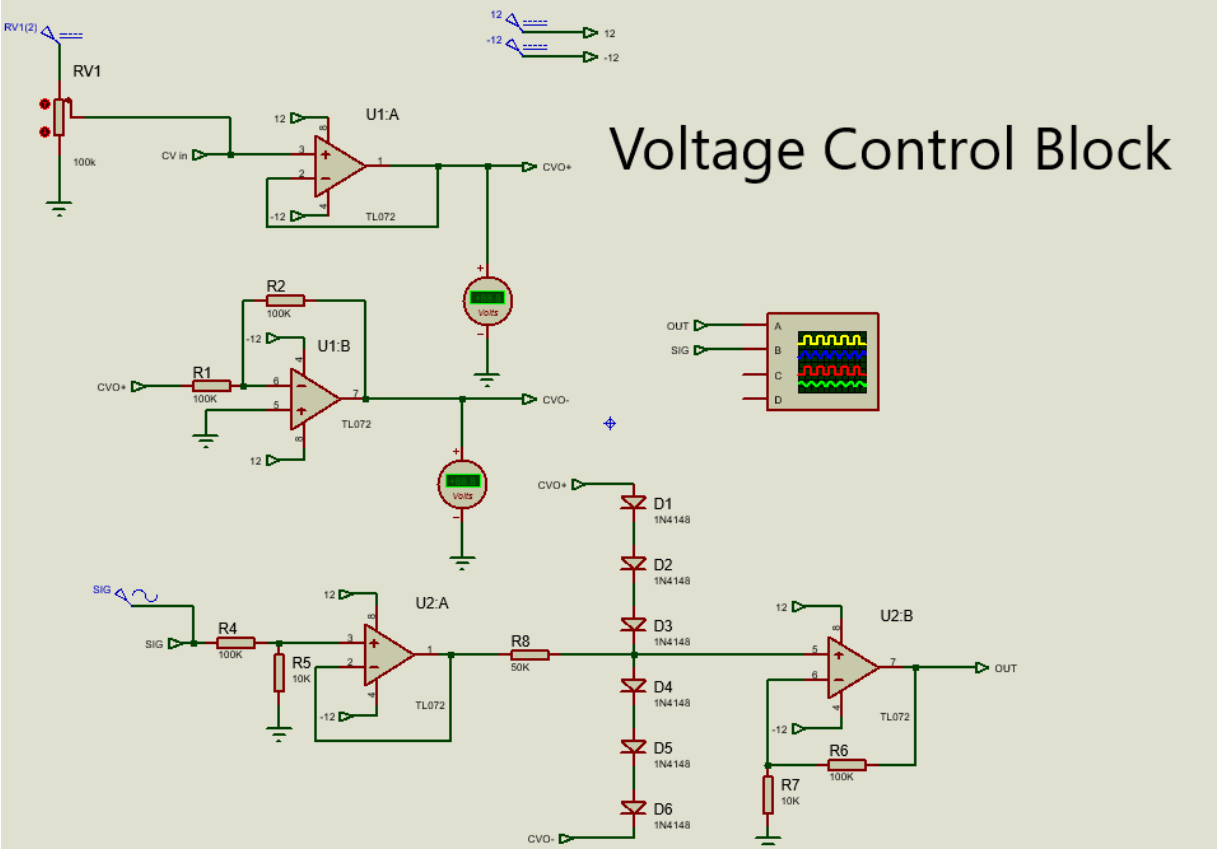

Fig. 4. Voltage Control Block schematic

1.3 Simulation

CV=0

During this simulation the CV=0 → Gain =1

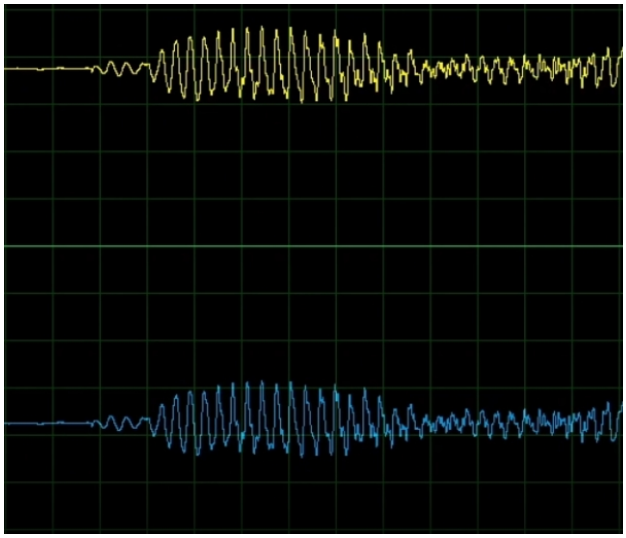

Fig. 5. Simulation 1

CV=2

During this simulation the CV=0 → Gain < 1

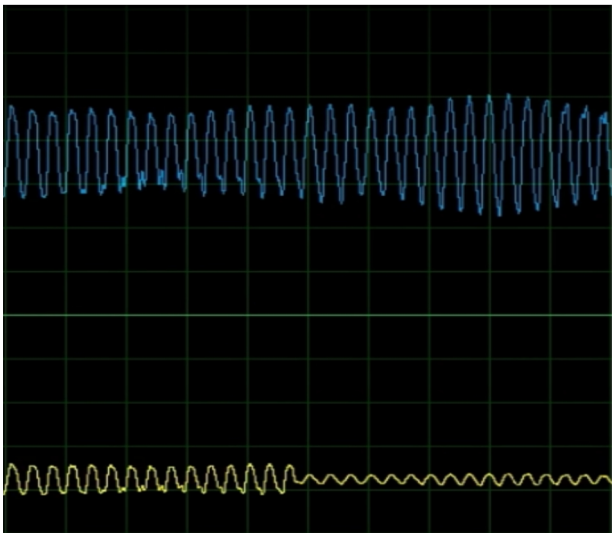

Fig. 6. Simulation 2

2. Peak Detector

Available methods

There are several approaches of obtraining in the framework of peak detection, and these are a few of them.
Diode-capacitor circuit
Diode-capacitor-Amplifier
Diode-capacitor-RC coupling

Chosen Method:

The Diode-Capacitor-RC coupling is the technique I have selected because of its simple circuit, high efficiency, and high response time.

2.1 functioning

We can create a peak detector by wiring a buffer op amp through a diode and an RC coupling. When the input signal increases, the capacitor charges, and when the input signal decreases, the current flowing from the capacitor will drain through the resistor to ground (the diode blocks the other sense of current flow). This allows us to detect the output from the resistor.

2.2 Schematic

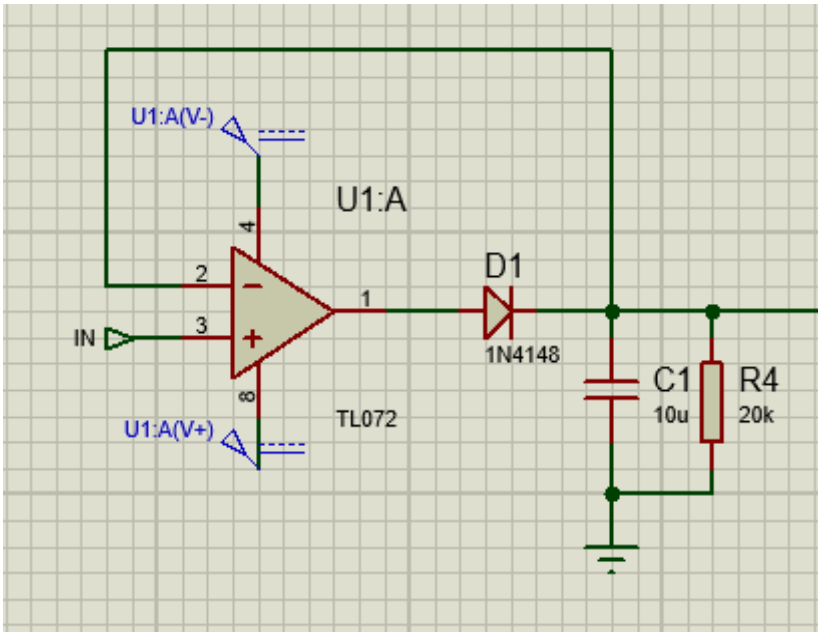

Fig. 7. Simulation Peak detector

2.3 Simulation

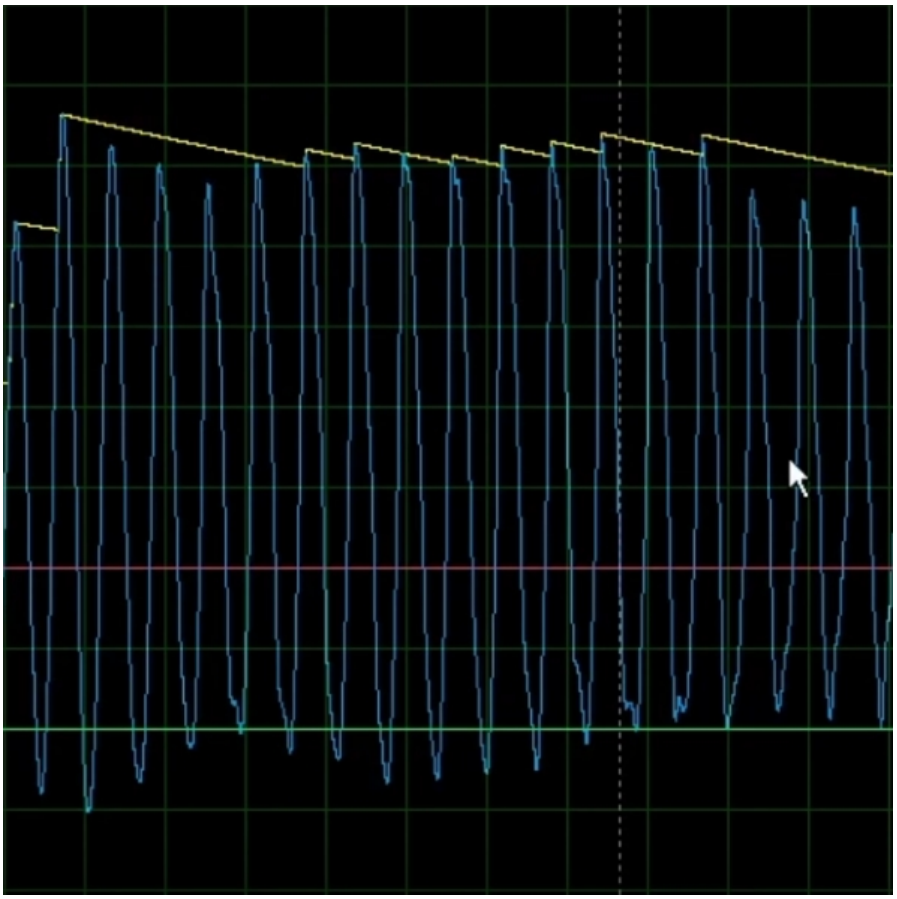

Fig. 8. Simulation Peak detector

Note

Because of its orientated diodes, our control voltage block (built on the preceding block) does not require the negative peaks. In any case, since all of the signals will be somewhat sinusoidal, we do not require the negative sections.

3. Signal Comparator Block

3.1 functioning

The comparator block's operation is really simple, and we do it by utilizing a differential amplifier with gain 1.
The threshold voltage is wired to the amplifier's non-inverting input, so a negative output indicates no change in the signal because the input it is below the threshold, and a positive output indicates a decrease in the signal because it is above the threshold. The output of the comparator block will be the input of the VC block.

Since our input is maximum at 12 volts peak to peak, the threshold element will be a variable voltage that swings between 0 and 6 volts.

3.2 Schematic

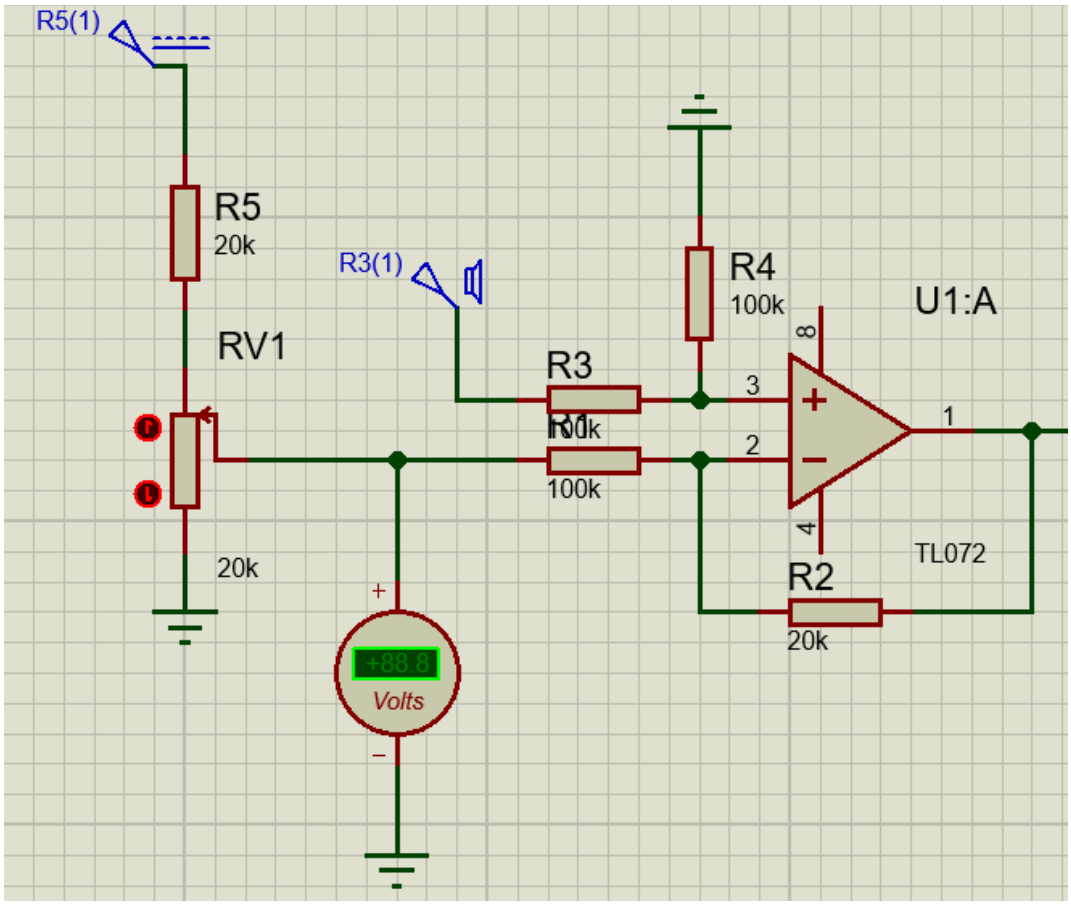

Fig. 8. Comparator Block

4. Assembling

The assembly process is straightforward, combining the previous blocks together and fine-tuning the wiring and input/output pins.

4.1 Schematics

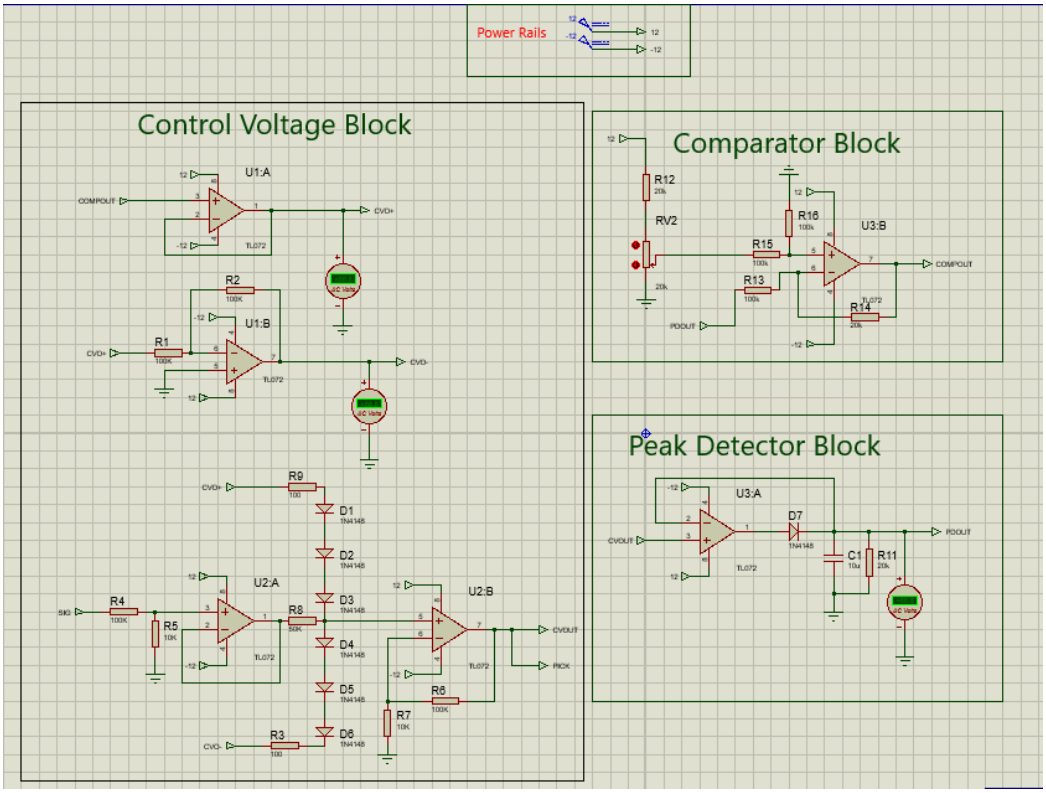

Fig. 9. Assembled Blocks

5. Analyzing

From the tests that I have made through the simulation and my own thinking, I identified a few problems that have caused the system not to fail completely, but it is not behaving as we would like. First, the control voltage inputs (same as the comparator outputs) are always positive even when the threshold is set at 0 volts, so the output signal from the CV will always be shrunken down by some unwanted factor. I also noticed that in the CV input, if the input difference went above 2 volts, the output will be completely silenced, and the signal in the output is somewhat distorted.

6. Proposed Solutions

The main issue with the output being silenced is that the CV input is becoming far too high (approximately 2.5 volts), which will widely open the diodes and drain the output signal completely to ground. My solution to this is to connect a voltage divider of 1/2 between the comparator output and the CV input.

Through experimentation, I discovered that using a 30K resistor and a 10K resistor with a variable potentiometer works best for our desired work.

Schematics After adjustment

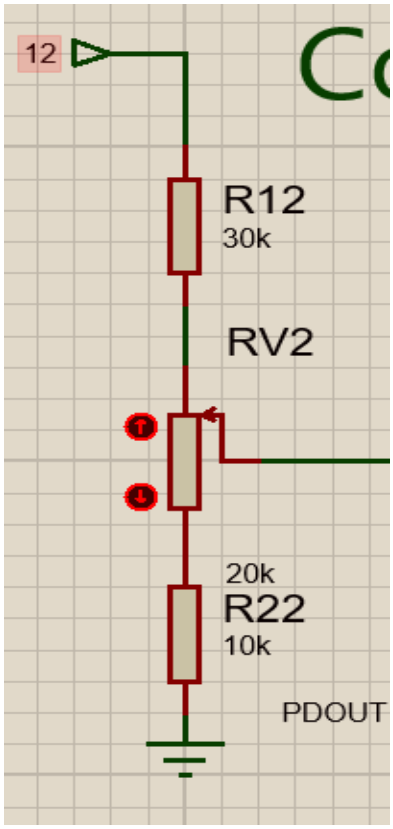

Fig. 10. Refined POT

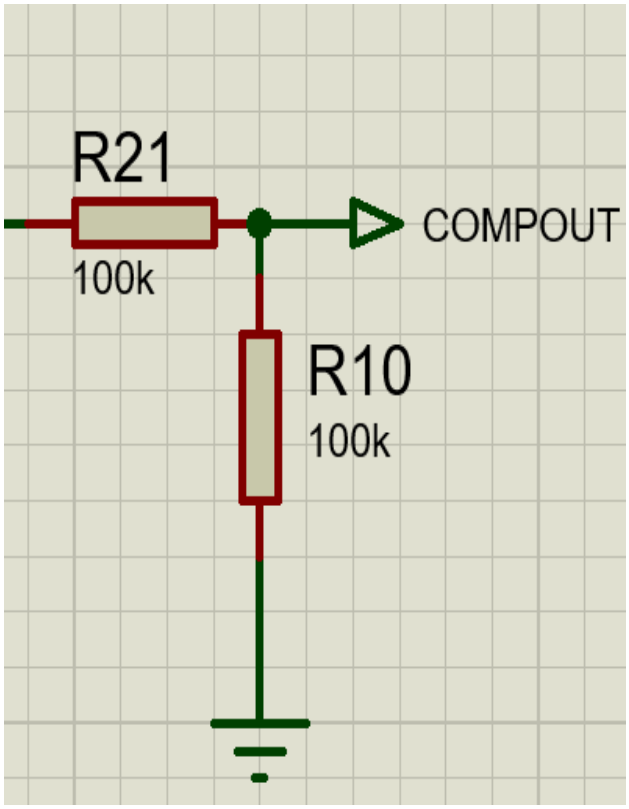

Fig. 11. RefinedCompout

7. Adding features

7.1 Attack

Definition

Attack is how quickly the system starts reducing volume after a signal exceeds the desired threshold.

in other-words is how much does the system should wait before reducing the volume of the input.

Explanation

During the testing and debugging phase of the project and its simulation, I identified a simple and effective method for implementing the attack control. This approach is based on manipulating how quickly the peak detector capacitor responds to the incoming signal peak. By slowing the charging rate of the capacitor, the peak detector responds more gradually, which automatically reduces how quickly peak information is passed to the comparator.

As a result, replacing the fixed resistor between the diode and the capacitor with a variable resistor provides a practical solution for implementing the attack feature. In this design, a 100 kΩ potentiometer was used for this purpose.

7.2 Release

Definition

When the input signal level drops below the threshold, the release time is the amount of time needed for the control system to eliminate gain reduction and return to its nominal condition. It controls how the system recovers after attenuation.

Explanation

The release time is implemented using a simple RC-based approach.

The release time constant is defined as $\tau = R \cdot C$, where 10 µF is the fixed value of the capacitor.

The release time is controlled by varying the resistance in the discharge path using a 100 kΩ potentiometer.

To prevent the discharge path from being shorted to ground when the potentiometer is set to its minimum value, a 5 kΩ fixed resistor is placed in series with the potentiometer. This ensures a non-zero minimum resistance and provides safe, stable operation.

As a result, the release time constant is adjustable over a range defined by:

$\tau = (5\ k\Omega \text{ to } 105\ k\Omega) \times 10\ \mu F$ or $\tau \in [50\ ms, 1.05\ s]$.

Schematics After adjustment

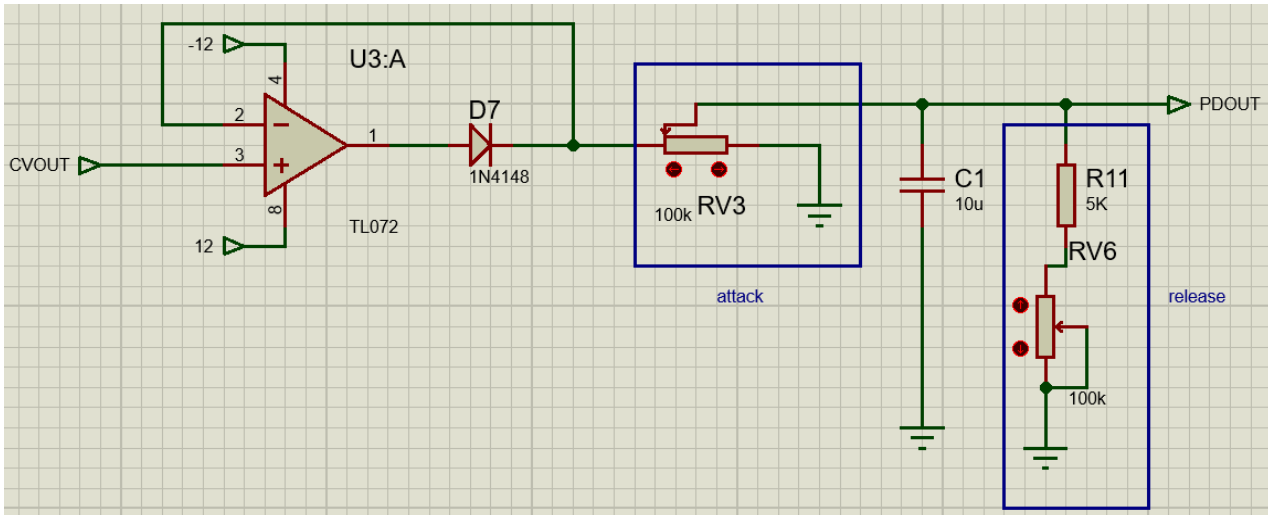

Fig. 12. Attack & Release

7.2 Ratio

Definition

Compression ratio defines how much the system reduces the output signal level relative to the amount by which the input level exceeds a defined threshold.

Explanation

the ratio determines the relationship between input level exceedance and the resulting gain reduction applied by the system. In the proposed design, the ratio is implemented by scaling the comparator output using a variable voltage divider. By attenuating the control voltage that drives the gain-control stage, the system adjusts how aggressively gain is reduced once the threshold is exceeded. Higher divider output results in stronger gain reduction (higher ratio), while lower divider output produces gentler compression behavior (lower ratio).

Schematics After adjustment

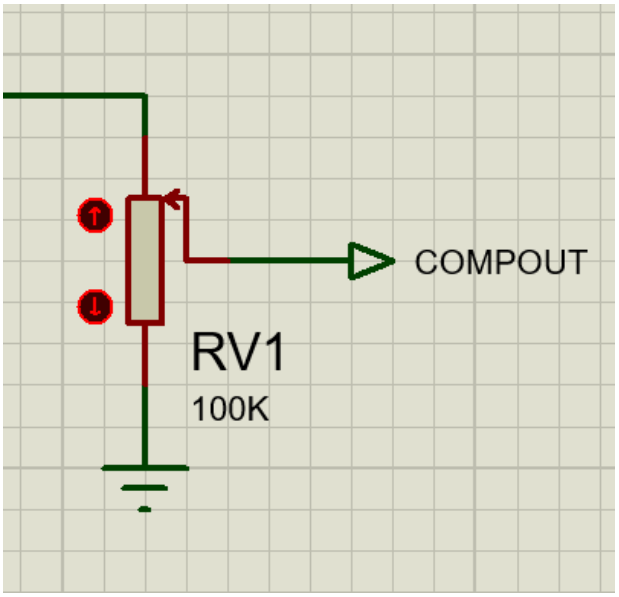

Fig. 13. Ratio

8. Analyzing