Politecnico di Torino

System design project

Project8

IP-core Manager for FPGA-based Designs (RT level)

Report on the activities held

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CHAPTER 1

Report on the activities held

Setting up the group and the environment to work in team

07/03/2017 12/03/2017	**Group formation and selecting the homework** Discussing the possibility to work in a team of 4 people, and the preference of the homework available.
15/03/2017	**Confirmation of the group** It has been announced the groups and the related project. Another member joined the team. We also exchanged the email address and the telephone number to fasten the communication between members abroad (Whatsapp, Skype, Telegram...).
22/03/2017 27/03/2017	**Redmine platform** Set-up the Redmine platform. Understanding how to use it, register, open a new topic, upload file, register time.

Understanding the environment and the requirements

22/03/2017 03/04/2017	**SEcube documentation** Reading the SEcube documentation and write down the analysis.
03/04/2017 10/04/2017	**Communication Protocol v.1.0** Meeting with the professor on 3^{rd} April and on 4^{th} April. Then we discussed with other projects team (project 13, 7, 14) to enhance the protocol.
11/04/2017 20/04/2017	**Communication Protocol v.2.0** During Easter Holyday, the project 13 sent the second version to the teacher, but other modifications were needed.
26/04/2017 02/05/2017	**Communication Protocol v.3.0** Discussion with the team involved. Then the project 13 submitted the final protocol.

Project Development and Documentation

18/04/2017 23/04/2017	**GIT setup and backbone in VHDL** Read GIT manual, GIT set up. Write in VHDL the interface of all the components.
21/04/2017 26/04/2017	**Presentation of the 26^{th} April** It has been requested 3 slides talking about: - Gantt - Milestones - Deliverables - Issues already closed - still open..
02/05/2017 10/06/2017	**Developemnt of the IP-core Manager and documentation** -Split the work among us - Deciding the communication among the components - Write down the architecture, upload it on GIT, perform some tests - Report timing and area and synthesys results with LATTICE Diamond - Documentation and presentation

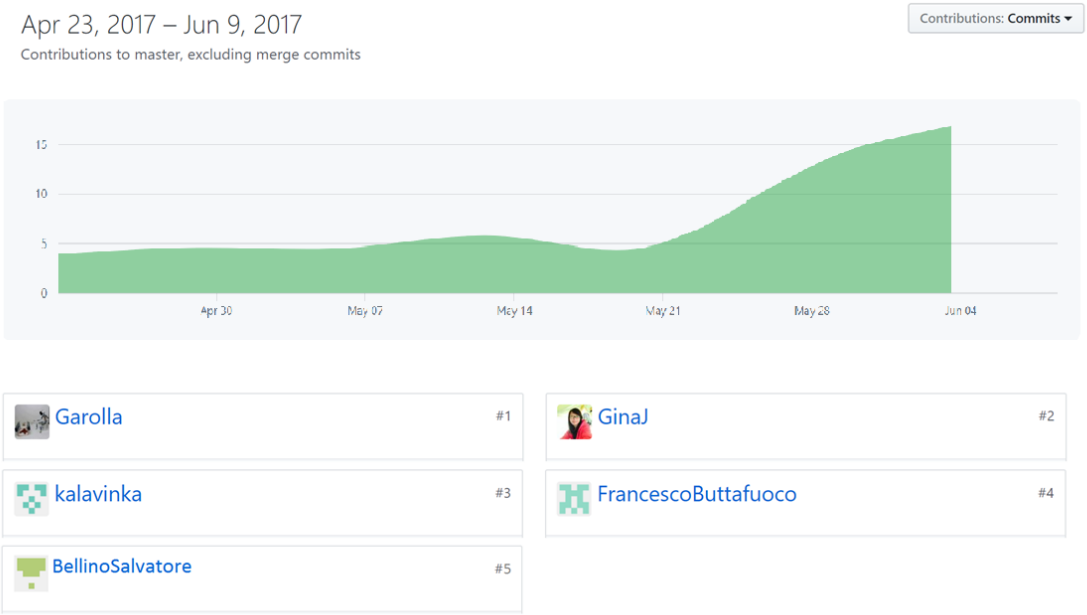

Figure 1.1: Our project on GIT, with us as contributors

Assignment of the tasks

GAROLLA Emanuele	-Backbone of project in VHDL -Dual port buffer 64x16 (Behavioral) -Assemble all files -Final Testbench of the overall architecture -Slides
JIANG Gina	-Documentation for the 26^{th} April -Documentation for the 27^{th} May -Report timing and area, synthesys result (LATTICE Diamond) -Technical report
BELLINO Salvatore	-Dual port buffer 64x16 (Behavioral) -Register 0 -Register 16 bits -Decoder -Testbench for the data buffer -Slides
FORNO Evelina	-Dummy IP-core -Adder IP-core (FSM with 3 stage) -First version of testbench -Slides
BUTTAFUOCO Francesco	-IP-Manager Behavioral -Enabling the right IP core -Propagate the right Data from the selected IP core to the Buffer/CPU -Interrupt Handler -Slides

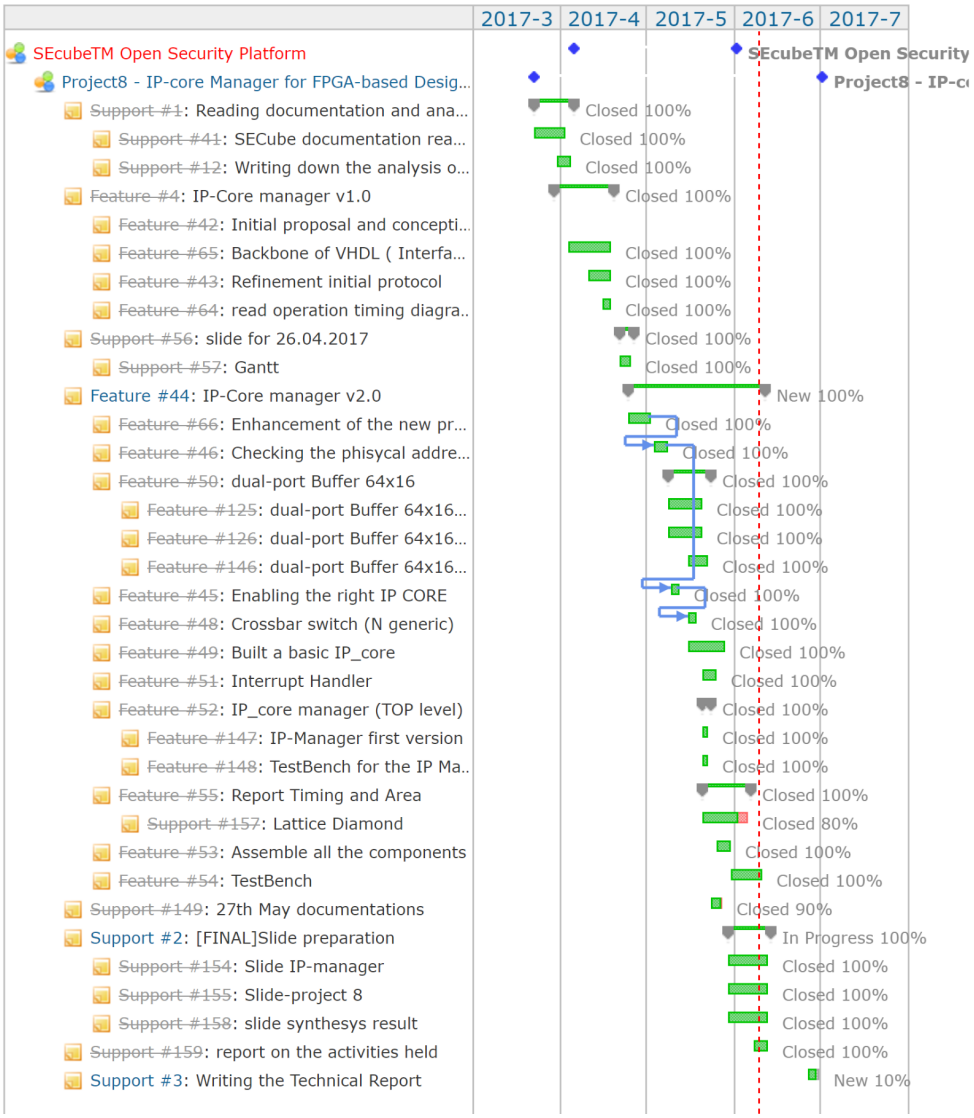

Figure 1.2: Gantt chart of our project