



Politecnico di Torino

System design project

Project8

IP-core Manager for FPGA-based Designs (RT level)

Final Report

Master degree in Computer Engineering
Specialization in Embedded Systems

Referents:

Prof. Paolo Ernesto Prinetto
PhD. Student Giuseppe Airò Farulla

Authors:

Emanuele Garolla
Gina Jiang
Evelina Forno
Francesco Buttafuoco
Salvatore Bellino

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CHAPTER 1

Introduction

1.1 Multi IP-core systems and the IP-core Manager

A multi IP-core system is a component with two or more independent unit each one designed for a different purpose. These cores are deployed into the FPGA and are used for enhancing performance, implementing functions, and simultaneous processing of multiple tasks. However due to the increasing complexity, a IP core manager is required to handle context switching, scheduling, and interrupt handling.

The first and basic task for this core manager is to enable the connection between the CPU and the selected core. More in particular this means exchanging the data in the required time as described in the protocol. The CPU can talk to one and only one core, therefore the core manager will disregard other cores whether they finished or not their task.

The exchanging of data is done by a means of a dual-port buffer (64x16). The buffer is the component that communicate the physical address of the interested core from the CPU to the IP-core manager (and viceversa) and exchange the data between the CPU and the IP-cores.

Even for the data buffer we have some constraints: only one core at a time can talk to the buffer. This requirement is satisfied thanks to the IP manager.

As for the priority of the cores, we put the most priority core at $port_0$ and the least one to the last port, i.e. $port_{n-1}$.

CHAPTER 2

System's architecture

2.1 IP Manager interfaces

A multi IP-core system requires a IP core manager to handle the complexity of this system. Main tasks of the IP Manager are the correct exchange of data between the target IP and the CPU. Another critical task is the interrupt handling. Figure 2.1 shows the overall architecture of the whole system adopted.

As shown in the figure, the IP manager has a standard interface with the buffer. This interface is used to redirect data to/from the target IP and to access the buffer itself (e.g. to write the row 0).

However, it is provided with a direct access (read-only) to the internal element to speed-up the routing process whenever a new transaction begins. It is important to underline that for each instantiated IP there are a set of standard signals and some protocol-specific signals. The former are the very same signals used for accessing the buffer, whilst the latter are used for handling interrupt requests. For sake of clarity, we report the function of the IP-specific signals for the generic IP x:

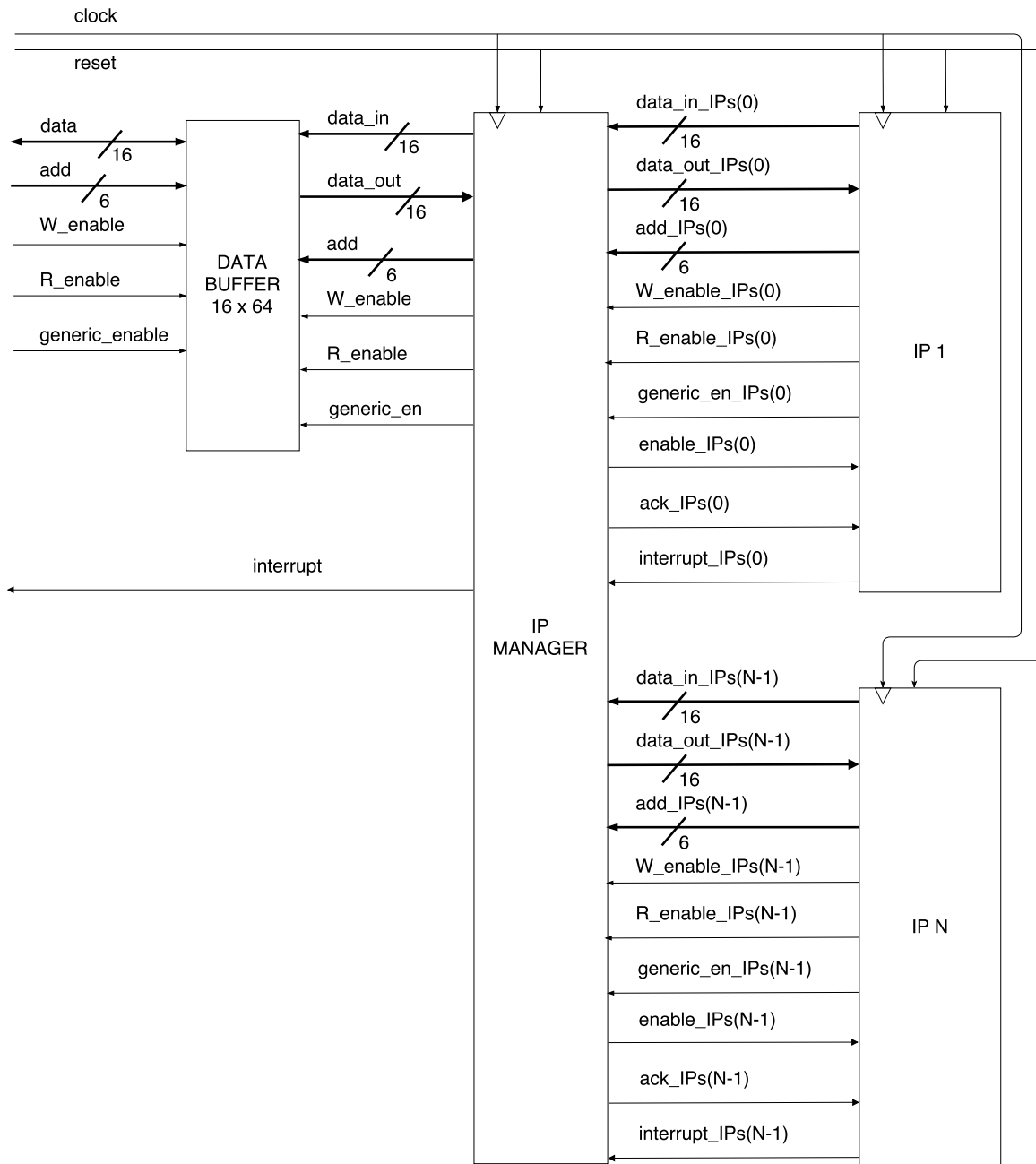


Figure 2.1: System architecture

CHAPTER 3

IP-core Manager functionalities

3.1 Enabling the right IP

The first and basic task for this core manager is to enable the connection between the CPU and the selected core. More in particular this means exchanging the data in the required time as described in the protocol. The CPU can talk to one and only one core, therefore the core manager will disregard other cores whether they finished or not their task. We know that the CPU writes at row_0 what it wants to do. Here we can read the physical address of the chosen IP core. If we know that the 1st core is selected, than the IP manager has to enable the 1st core (i.e. $port_0$) and disable all the other ones, thus having the following signal:

$$\begin{aligned} enable_0 &= '1' \\ enable_1 &= '0' \\ enable_2 &= '0' \\ &\vdots \\ enable_{n-1} &= '0' \end{aligned}$$

We can put all these signal together as if they were an array.

To make this kind of operation, a conversion is required.

We can clearly see that only one bit is at '1', while the others are at '0', this is due because the CPU can talk at most to only one IP-core.

The feature of having at most one bit at '1' is the well known *one hot encoding*.

We implicitly implemented a "kind" of *binary to one hot encoding* converter.

At row_0 we read the physical address, and we raise the right enable signal, keeping the other ones at '0'.

Figure 3.1 shows this functionality.

A small adjustment has been done, since the physical address 0 is reserved to the IP

manager, whilst the *IP core 0* has as physical address *1*.

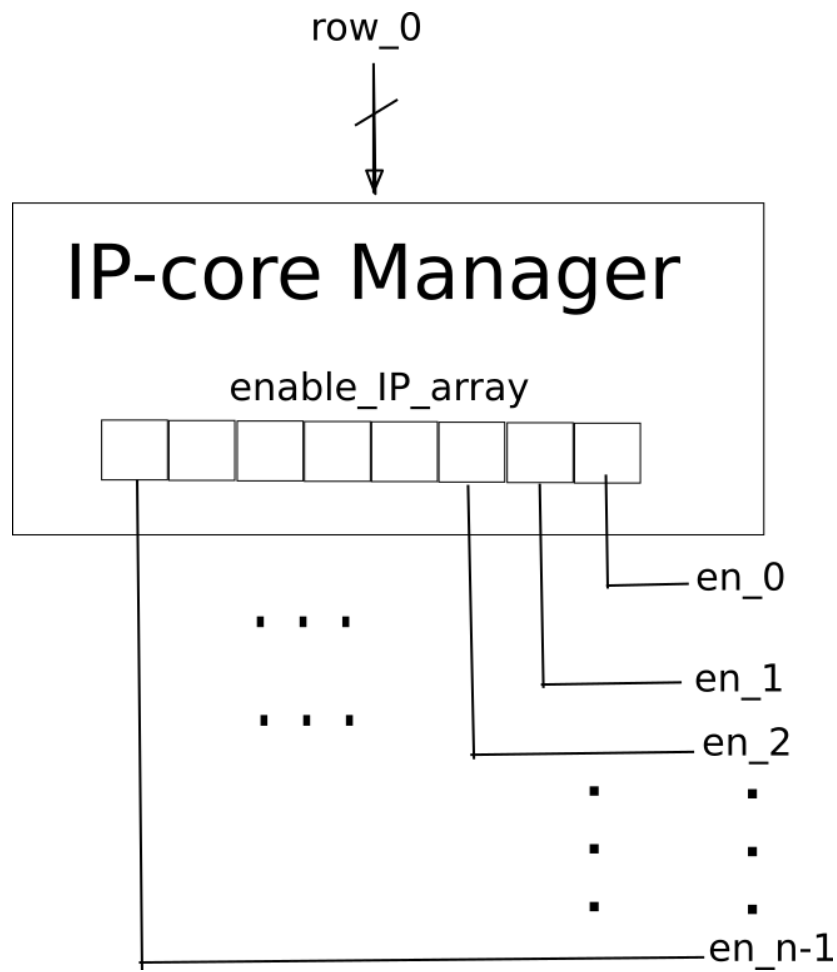


Figure 3.1: Enabling the right IP core

This component is active during the rising edge of the clock and when the CPU wants to start a transaction.

3.2 Connecting the signals

The IP core Manager has the duty to make possible the exchanging of data between the CPU (buffer) and the selected IP core, in both direction i.e. from CPU to the IP core and from the IP core to CPU. In order to select the right input among the N ones of the IP cores, we can just look at row_0 , bits $[11 : 0]$, because here there is the physical address of the selected core.

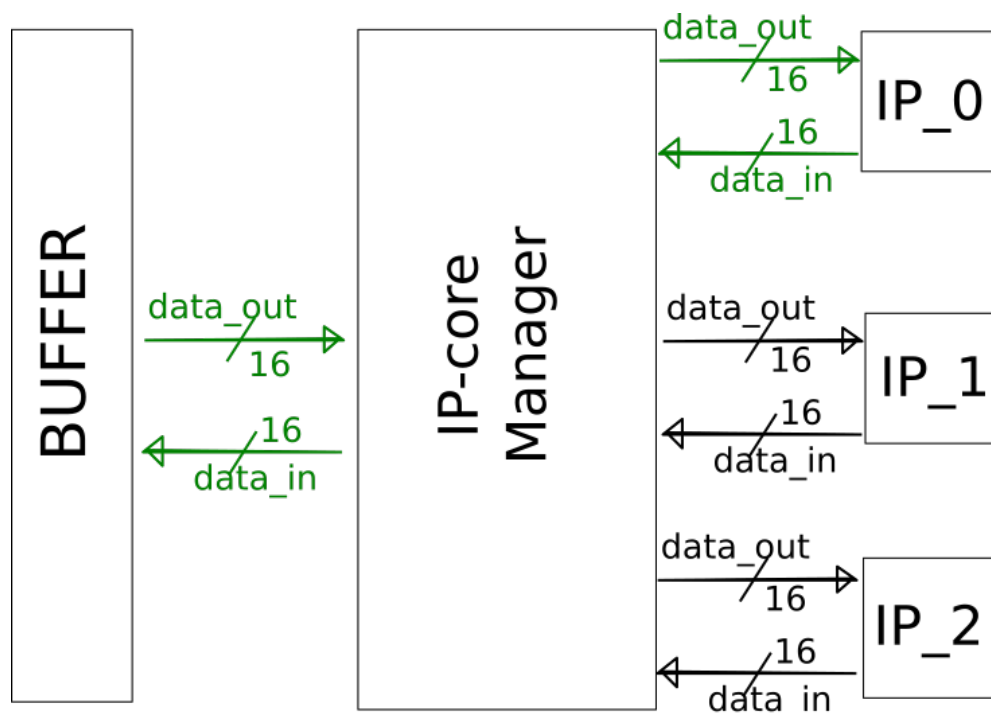


Figure 3.2: connecting the signal with IP_0 , supposing row_0 ask for the first IP core

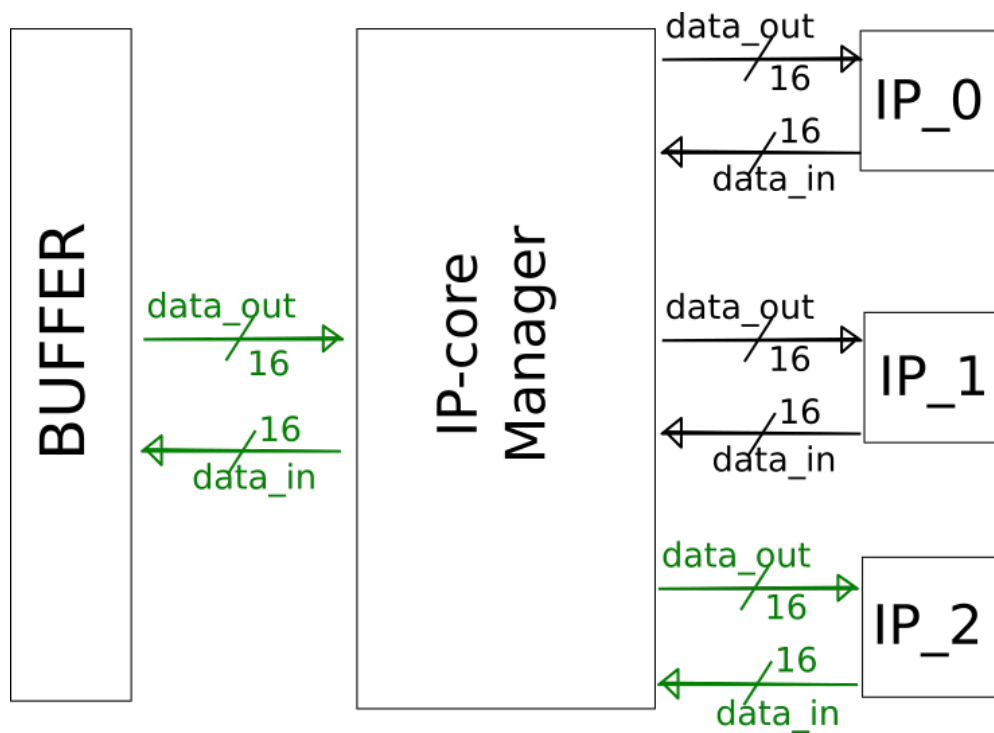


Figure 3.3: connecting the signal with IP_2 supposing row_0 ask for the third IP core

3.3 Interrupt Handler

The IP-core manager has to manage the case when a single or multiple core raise an interrupt request. However since the architecture is a master (CPU) slave (FPGA) architecture, the IP manager must guarantee that an interrupt request from one or more of IPs do not interrupt a transaction started by the master. In other words, the interrupt handler will be active at the end of a transaction.

In the case when multiple core raise the interrupt, the IP core manager will give priority to the core with the most priority level which is connected to the lowest port i.e. $port_0$.

In order to do so, we collect all the $interrupt_x$ signals of the cores into an array. Then we search for the LSB at '1'. Finally we convert the position of this bit into the physical address of the core requesting the interrupt.

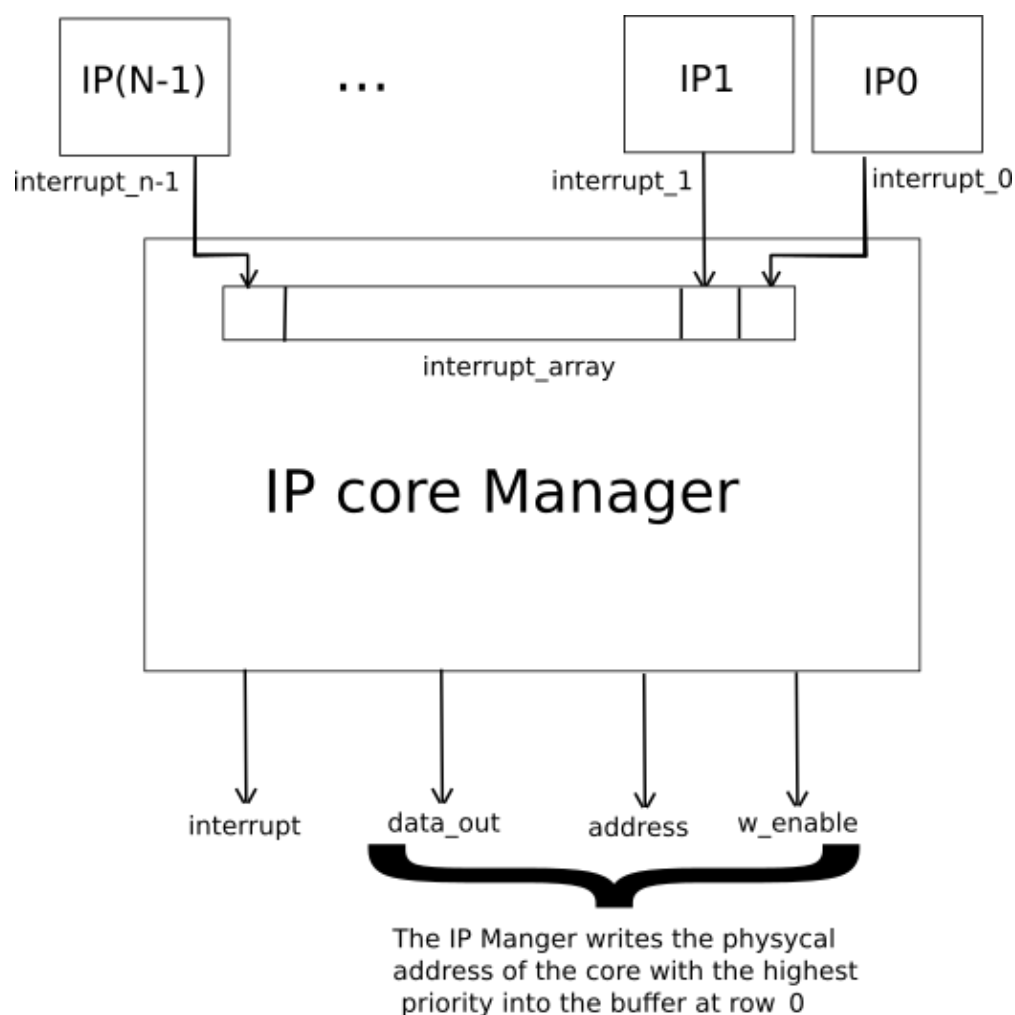


Figure 3.4: Interrupt Handler

The work of the IP Manager is first to check if there is any interrupt, this can be done by comparing the value of the interrupt vector. If the value is zero, that means that nobody raised the interrupt.

Otherwise it has to find the core with the highest priority.

In order to do so, it can iterate N times, i.e. from $i = N - 1$ to $i = 0$. In this loop it checks the bit in $Interrupt_array(i)$, if it is '1', then the variable i is the physical address of the IP core requesting an interrupt. However, we keep the loop, because it is possible to have an IPcore with an higher priority.

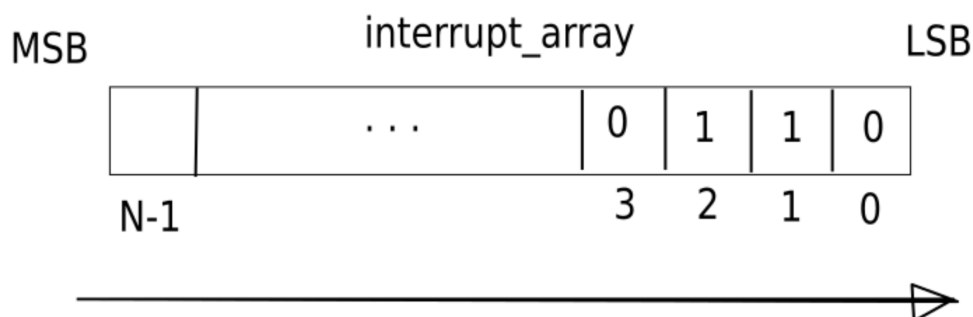


Figure 3.5: A possible interrupt vector

For instance, let's take the interrupt vector shown in fig. 3.5.

When iterating with $i = 2$, we want to send the address of the third core, but when we decrease the counter $i = 1$, we have to update this address. When $i = 0$ we leave everything unchanged.