



Politecnico di Torino

# System design project

## Project8

### IP-core Manager for FPGA-based Designs (RT level)

### Report on the activities held

Referents:

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## CHAPTER 1

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# Report on the activities held

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### Setting up the group and the environment to work in team

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07/03/2017	<b>Group formation and selecting the homework</b> Discussing the possibility to work in a team of 4 people, and the preference of the homework available.
12/03/2017	
15/03/2017	<b>Confirmation of the group</b> It has been announced the groups and the related project. Another member joined the team. We also exchanged the email address and the telephone number to fasten the communication between members abroad.
22/03/2017	<b>Redmine platform</b> Set-up the Redmine platform. Understanding how to use it, register, open a new topic, upload file, register time.
27/03/2017	

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### Understanding the environment and the requirements

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22/03/2017	<b>SEcube documentation</b> Reading the SEcube documentation and write down the analysis.
03/04/2017	
03/04/2017	<b>Communication Protocol v.1.0</b> Meeting with the professor on 3 <sup>rd</sup> April and on 4 <sup>th</sup> April. Then we discussed with other projects team (project 13, 7, 14) to enhance the protocol.
10/04/2017	
11/04/2017	<b>Communication Protocol v.2.0</b> During Easter Holyday, the project 13 sent the second version to the teacher, but other modifications were needed.
20/04/2017	
26/04/2017	<b>Communication Protocol v.3.0</b> Discussion with the team involved. Then the project 13 submitted the final protocol.
02/05/2017	

## Project Development and Documentation

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18/04/2017	<b>GIT setup and backbone in VHDL</b>
23/04/2017	Read GIT manual, GIT set up. Write in VHDL the interface of all the components.
21/04/2017	<b>Presentation of the 26<sup>th</sup> April</b>
26/04/2017	It has been requested 3 slides talking about: <ul style="list-style-type: none"> <li>- Gantt</li> <li>- Milestones - Deliverables</li> <li>- Issues already closed - still open..</li> </ul>
02/05/2017	<b>Developemnt of the IP-core Manager and documentation</b>
10/06/2017	-Split the work among us - Deciding the communication among the components - Write down the architecture, upload it on GIT, perform some tests - Report timing and area and synthesys results with LATTICE Diamond - Documentation and presentation

## Assignment of the tasks (part 1/2)

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GAROLLA Emanuele	-Backbone of project in VHDL -Dual port buffer 64x16 (Behavioral) -Assemble all files -Final Testbench of the overall architecture -Slides
JIANG Gina	-Documentation for the 26 <sup>th</sup> April -Documentation for the 27 <sup>th</sup> May -Report timing and area, synthesys result (LATTICE Diamond) -Technical report
BELLINO Salvatore	-Dual port buffer 64x16 (Behavioral) <ul style="list-style-type: none"> <li>-Register 0</li> <li>-Register 16 bits</li> <li>-Decoder</li> </ul> -Testbench for the data buffer -Slides

## Assignment of the tasks (part 2/2)

FORNO Evelina

- Dummy IP-core
- Adder IP-core (FSM with 3 stage)
- First version of testbench
- Slides

BUTTAFUOCO  
Francesco

- IP-Manager Behavioral
- Enabling the right IP core
- Propagate the right Data from the selected IP core to the Buffer/CPU
- Interrupt Handler
- Slides

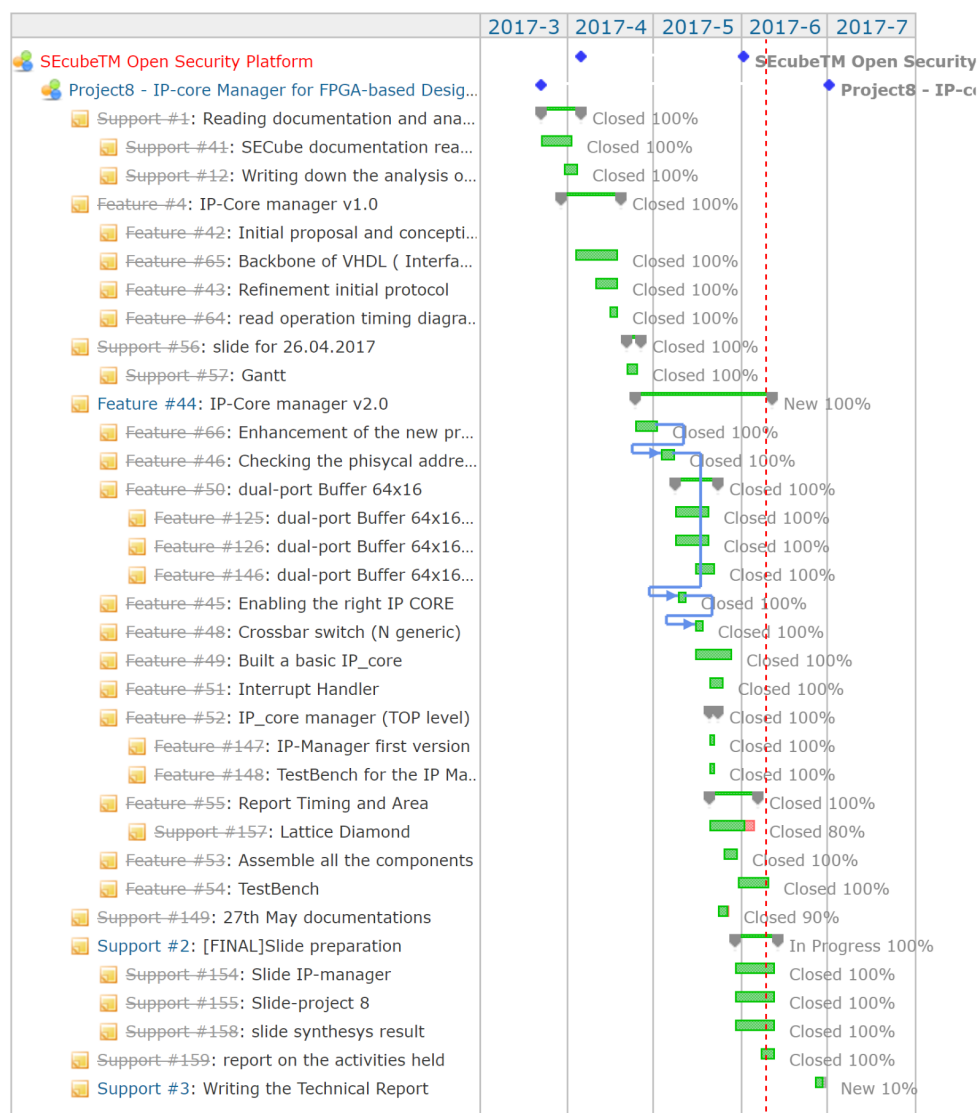


Figure 1.1: Gantt chart of our project