Politecnico di Torino

System design project

Project8

IP-core Manager for FPGA-based Designs (RT level)

Report of the Milestones

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Milestones already met

02/05/2017 | **Final Protocol specification**
It has been decided the CPU transaction, the interrupt handling protocol,and the format of the 16 bits control word that the CPU writes at address *0* for the IP manger.

12/05/2017 | **Enabling the right IP**
Given the physical address of a given IP-core, the IP-core manager has to enable the communication between the interested IP-core and the CPU while disabling the other cores.

18/05/2017 | **Cross switching**
A switch is needed when we have to propagate to the Data Buffer and to the CPU the right *data_in*, among the *N* *data_in* of the *N* IP-cores. The same thing is required in the other sense, when we have to send the data from the CPU to the selected IP-core, i.e. not to all of them.

20/05/2017 | **Dual-port Buffer 64x16**
We have written 2 version of the dual-port Buffer 64x16.
The first one is written with a behavioral architecture, while the second one is with a structural architecture.
The structural architecture is more complex because it requires to have all the subcomponent instantiated and connected in the right port between them.

25/05/2017 | **Interrupt Handling**
The IP-core manager has to manage the case when a single or multiple core raise an interrupt request.
We will give priority to the core with the most priority level.

Future developments and the planning

28/05/2017 | **Basic IP-Core**
Built a basic IP-core with the required interfaces.
This component will be used to test the correct behaviour of the IP-core manager

05/06/2017 | **Assemble all the components and Test**
Connect all the entities and the components.
Simulate a scenario for the IP-core manager and check the correct behaviour of everything.

09/06/2017 | **Analyze the possibility to deploy on Secube board**