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final

This instruction is designed to expose NVIDIA's final register combiner to assembly. Final combiner is always enabled. When it is not specified in shader explicitly, it defaults to *final 1-zero,r0,zero,zero,zero,zero,zero,r0*, which is setting shader's output color to the content of *r0* register. Final combiner is free on NVIDIA's hardware. Final combiner (other than the default one) may be quite expensive on ATI's hardware (up to four instruction slots).

```
final src0, src1, src2, src3, src4, src5, src6
```

Registers

Argument	Description	v _n	c _n	t _n	r _n	zero, fog	addr0v1	mulef
src0, src1, src2, src3	source register	X	х	X	x	X	X	X
src4, src5, src6	source register	X	X	X	X	X		

addr0vI is a special token, which can be used only as an argument in *final* instruction. It is equivalent to setting input to the clumped sum of r0 and vI, i.e. addr0v1.rgb = clamp(r0 + v1). Alpha component of addr0vI is zero.

mule f is a special token, which can be used only as an argument in final instruction. It is equivalent to setting input to the multiplication of arguments src4 and src5, i.e. mulef.rgb = src4 * src5. Alpha component of mule f is zero.

Remarks

All arguments modifiers except **invert** are prohibited. All arguments are clamped to the unit range. a selector is allowed on src0-src5 arguments. a and b selectors are allowed on src6.

This instruction sets shader's output color according to the following formula

```
output.rgb = src0 * src1 + (1-src0) * src2 + src3
output.a = src6
```

On NVIDIA's hardware fog blending has to be done in pixel shader. This is what final combiner is supposed to do, e.g. *glEnable(GL_FOG)* will not affect anything. Fog factor (which is in .a portion of *fog* register) is only available in *final* instruction.

ATI's hardware has fog blending, which occurs after pixel shader. It is controlled in normal way via *glEnable(GL_FOG)*.

Example

```
ps.1.2
def c0,1,1,0,0 // fog color
tex t0 // Load texture
tex t1 // Load texture
final v1.a,t0,c0,1-t1,zero,zero,c0
```