(OPEN BOOK TEST) 21st Nov2023

ISE-II of Sub–Operating System

2022-23 Sem- I

(Only book is allowed for reference.
Internet reference is not allowed.
Answer along with steps and justification is preferred only answer will be not be considered for evaluation) **Time 30 min**

1. Consider a simple system running a single process. The size of physical frames and logical pages is 16 bytes. The RAM can hold 3 physical frames. The virtual addresses of the process are 6 bits in size. The program generates the following 20 virtual address references as it runs on the CPU: 0, 1, 20, 2, 20, 21, 32, 31, 0, 60, 0, 0, 16, 1, 17, 18,32, 31, 0, 61. (Note: the 6-bit addresses are shown in decimal here.) Assume that the physical frames in RAM are initially empty and do not map to any logical page.**(4m)**

(a) Translate the virtual addresses above to logical page numbers referenced by the process. That is, write down the reference string of 10/20 page numbers corresponding to the virtual address accesses above. Assume pages are numbered starting from 0, 1, ...

(b) Calculate the number of page faults generated by the accesses above, assuming a FIFO page replacement algorithm. You must also correctly point out which page accesses in the reference string shown by you in part (a) are responsible for the page faults.

(c) Repeat (b) above for the LRU page replacement algorithm.

(d) What would be the lowest number of page faults achievable in this example, assuming an optimal page replacement algorithm were to be used? Repeat (b) above for the optimal algorithm.

2. Consider a system with several running processes. The system is running a modern OS that uses virtual addresses and demand paging. It has been empirically observed that the memory access times in the system under various conditions are: t1 when the logical memory address is found in TLB cache, t2 when the address is not in TLB but does not cause a page fault, and t3 when the address results in a page fault. This memory access time includes all overheads like page fault servicing and logical-to-physical address translation. It has been observed that, on an average, 10% of the logical address accesses result in a page fault. Further, of the remaining virtual address accesses, two-thirds of them can be translated using the TLB cache, while one-third require walking the page tables. Using the information provided above, calculate the average expected memory access time in the system in terms of t1,t2, and t3. **(1.5 m)**

3. The **page size in a system** (running a Linux-like operating system on x86 hardware) **is increased** while **keeping everything else** (including the total size of main memory) **the same**. For each of the following metrics below, indicate whether the metric is generally expected to increase, decrease, or not change as a result of this increase in page size. **(1.5 m)**

(a) Size of the page table of a process

(b) TLB hit rate

(c) Internal fragmentation of main memory

5. Consider a reference string: 4, 7, 6, 1, 7, 6, 1, 2, 7, 2. the number of frames in the memory is 3. Find out the number of page faults respective to: **(3m)**

1. Optimal Page Replacement Algorithm
2. FIFO Page Replacement Algorithm
3. LRU Page Replacement Algorithm