BK4829 Datasheet

DS-BK4829-E01 V1.0

2023/5/26

Contents

1. Overview

1.1 Features

- Worldwide band: 18 MHz ~ 580 MHz, 760 MHz ~ 1160 MHz
- 12.5/25/6.25/20 kHz channel spacing
- On-chip 7 dBm RF PA
- 3.0 V to 3.6 V power supply
- CTCSS tone receiver with tail CTCSS frequency detector
- 23/24 bit programmable DCS code
- Standard DTMF and programmable in-band dual tone
- SELCALL and programmable in-band single tone
- FSK data modem
- Frequency inversion scrambler
- Voice activated switch (VOX)
- RF signal strength measurement
- TX audio signal strength indication and RX audio signal strength indication
- Frequency scan function
- 3-wire interface with MCU with maximum 8 Mbps clock rate
- QFN32 package, 4 x 4 mm

1.2 Applications

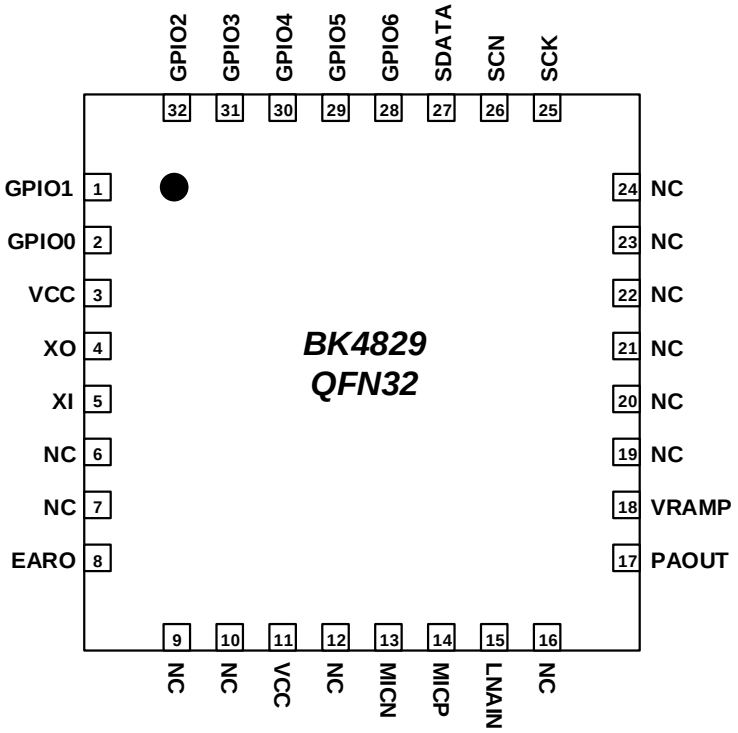
- Personal radio service
- Baby monitor
- Toys

1.3 General Description

The BK4829 is a half-duplex TDD FM transceiver operating within 18 MHz ~ 580 MHz, 760 MHz ~ 1160 MHz band range for worldwide personal radio. Besides speech communication, the BK4829 on-chip FSK data modem supports F2D and F1W emission to be used in both FRS and DPMR band for text message and GPS information exchange.

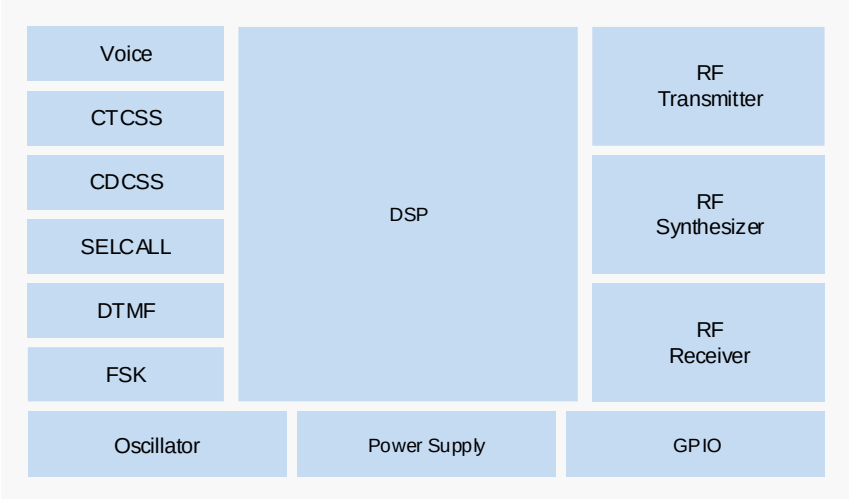
The BK4829 is a complete, small form factor solution optimized for low-power, low-cost, and highly integrated mobile and portable consumer electronic devices, requiring only a few external decoupling capacitors and an external inductor for input matching.

Figure 1-1 QFN32 Pin Assignments (Top View)



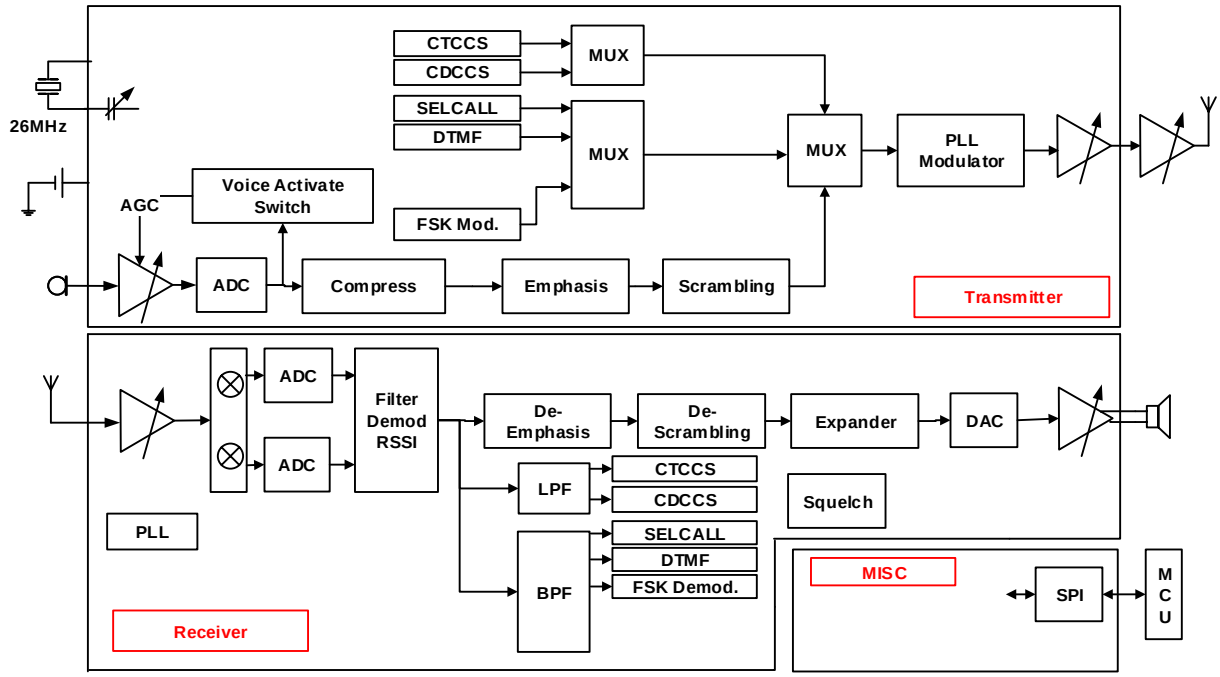
1.4 Block Diagram

Figure 1-2 General Block Diagram



2. Functional Description

Figure 2-1 Functional Block Diagram



2.1 Overview

The BK4829 integrates high performance PLL, ADC, DAC, and advanced digital signal processing capability on a single chip. The digital low-IF image rejection architecture enables it to work with a very simple MCU as a two-way radio communication system. On-chip flexible and precise, continuous and discrete tone generator and detector enable a secure link and digital signaling.

2.2 RF Transceiver

The BK4829 includes an integrated RF transceiver which is compliant with the specifications of most countries in the world. The RF transceiver requires the following external components to operate:

- A 26 MHz crystal;
- Simple input matching and output matching;
- Several SMD capacitors for decoupling and DC blocking.

2.3 FM Receiver

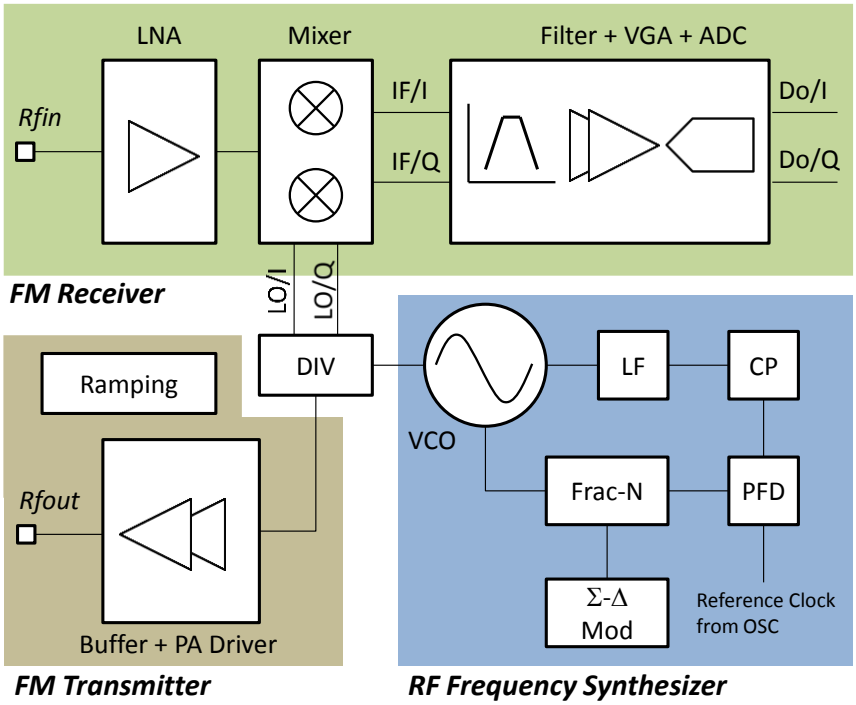
The receiver implements a low-IF image rejection architecture which is composed with two parts: RF front-end and IF part. The RF front-end comprises a LNA and a quadrature mixer. The IF part comprises a low-pass filter (LPF) for channel filtering, a variable gain amplifier (VGA) and a high precision analog-to-digital converter (ADC). The block diagram of the FM receiver is shown in Figure 2-2.

At the RF front-end part, the LNA is a differential low-noise amplifier with single-ended input. The LNA is followed by a quadrature mixer that down-converts the RF signal directly to IF signal. The low-IF image rejection architecture is implemented in order to eliminate the external SAW filters.

At the IF part, the down-converted in-phase IF signal (IF/I) and quadrature-phase IF signal(IF/Q) are first filtered by the BPF, and then amplified by the VGA. The Sigma-Delta ADC samples analog IF signal from VGA, and converts it to digital IF signal. Then the digital signal will be sent to DSP for second down-conversion and audio processing.

To avoid serious distortion with high-level input power, AGC function is added to automatically adjust the gain of LNA and the gain of VGA.

Figure 2-2 Radio Block Diagram



2.4 FM Transmitter

The transmitter is a single-ended amplifier including a buffer and a PA driver. The block diagram of the transmitter is shown in Figure 2-2. Because FM modulation is of constant envelope, the amplifier works in saturated mode to save current consumption.

The output power of FM transmitter can be programmed from -5 dBm to +8 dBm through a 3-wire SPI interface.

2.5 RF Frequency Synthesizer

An RF synthesizer is implemented to generate local oscillator (LO) signals. It includes a voltage controlled oscillator (VCO), a fractional-N divider (frac-N), a phase-frequency detector (PFD), a charge pump (CP) and a loop filter (LF). The RF synthesizer is shared for RX mode and TX mode. The block diagram of the synthesizer is shown in Figure 2-2.

In RX mode, the RF frequency synthesizer generates unmodulated LO signals. And the unmodulated LO signal is then divided by an integer Ndiv for down-conversion mixer in the FM receiver. In TX mode, FM modulation is realized in the RF frequency synthesizer.

In RX mode, the locked frequency of the synthesizer is equal to Ndiv x (fwanted - fIF). While in TX mode, the locked frequency of the synthesizer is equal to Ndiv x fwanted.

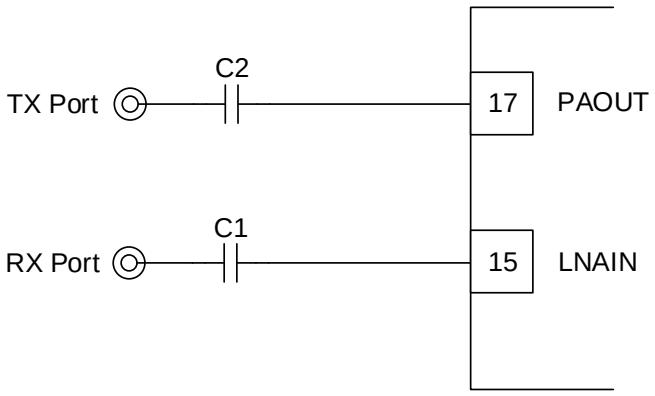
Channel selection is also implemented by programming the value of fractional-N through a 3-wire SPI interface. On power up or channel reselection, the synthesizer takes less than 0.3 ms to settle.

For BK4829, the default crystal is 26 MHz. The frequency tolerance of the crystal should be within ±2.5 ppm to keep a reliable communication.

2.6 Input/Output Matching

Since the LNA input and the PA output are of single-ended, an external balun is not necessary. Both the input matching and the output matching can be implemented using low-cost discrete inductors and capacitors. The schematic of input/output matching is shown in Figure 2-3.

Figure 2-3 Schematic of Input/Output Matching



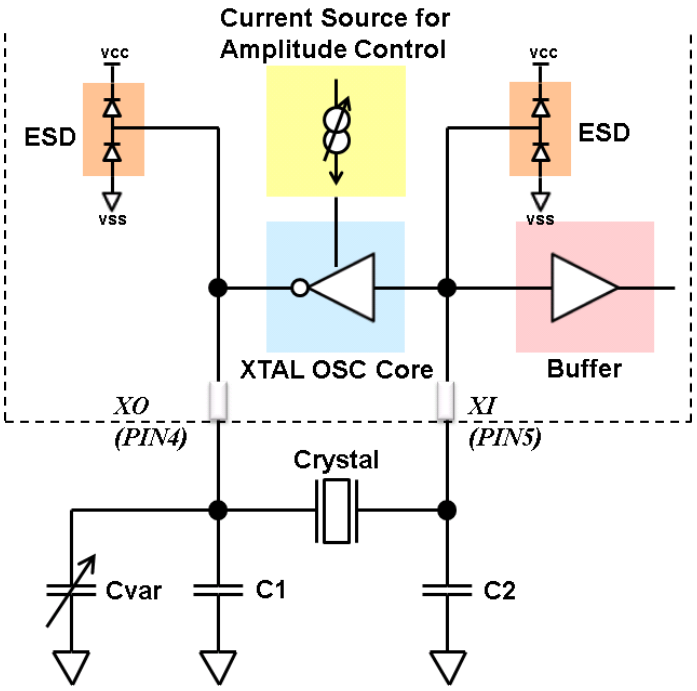
As for input matching, capacitor C1 is used for DC-blocking. The recommended value of C1 is 100 pF. As for output matching, capacitor C2 is used for DC-blocking, too.

2.7 Crystal Oscillator

The BK4829 integrates a low-power amplitude-regulated 26 MHz crystal oscillator. The 26 MHz crystal oscillator not only provides the reference frequency for the RF synthesizer, but also provides clock for digital part. The circuit diagram of the 26 MHz crystal oscillator is shown in Figure 2-4.

The 26 MHz crystal oscillator is designed for use with a quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal datasheet. Figure 2-4 shows how the crystal is connected to the 26 MHz crystal oscillator. C1 and C2 are ceramic SMD (Surface Mount Device) capacitors connected between each crystal terminal and ground. Cvar is an adjustable capacitor for frequency calibration.

Figure 2-4 Circuit Diagram of 26 MHz Crystal Oscillator



$$C_{load} = \frac{C_1^{'} \times C_2^{'}}{C_1^{'} + C_2^{'}}$$

$$C_1^{'} = C_1 + C_{var} + C_{par}$$

$$C_2^{'} = C_2 + C_{par}$$

in which, Cpar is parasitic capacitance including PCB trace capacitance and pin input capacitance. The value of Cpar is about 1 pF.

2.8 Power Supply Decoupling

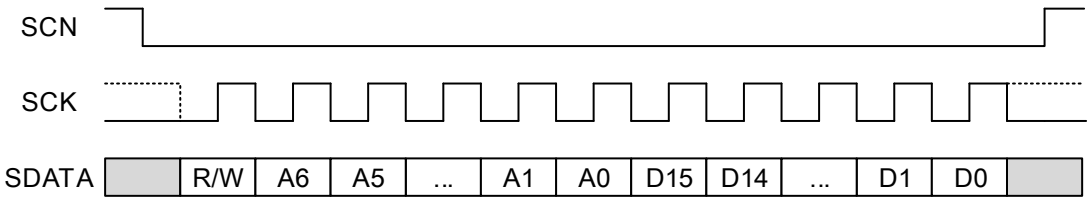
Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application.

2.9 SPI Interface

The BK4829 has a 3-wire SPI interface. These 3 wires are SCK (PIN25), SCN (PIN26), SDATA (PIN27) for data exchange. SCK and SCN are input pins, while SDATA is a bi-direction pin.

The BK4829 always latches data at the SCK rising edge and outputs its data at SCK falling edge.

Figure 2-5 Three-Wire Interface Timing



3. Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-0.3	-	+3.6	V
I/O pin voltage	V_{IO}	-0.3	-	V_{DD}+0.3	V
Storage temperature	T_{STR}	-40	25	105	℃

3.2 Recommended Operating Conditions

All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.0	-	3.6	V
Operating temperature [a]	T_{OPR}	-40	25	105	℃

a. The range of operating temperature mainly depends on the specification of the crystal. The frequency tolerance of the crystal should be within ±2.5 ppm during all operating conditions.

3.3 Current Consumption

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply current (RX mode)	I_{RX}	RX on	-	49	-	mA
Supply current (TX mode)	I_{TX}	TX on	-	43	-	mA
Power down current	I_{PD}	Sleep	-	30	-	μA

3.4 Receiver Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating frequency	F_{OP}	-	760	-	1160	MHz
		-	18	-	580	MHz
Sensitivity	RXSENS	a, d, e	-124	-123	-	dBm
Adjacent channel selectivity	ACS	b, d	66	67	68	dB
Blocking	BLK	c, d	85	87	88	dB
Inter-modulation	IMD	d	65.5	66	66	dB
Audio						
Earpiece output level	EARO	e	-	146	-	mVrms
SINAD	ASNR	e, f	53	53	53	dB
Amplitude response	ARES	-	-3	-	3	dB
Audio noise floor	ANF	-	-	81	-	dBm
CTCSS						
CTCSS sensitivity	CTSEN	-	-	-123	-	dBm
CTCSS response time	CTRES	-	75	-	125	ms
Frequency range	SAF	-	62.5	-	250.3	Hz
DCS						
CDCSS sensitivity	CDSEN	-	-	-123	-	dBm
CDCSS response time	CDRES	-	-	171	-	ms
Code length	CLEN	-	23	-	24	Bit
Bit rate	BRATE	-	-	134.4	-	Hz
SELCALL						
SELCALL sensitivity	SELSEN	-	-	-123	-	dBm
SELCALL response time	SELRES	-	-	30	-	ms
Frequency range	IBSF	-	400	-	3000	Hz
DTMF						
DTMF sensitivity	DTSEN	-	-	-123	-	dBm

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DTMF response time	DTRES	-	-	20	-	ms
High band frequency range	FH	-	1209	-	1633	Hz
Low band frequency range	FL	-	697	-	941	Hz
MIC input impedance	Zin	-	-	25	-	K

Test condition:

a. 12 dB SINAD
b. 1st adjacent channel (±12.5 kHz)
c. Frequency offset > 1 MHz
d. According to ETSI standard (EN 300 296-1 V1.4.1)
e. 1 kHz tone, 1.5 kHz deviation
f. -50 dBm input power

3.5 Transmitter Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating frequency	F_{OP}	-	760	-	1160	MHz
		-	18	-	580	MHz
Output power	POUT	a	-5	-	8	dBm
Adjacent channel power rejection	ACPR 1st	-	-	68	69	dBc
Alternate channel power rejection	ACPR 2nd	-	-	74	75	dBc
Microphone sensitivity	MICSENS	b	-	11	-	mV
SINAD	TSINAD	c	-	49	-	dB

Test condition:

a. Depend on output matching and register settings
b. 1.5 kHz deviation
c. At sensitivity level

3.6 SPI Control Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK Frequency	f_{SCK}	0	-	8	MHz
SCK High Time	t_{HIGH}	25	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK Low Time	t_{LOW}	25	-	-	ns
SDATA Input, SCN to SCK↑ Setup	t_S	20	-	-	ns
SDATA Input to SCK↑ Hold	t_{HSDATA}	10	-	-	ns
SCN Input to SCK↓ Hold	t_{HSCN}	10	-	-	ns
SCK↓ to SDATA Output Valid	t_{CDV}	2	-	25	ns
SCK↓ to next SCK↑ after Address In	t_{NXT}	1	-	-	μs
SCK, SCN, SDATA, Rise/Fall Time	t_R, t_F	-	-	10	ns

Figure 3-1 3-Wire Control Interface Write Timing Diagram

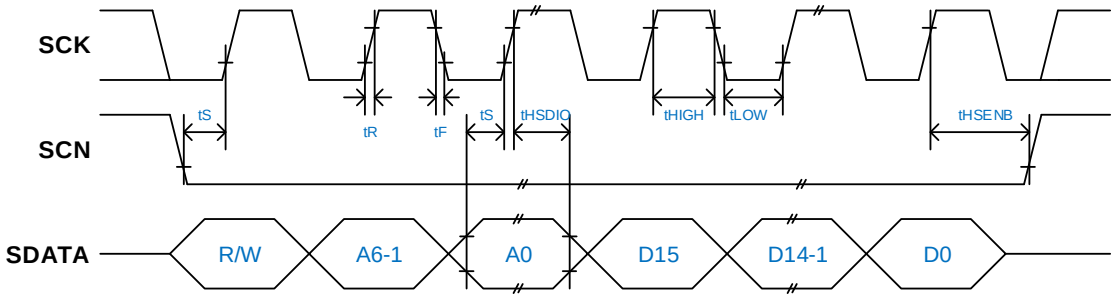
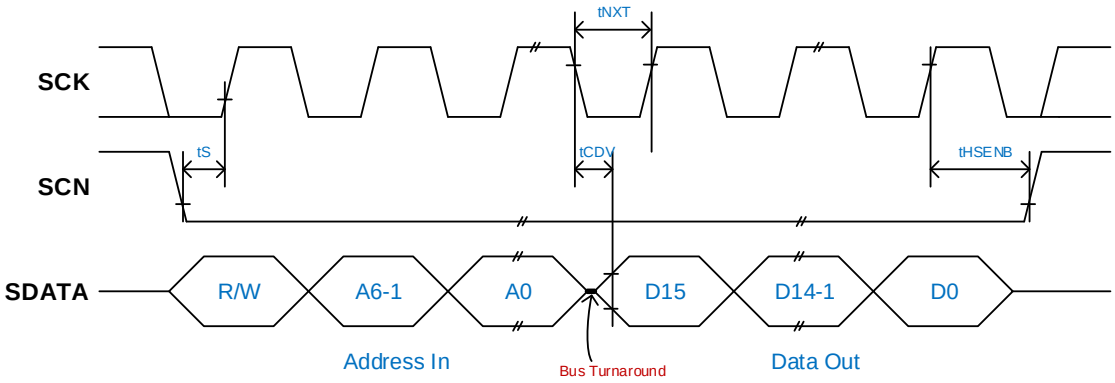


Figure 3-2 3-Wire Control Interface Read Timing



4. Pin Description

The BK4829 is offered in a 4 x 4 mm, 32-pin QFN package. Figure 4-1 shows the pin assignments of the QFN32 package.

Figure 4-1 QFN32 Pin Assignments (Top View)

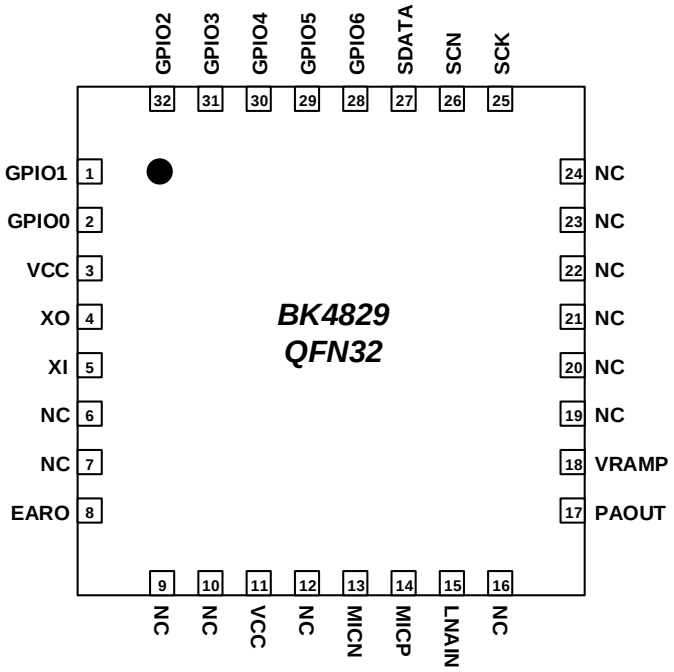


Table 4-1 shows the pin descriptions of the QFN32 package.

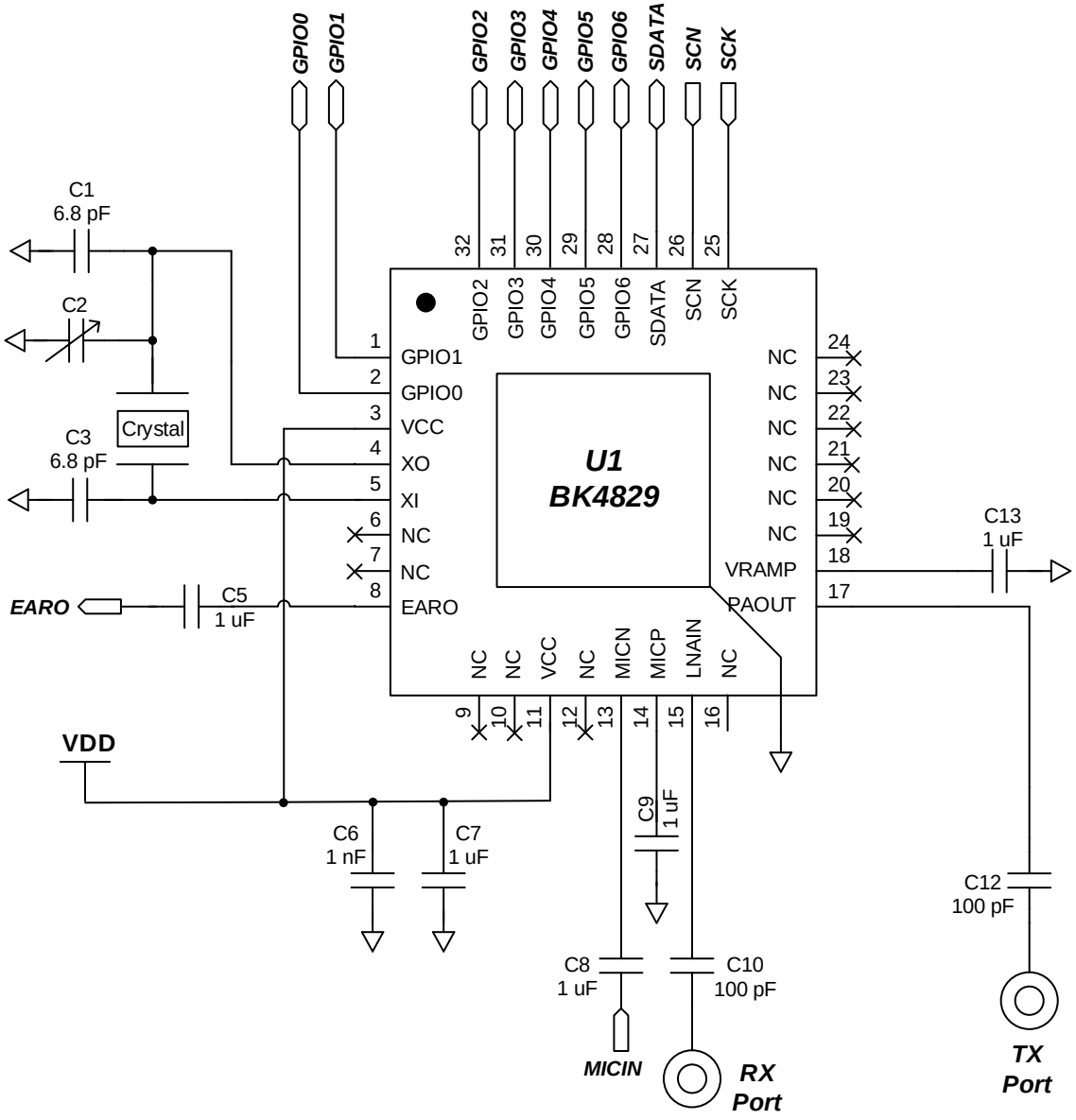
Table 4-1 QFN32 Pin Descriptions

Pin #	Name	I/O	Description
1	GPIO1	I/O	General purpose input/output - there is internal pull-down on this port.
2	GPIO0	I/O	General purpose input/output - there is internal pull-down on this port.
3	VCC	Input	Digital Power supply, 3.0 V to 3.6 V
4	XO	Output	Crystal oscillator port, output
5	XI	Input	Crystal oscillator port, input
6	NC	-	-
7	NC	-	-
8	EARO	Output	Earpiece output
9	NC	-	-

Pin #	Name	I/O	Description
10	NC	-	-
11	VCC	Input	Analog Power supply, 3.0 V to 3.6 V
12	NC	-	-
13	MICN	Input	Microphone input, negative
14	MICP	Input	Microphone output, positive
15	LNAIN	Input	Input of low noise amplifier
16	NC	-	-
17	PAOUT	Output	Output of power amplifier
18	VRAMP	Output	Programmable PA Bias output, 0 V to 3.2 V
19	NC	-	-
20	NC	-	-
21	NC	-	-
22	NC	-	-
23	NC	-	-
24	NC	-	-
25	SCK	Input	SPI clock
26	SCN	Input	SPI enable
27	SDATA	I/O	SPI data
28	GPIO6	I/O	General purpose input/output - there is internal pull-down on this port.
29	GPIO5	I/O	General purpose input/output - there is internal pull-down on this port.
30	GPIO4	I/O	General purpose input/output - there is internal pull-down on this port.
31	GPIO3	I/O	General purpose input/output - there is internal pull-down on this port.
32	GPIO2	I/O	General purpose input/output - there is internal pull-down on this port.

5. Typical Application Schematic

Figure 5-1 BK4829 Schematic



6. Package Information

Figure 6-1 QFN32 4 x 4 mm Package Outline

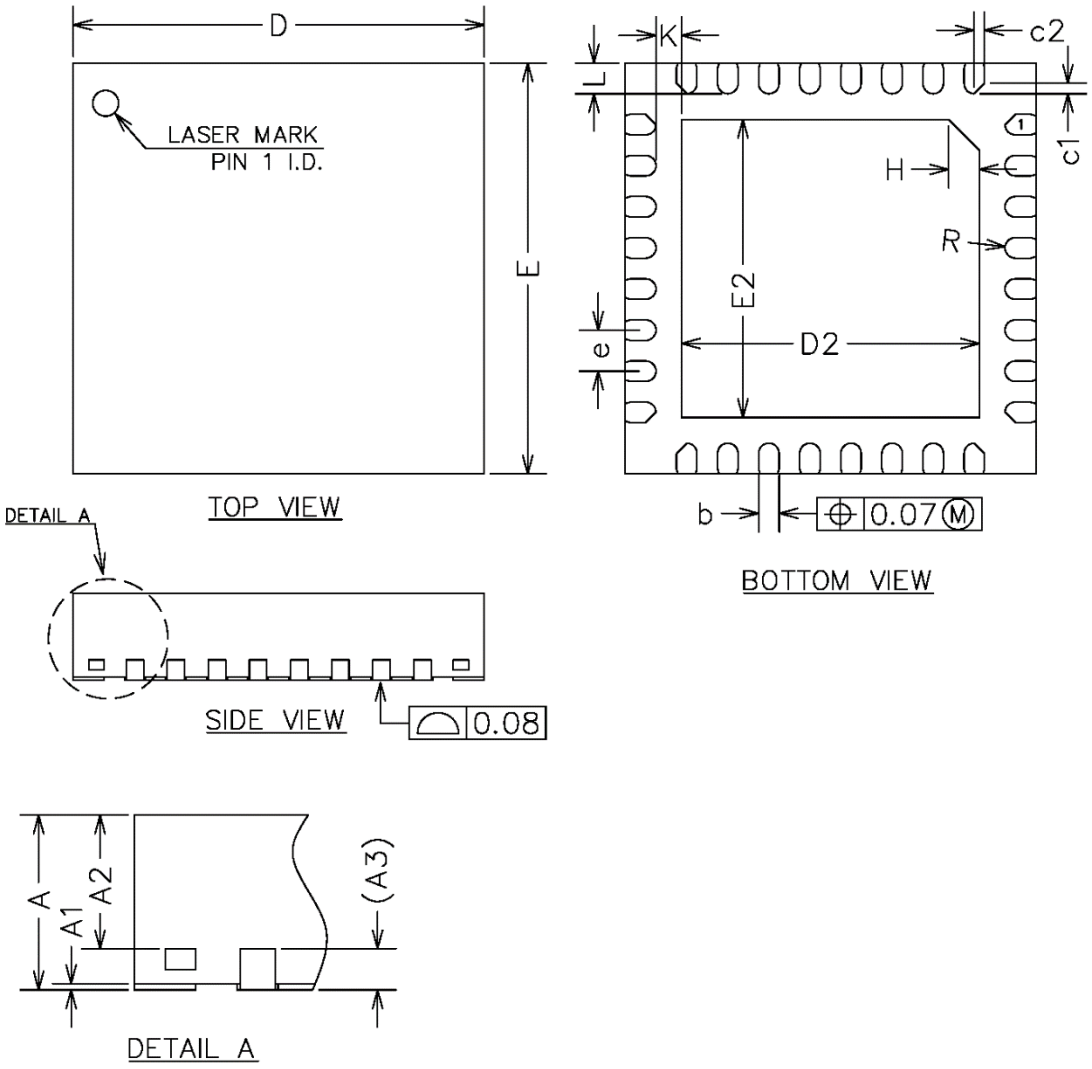


Table 6-1 QFN32 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A3	0.20 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30 REF		
K	0.25 REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

Table 6-2 Soldering Layer Content

Content	Width	Unit
Ni	0.5 - 2.0	μm
Pd	0.02 - 0.15	μm
Au	0.003 - 0.015	μm

Storage Caution

1. Calculated shelf life in vacuum sealed bag: 12 months at <40°C and 90% relative humidity (RH).
2. Peak package body temperature: 260 °C.
3. After vacuum sealed bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within 168 hours of factory conditions <40°C/60% RH, or
   b) Stored at 10% RH.

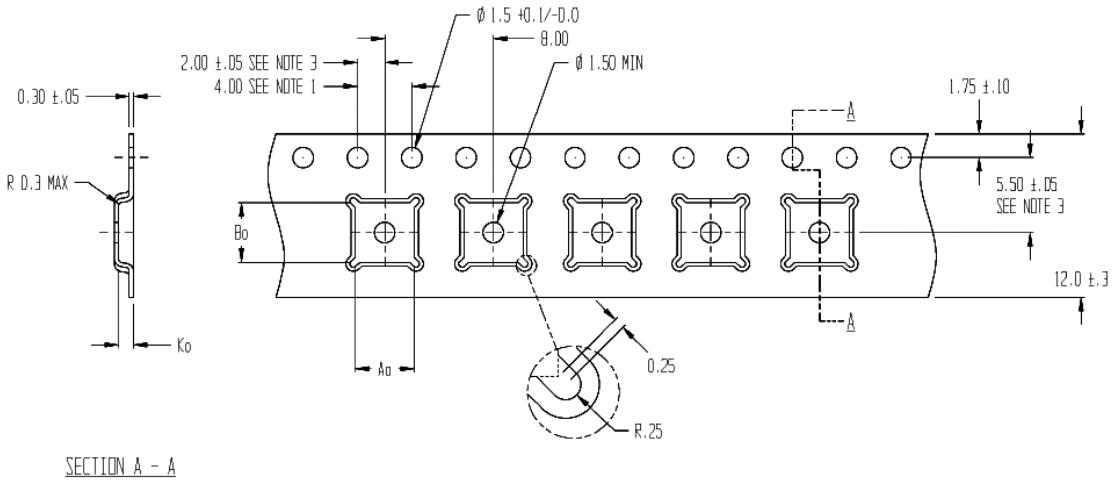
7. Tape and Reel Information

All dimensions are in millimeters by default.

7.1 Tape Information

The figure below shows the dimensions of the tape for the BK4829 QFN package.

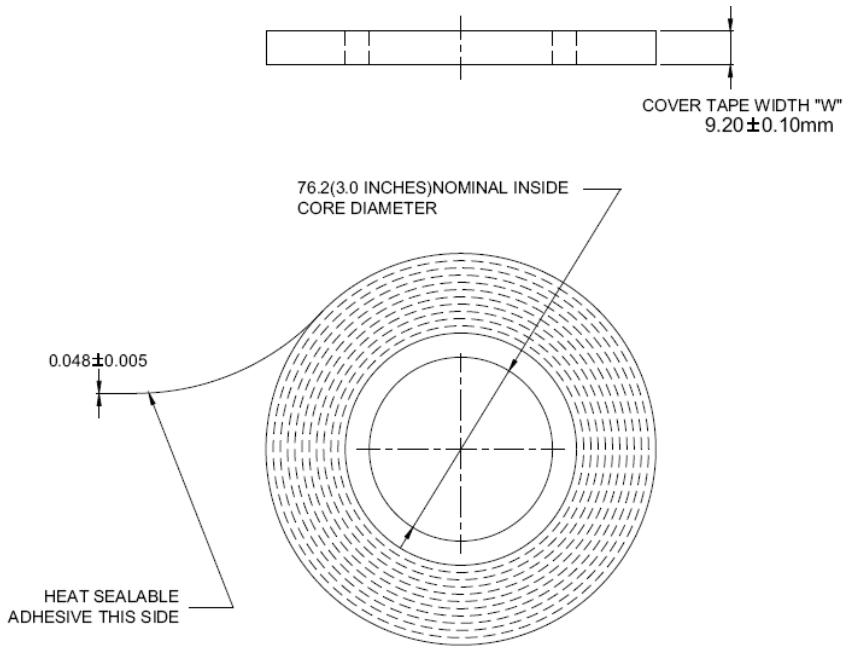
Figure 7-1 Tape Dimensions



A_0	B_0	K_0	Unit	Notes
4.35	4.35	1.1	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2. 2. Camber in compliance with EIA 481. 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

7.2 Cover Information

Figure 7-2 Cover Dimensions

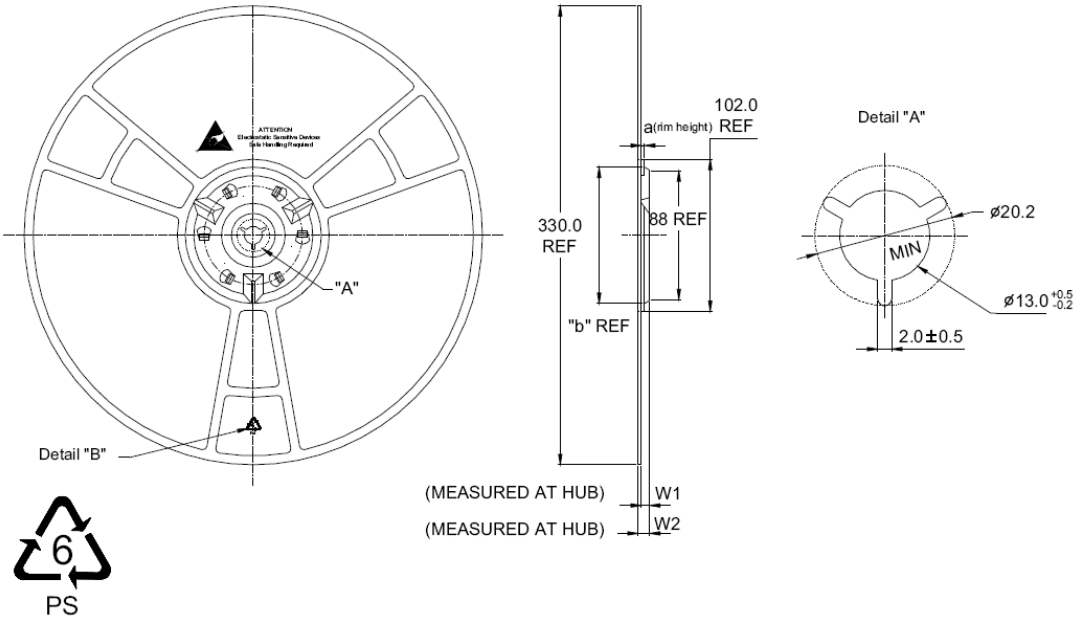


Note:

1. Reel to contain 300 meters of splice free material.
2. Material: Polyester film with antistatic coating and adhesive coating.
3. Color: Transparent, natural

7.3 Reel Information

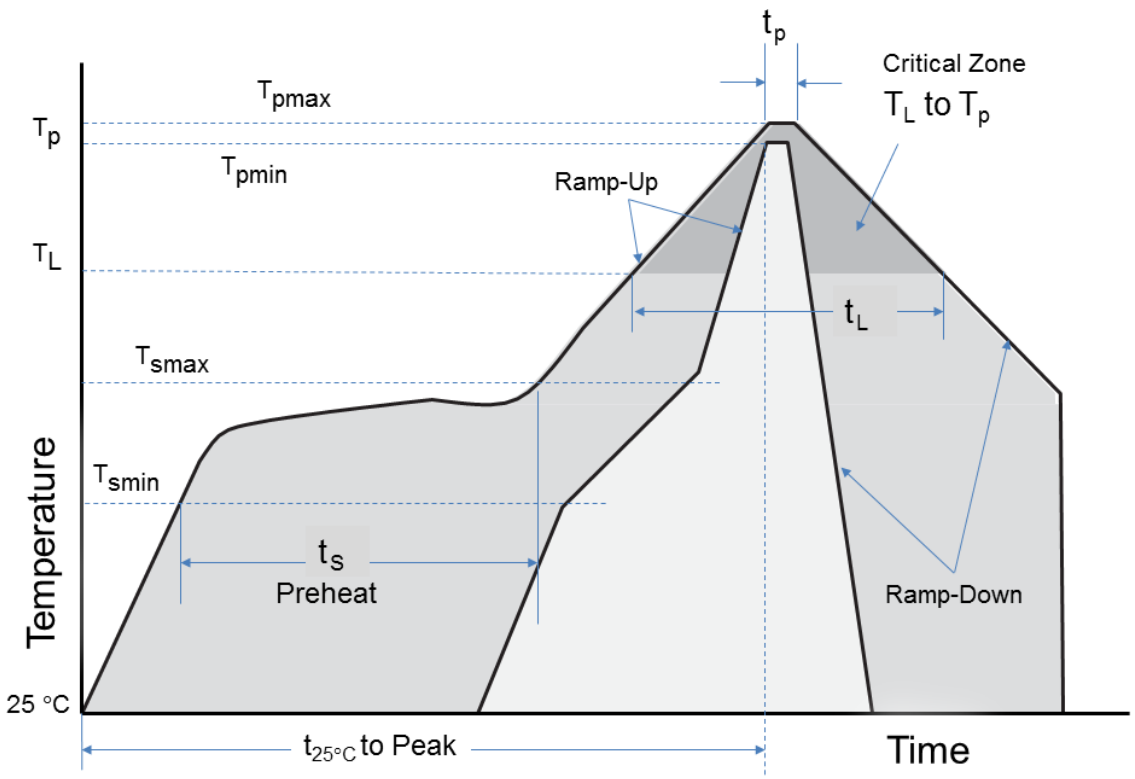
Figure 7-3 Reel Dimensions



Nominal Hub Width	W1 +0.6 mm -0.4 mm	W2 MAX	a	b	Unit
12	12.8	18.2	1.5	96.5	mm

8. Reflow Soldering Profile

Figure 8-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 ℃/second max.
Preheat	Temperature min. (T_{smin})	150 ℃
	Temperature max. (T_{smax})	200 ℃
	Time (t_s)	60 - 180 seconds
Time maintained above	Temperature (T_L)	217 ℃
	Time (t_L)	60 - 150 seconds
Peak/classification temperature (T_p)		260 ℃
Time within 5 ℃ of actual peak temperature (t_p)		20 - 40 seconds
Ramp-down rate		6 ℃/second max.

Profile Feature	Specification
Time 25 ℃ to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC (RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

9. Ordering Information

Table 9-1 Ordering Information

Part Number	Package	Operating Temp	Packing	Minimum Ordering Qty (MOQ)
BK4829QN32A	4 mm x 4 mm QFN32	-40 to +105 ℃	Tape and Reel	3000

Revision History

Version	Date	Description
1.0	2023/5/26	Initial release.

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