



DRS. KIRAN & PALLAVI PATEL GLOBAL UNIVERSITY

Established Under Gujarat Private Universities (Amendment) Act, 2021 (Gujarat Act No. 15 of 2021)

KPGU
Vadodara

FACULTY OF ENGINEERING & TECHNOLOGY

KRISHNA SCHOOL OF EMERGING TECHNOLOGY

&

APPLIED RESEARCH

(KSET)

FINAL DRAFT

OF

DETAILED SCHEME

&

SYLLABUS OF SEMESTER 3 / YEAR 2

B. TECH. COMPUTER SCIENCE & ENGINEERING

DURATION: 4 YEARS (8 SEMESTERS)

MONTH: JULY

YEAR: 2022

Year : 2 Semester : 3																		
Sr No.	Name of Subject	Teaching Scheme				Evaluation Scheme											Credits	
		The or y H ou rs /w ee k	Tu to ria l H ou rs/ we ek	Pr ac tic al H ou rs/ we ek	To tal	Theory					Practical				To tal Ma rks	The or y	P r a c ti c a l	
						E x	Internal				Internal			E xt er n al				
							Continuous Evaluation				Term Work							V iv a/ P r a c t ic al E x a m
							E S S	A tt e n d a n c e	A ss ig n m e n t	M i d S e m - I	M i d S e m - II	A t t e n d a n c e	L a b w o r k					
1	Data Structures	3	0	0	3	70	5	5	10	10	-	-	-	-	-	100	3	0
2	Data Structures Laboratory	0	0	4	4	-	-	-	-	-	5	5	5	5	30	50	0	2
3	Database Management Systems	3	0	0	3	70	5	5	10	10	-	-	-	-	-	100	3	0

HoD

Director

Dean

DRS. KIRAN & PALLAVI PATEL GLOBAL UNIVERSITY, VADODARA (KPGU)

4	Database Management Systems Laboratory	0	0	4	4	-	-	-	-	-	5	5	5	5	30	50	0	2
5	Digital Electronics	3	0	0	3	70	5	5	10	10	-	-	-	-	-	100	3	0
6	Digital Electronics Laboratory	0	0	2	2	-	-	-	-	-	5	5	5	5	30	50	0	1
7	Maths-III	3	0	0	3	70	5	5	10	10	-	-	-	-	-	100	3	0
8	Maths-III Laboratory	0	0	2	2	-	-	-	-	-	5	5	5	5	30	50	0	1
9	Language Elective-2	3	0	0	3	70	5	5	10	10	-	-	-	-	-	100	3	0

Program Education Objectives (PEOs):

PEO1	To build a strong foundation for problem solving ability, critical thinking and mathematical principles in the domain of computer Science and emerging Technologies.
PEO2	To adapt innovative teaching methodology to elevate research and technical skills with advancements in computing tools and technologies and provide sustainable solutions to the social, economical and industrial problems.
PEO3	To produce competent computer professionals with various skills to formulate, analyze and design diverse problems and address challenges by developing software solutions.
PEO4	To exhibit lifelong learning skills, professional skills, leadership qualities, entrepreneurship and ethical values for global enrichment.
PEO5	Integrate computer science with AI, IoT, healthcare, finance, robotics, and smart technologies to create innovative solutions for real-world challenges.

Program Specific Outcomes (PSOs):

PSO1	Applying core mathematical concepts of computer Science and Engineering to solve complex problems by dividing it into smaller problems.
PSO2	To develop the research skill and ability to analyze the feasible solution in context with software development and management using modern tools and technologies.

HoD

Director

Dean

Program Outcomes (POs):

PO1	Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

Course Title	Digital Electronics		Cour se No (Will be assigned)							
Specialization			Structure							
Course/Branch	CSE			L	T	P	C			
Offered for	3 rd Sem			3	0	0	3			
Faculty	E & T		Status	B S C	H SC	ES C	P C C	Prof . Electi ve	Ope n Electi ve	Mino r(Ho ns)
Pre requisite	Y	N		-	-		-	-	-	-
	-	-		Project/		Seminar		Internship		Mandatory
				-	-	-	-			
For Office Use Only										
Date of Submission			Type	Ne w	Modification			Merging		
To take effect from										

HoD

Director

Dean

Date of approval by Board of Study		Date of approval by Academic Council	
---	--	---	--

Sr No	Name of Course	Teaching Scheme				Evaluation Scheme											Credits	
		T he o r y H o u r s/ w e e k	Tu tor ial H o u r s / w e e k	Pr act ica l H o u r s / w e e k	To tal	Theory					Practical				T o t al M ar ks	T he o r y	Pr ac tic al	
						Ex	Internal				Internal			Ex te rn al				
Continuous Evaluation					Term Work				Vi va / Pr ac tic al Ex a m									
E S S	A t t e n d a n c e	A s s i g n m e n t	-I M i d S e m	-II M i d S e m	A t t e n d a n c e	L a b w o r k	W r i t i n g R e p o r t	P e r f o r m a n c e										
1	Digital Electronics	3	0	0	3	70	5	5	10	10	-	-	-	-	-	100	3	-

Dean

Course Outcomes:	
C01	Solve the given problem using fundamentals of Number systems and Boolean algebra.
C02	Understand simplification of Boolean function and its conversion in different forms.
C03	Understand, analyze and design various Combinational circuits.
C04	Compare different flip-flop characteristics and FF Design, understand and analyze various sequential circuits.
C05	Demonstrate the process of Analog to Digital conversion and Digital to Analog conversion, understand various memory organization and TTL logic.

Content of the Course		
Module	Contents/Topics to be covered	H o u r s
Module 1	Number Systems and Logic Gates Digital computer and digital systems fundamentals AND, OR, NOT, NAND, NOR and Exclusive-OR operations, Boolean algebra, examples of IC gates, number systems-binary, signed binary, octal hexadecimal number, binary arithmetic, complements arithmetic, error detecting and correcting codes	06
Module 2	Boolean Function Simplification 2,3,4,5 variable K-map representation and simplification of logic functions using K-map, SOP and POS minimization of logical functions. Don't care conditions, VEM kmap, NAND or NOR implementation	05
Module 3	Combinational Logic Multiplexer, De-Multiplexer/Decoders, Adders, Subtractors, BCD arithmetic, carry look ahead adder, serial adder, parity checker/generator, code converters, priority encoders, decoders/drivers for display devices, Q-M method of function realization	06

Module 4	Sequential Logic: Introduction, RS,JK,D,T Flip-Flops, Triggering of Flip-Flops, Flip-Flop Excitation Tables, Analysis of Clocked Sequential Circuits, State Reduction and Assignment Design Procedure, Design of Counters, Design with State Equations	06
Module 5	Registers, Counters and the Memory unit Shift registers, applications of shift registers, serial to parallel converter, parallel to serial converter Ripple Counters, Synchronous Counters, Timing Sequences, Memory Unit, Johnson counter	08
Module 6	A/D and D/A conversion : A/D and D/A Converters Digital to analog converters: weighted resistor/converter, R-2R Ladder D/A converter, specifications for D/A converters, parallel comparator A/D converter, successive approximation A/D converter, counting A/D converter, dual slope A/D converter, A/D converter using voltage to frequency and voltage to time conversion, specifications of A/D converters	05
Module 7	Memory and PLDs : ALU, Digital logic families, TTL, Schottky TTL and CMOS logic, interfacing CMOS and TTL, Tri-state logic.read only memory (ROM), read and write memory(RAM), content addressable memory (CAM), charge de coupled device memory (CCD), commonly used memory chips, ROM as a PLD, Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).	05

Textbooks	
1	"Digital logic and Computer design", M. M. Mano, Pearson Education India, 2016.
2	"Fundamentals of Digital Circuits", A. Kumar, Prentice Hall India, 2016
3	"Digital Principles and Applications" Malvino & Leach, McGraw-Hill Education
References	
1	"Modern Digital Electronics", R. P. Jain, McGraw Hill Education, 2009.
Web content Link/E-material links	
1	https://nptel.ac.in/courses/108105113

DRS. KIRAN & PALLAVI PATEL GLOBAL UNIVERSITY, VADODARA (KPGU)

Course Title	Digital Electronics Laboratory		Cour se No <i>(Will be assigned)</i>							
Specialization			Structure							
Cours e/Bra nch	CSE			L	T	P	C			
Offered for	3 rd Sem			0	0	2	1			
Faculty	E & T		Status	B S C	H SC	ES C	P C C	Prof . Electi ve	Ope n Electi ve	Mino r(Ho ns)
Pre requisite	Y	N		-	-		-	-	-	-
	-	-		Project/		Seminar		Internship		Mandatory
				-	-	-	-			
For Office Use Only										
Date of Submissi on			Type	Ne w	Modification			Merging		
To take effect from										

HoD

Director

Dean

DRS. KIRAN & PALLAVI PATEL GLOBAL UNIVERSITY, VADODARA (KPGU)

Date of approval by Board of Study		Date of approval by Academic Council	
---	--	---	--

Sr No	Name of Course	Teaching Scheme				Evaluation Scheme										Credits			
		The or y H ou rs/ w ee k	Tu tor ial Ho urs /we ek	Pr act ica l Ho urs /we ek	To tal	Theory					Practical				T ot al M ar ks	T he or y	Pr ac tic al		
						Ex	Internal				Internal			Ex te rn al					
							Continuous Evaluation					Term Work						Vi va / Pr ac tic al Ex a m	
							E S S	A tt e n d a n c e	A s s i g n m e n t	-I M id S e m	-II M id S e m	A tt e n d a n c e	L a b w o r k						W rit in g R e p o r t
1	Digital Electronics Laboratory	0	0	2	2	-	-	-	-	-	5	5	5	5	30	50	-	1	

HoD

Director

Dean

Course Outcomes:	
C01	Solve the given problem using fundamentals of Number systems and Boolean algebra.
C02	Understand simplification of Boolean function and its conversion in different forms.
C03	Understand, analyze and design various Combinational circuits.
C04	Compare different flip-flop characteristics and FF Design, understand and analyze various sequential circuits.
C05	Demonstrate the process of Analog to Digital conversion and Digital to Analog conversion, understand various memory organization and TTL logic.

List of Experiment

Name of Laboratory: Digital Electronics Laboratory				
List of practical/Experiments				
Sr No	Objective	Performance	Study	Self-Study
1	Getting familiar with various digital integrated circuits of different logic families. Study of data sheet of these logic Families	-	Yes	-
2	To study the implementation of AND, OR and NOT gates using NAND and NOR gate.	Yes		-
3	To Simplify and Implement given Boolean function using logic gates.	Yes	Yes	-
4	To study and verify Code Conversion circuits Binary to Gray code Gray to Binary code BCD to XS-3 code	Yes	Yes	-

5	To study Half adder, Full adder, 2bit parallel adder and Half Subtractor circuit and verify its truth table.	Yes	Yes	-
6	To study different Flip Flops and verify its truth table	Yes	Yes	-
7	To study 4 to 1 line Multiplexer and 1 to 4 line Demultiplexer and verify its truth table.	Yes	Yes	-
8	To study 8 to 3 line Encoder and 3 to 8 line Decoder and verify its truth table.	Yes	Yes	-
9	To study 4 bit Ripple Up/Down Counter.	Yes	Yes	-
10	To study Serial In-Parallel Out 4bits Shift Register.	Yes	Yes	-
11	Study and configuration of A to D and D to A converter.	Yes	Yes	-