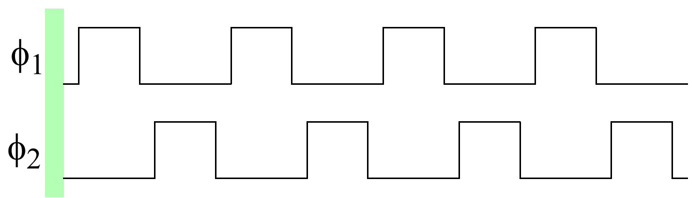
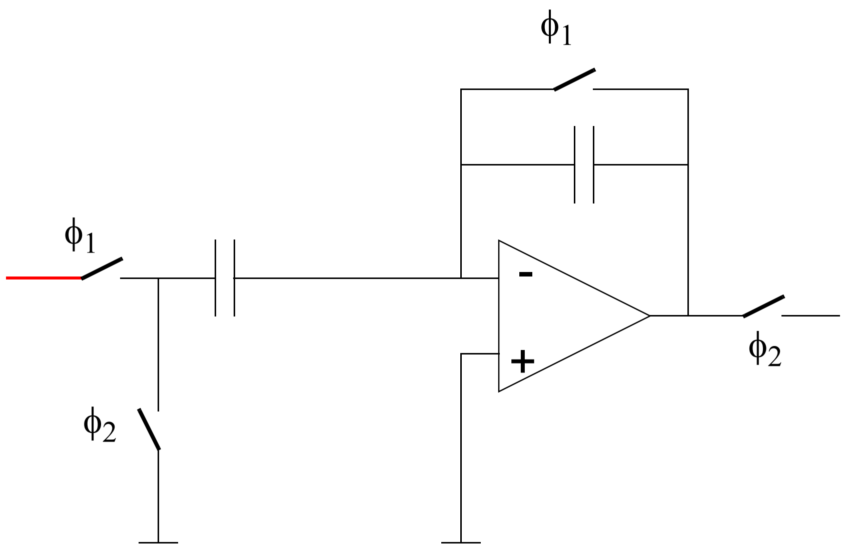
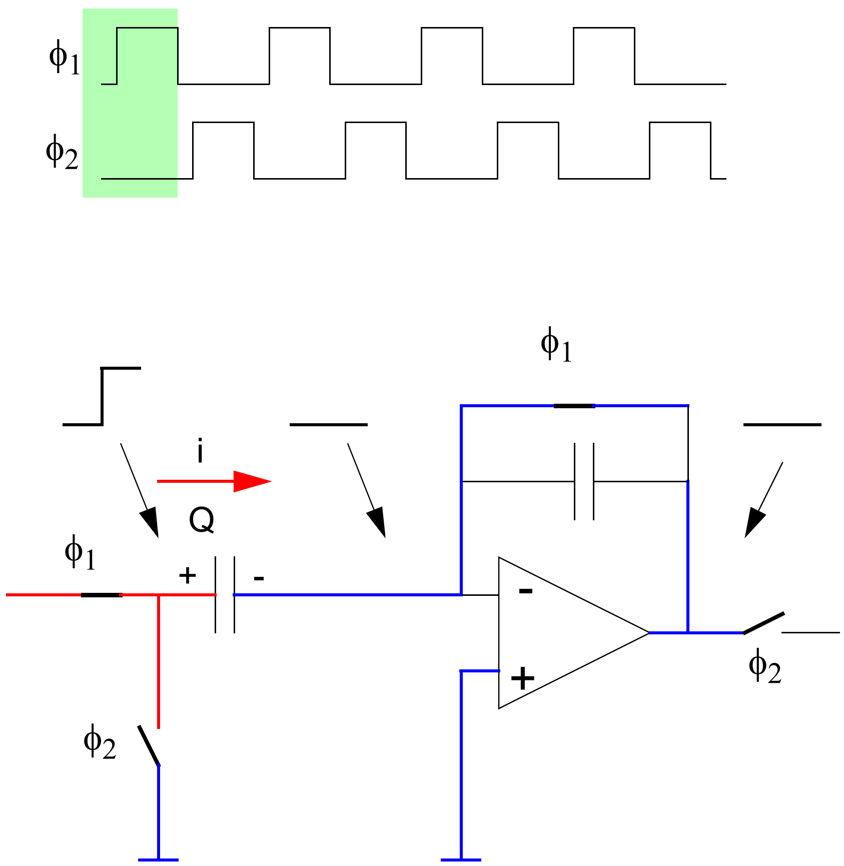
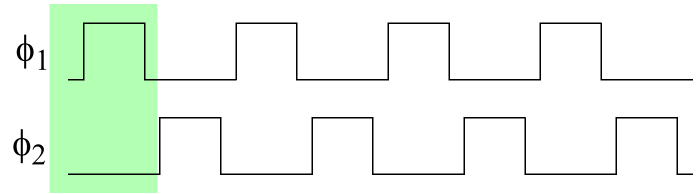
SWITCHED CAPACITOR AMPLIFIERS


ϕ_1
ϕ_2

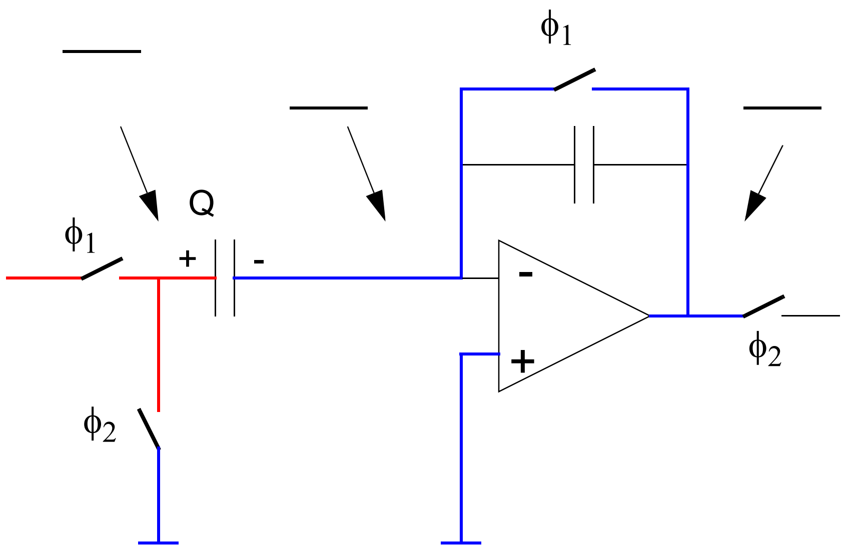

ϕ_1
ϕ_1
-
+
ϕ_2
ϕ_2



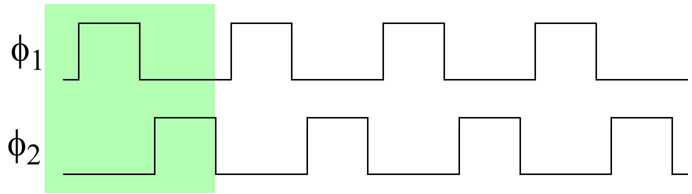
φ1
φ2
φ1
i
Q
φ1
+
-
-
+
φ2
φ2



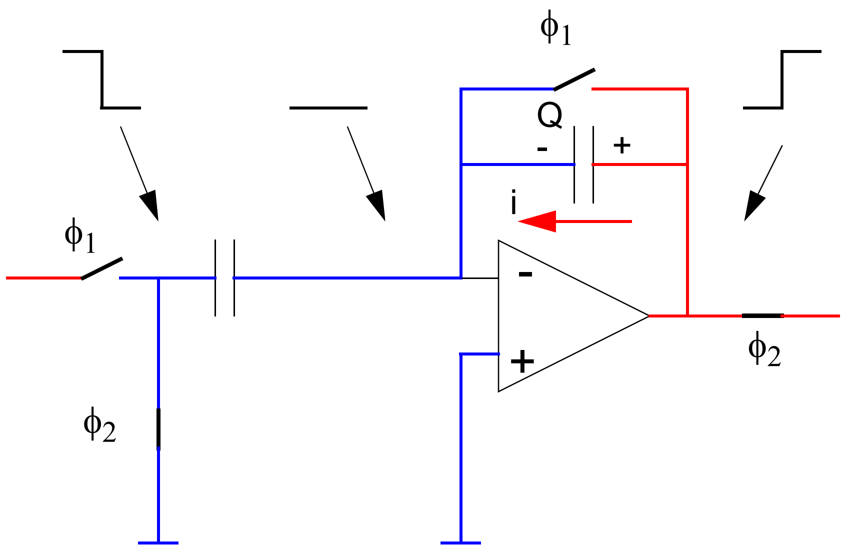
ϕ_1
ϕ_2



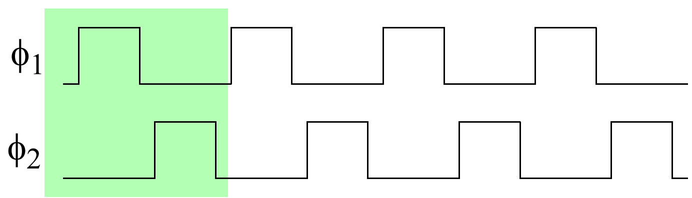
ϕ_1
Q
+
-
ϕ_1
-
+
ϕ_2
ϕ_2



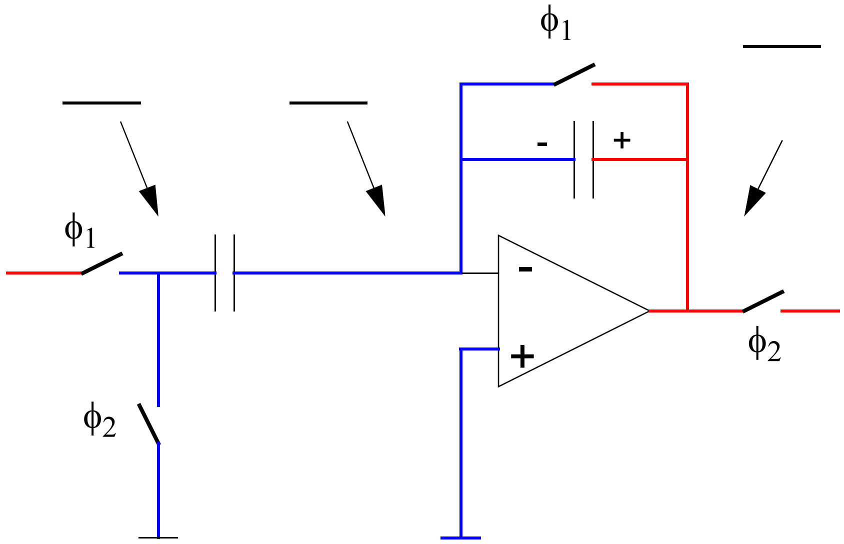
ϕ_1
ϕ_2



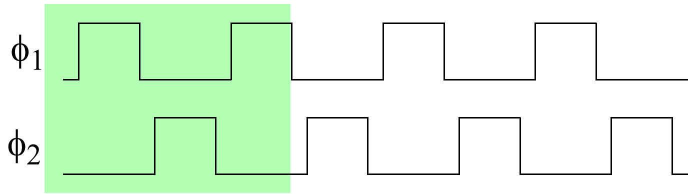
ϕ_1
Q
-
+
i
ϕ_1
-
+
ϕ_2
ϕ_2



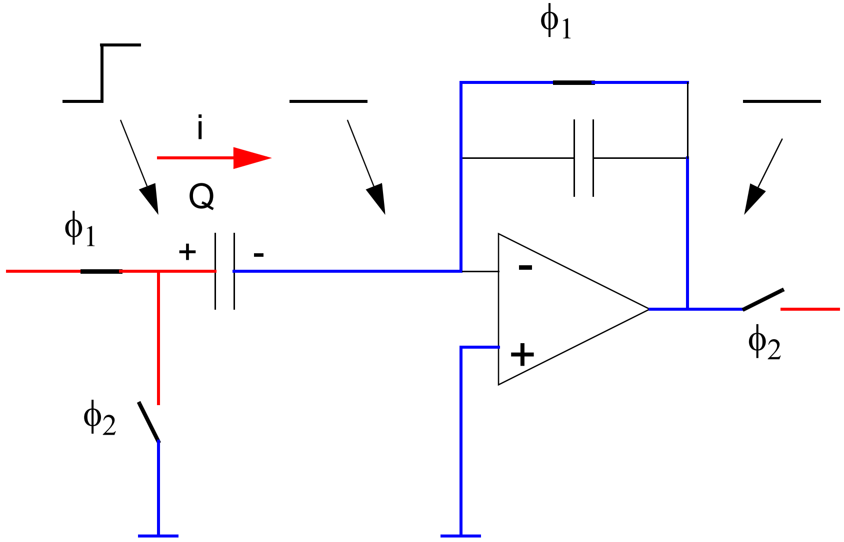
ϕ_1
ϕ_2



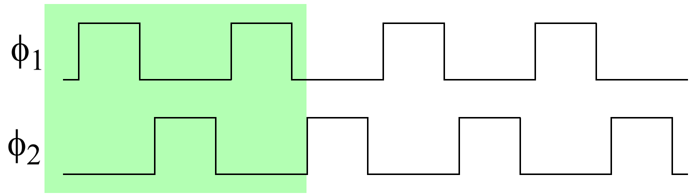
ϕ_1
ϕ_1
ϕ_2
ϕ_2
-
+
-
+



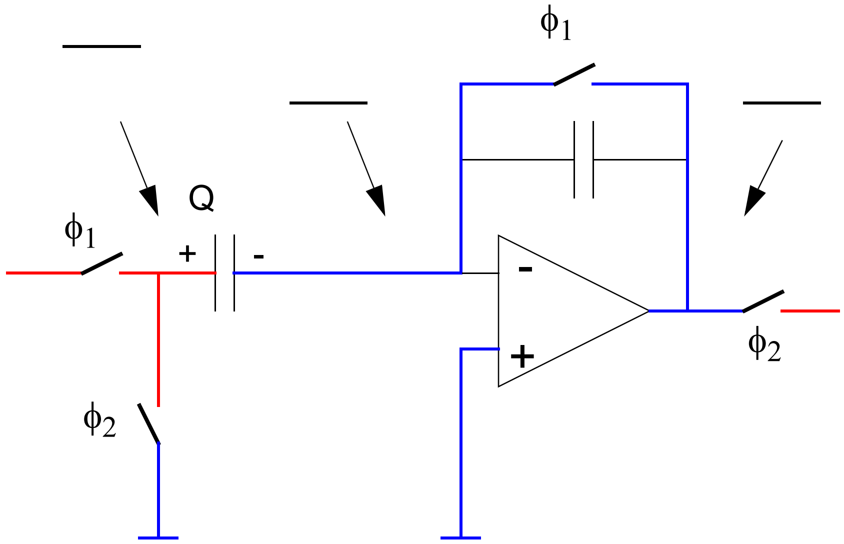
ϕ_1
ϕ_2



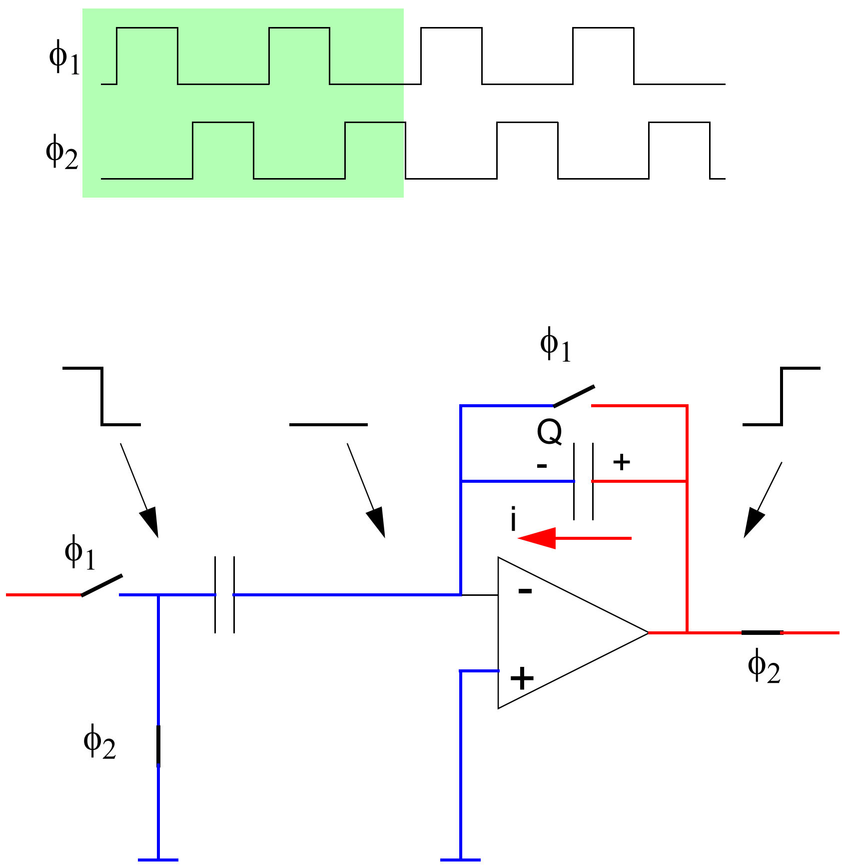
ϕ_1
i
Q
ϕ_1
+
-
-
+
ϕ_2
ϕ_2



ϕ_1
ϕ_2



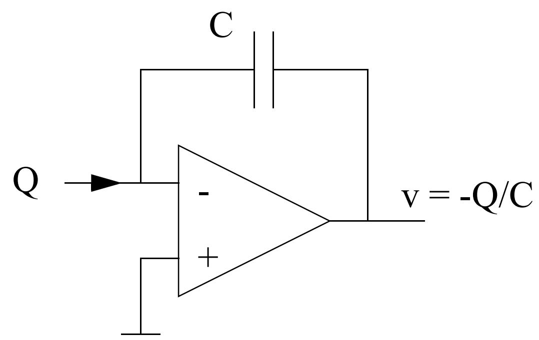
ϕ_1
Q
+
-
ϕ_1
-
+
ϕ_2
ϕ_2



ϕ_1
ϕ_2
ϕ_1
Q
-
+
i
ϕ_1
-
+
ϕ_2
ϕ_2

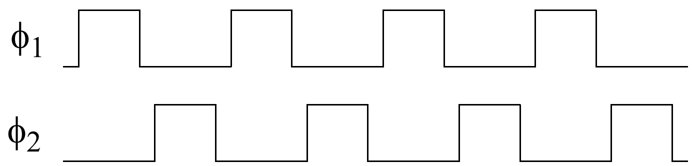
Simple amplifier

First approach: A_0 = infinite.



ϕ_1: $V_{C_1} = V_s - V_x \qquad V_{C_F} = 0 \qquad V_{out} = V_x$

ϕ_2:



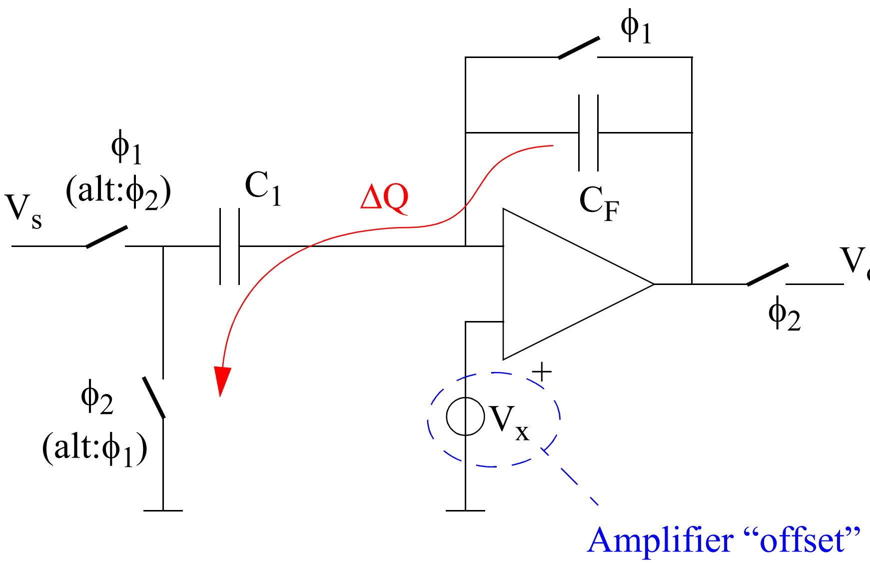
$$V_{C_1} = V_s + \Delta V_s - V_x = -V_x \qquad \text{because} \qquad \Delta V_s = -V_s$$

$$V_{C_F} = -\frac{\Delta Q_1}{C_F} = -\frac{[-V_x - (V_s - V_x)]C_1}{C_F} = \frac{V_s C_1}{C_F}$$

$$V_{out} = V_x + V_{C_F} = V_s \frac{C_1}{C_F} + V_x$$

Alternatively:

ϕ_1: $V_{C_1} = -V_x \qquad V_{C_F} = 0 \qquad V_{out} = V_x$



ϕ_2:

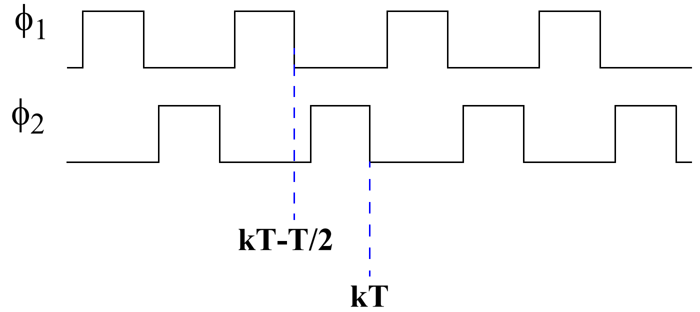
$$V_{C_1} = V_s - V_x$$

$$V_{C_F} = -\frac{\Delta Q_1}{C_F} = -\frac{[V_s - V_x - (-V_x)]C_1}{C_F}$$

$$V_{out} = -V_s \frac{C_1}{C_F} + V_x$$

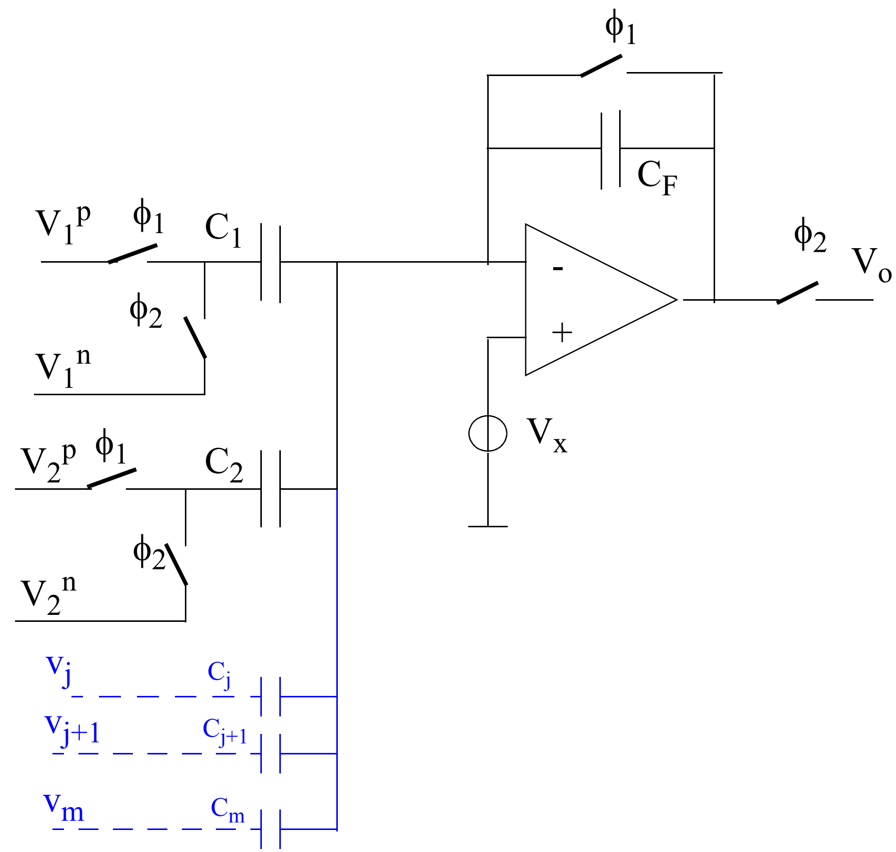
Summing amplifier (ideal):

$$V_{out} = [V_1^p(\phi_1) - V_1^n(\phi_2)]\frac{C_1}{C_F} + [V_2^p\phi_1 - V_2^n\phi_2]\frac{C_2}{C_F} + V_x$$



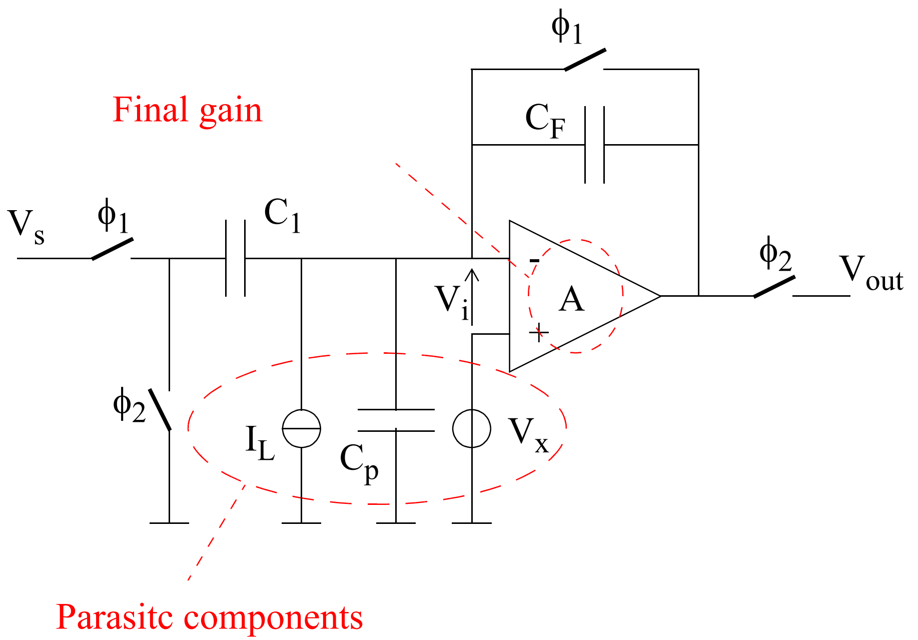
Generally:

$$V_{out}(kT) = V_x + \sum_{j=1}^{m}\frac{C_j}{C_F}\left[V_j^p\left(kT - \frac{T}{2}\right) - V_j^n(kT)\right] \quad \textbf{(4.1)}$$



Effect of Parasitics

- Final amplifier open loop gain (DC)
- Input offset
- Leak current from sampling capacitors.
- Parasitic capacitance (conductors)



The result is found by applying
the super position method
on the output signal.

That is the sum of all effects.

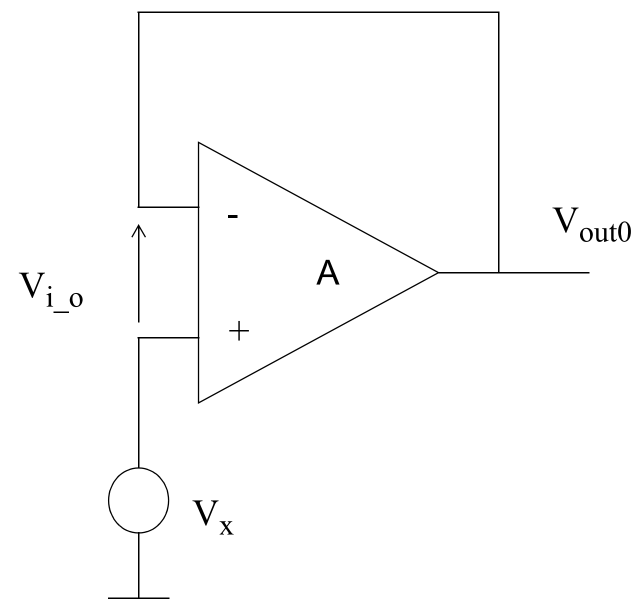
Output signal as a consequence of offset and final gain.

Open loop gain: A

$$V_{out0} = (V_x - V_{out0})A$$

$$(A+1)V_{out0} = V_x A$$

$$V_{out0} = \frac{A}{1+A}V_x = \varepsilon_0 V_x \qquad \textbf{(4.2)}$$

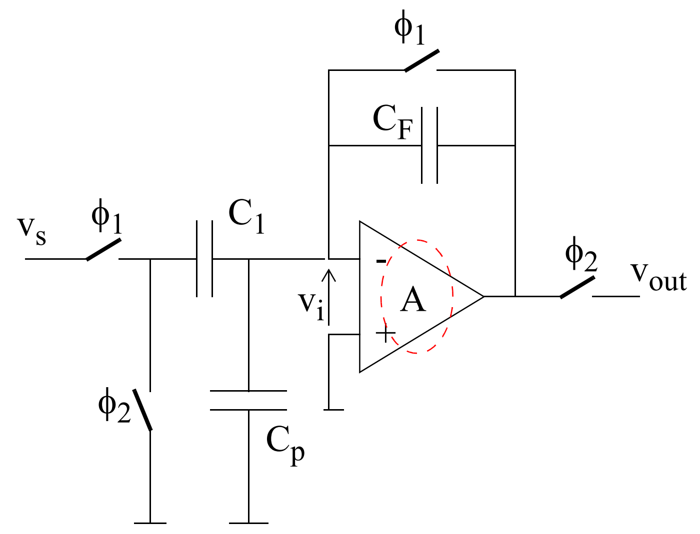


Output signal as a consequence of final gain and parasitic capacitance.

$$V_{out} = -V_i A \qquad \Delta V_s = -v_s$$

ϕ_1:

$$V_{C_1} = V_s - V_i = V_s - V_x \frac{A}{1+A} \qquad V_{C_F} = 0 \qquad V_{out} = V_x \frac{A}{1+A}$$



ϕ_2 (incremental voltage changes):

$$v_i = -v_s \frac{C_1}{C_1 + C_p + C_F} + v_{out} \frac{C_F}{C_1 + C_p + C_F}$$

$$v_{out} = -v_i A = v_s A \frac{C_1}{C_1 + C_p + C_F} - v_{out} A \frac{C_F}{C_1 + C_p + C_F}$$

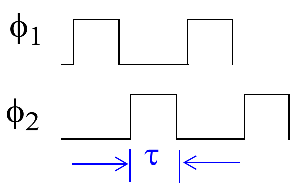
$$v_{out}\left[1 + A\frac{C_F}{C_1 + C_p + C_F}\right] = A v_s \frac{C_1}{C_1 + C_p + C_F}$$

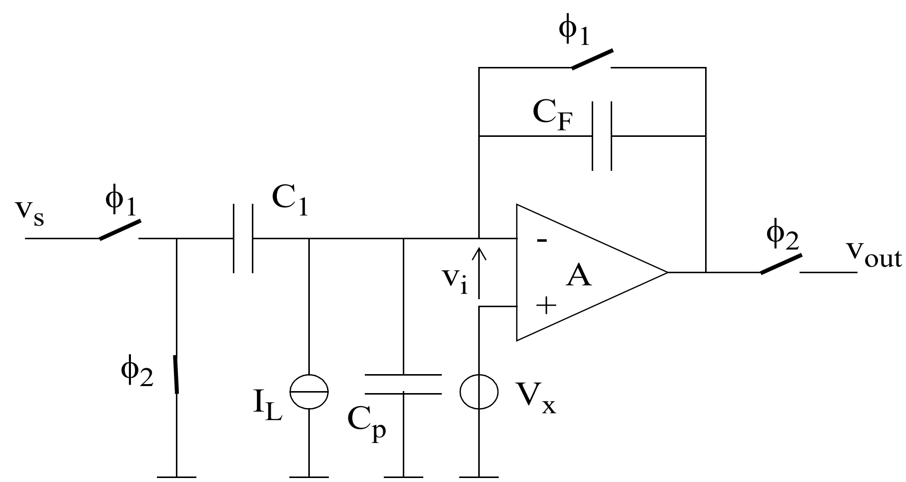
$$v_{out} = \frac{A v_s \frac{C_1}{C_1 + C_p + C_F}}{1 + A\frac{C_F}{C_1 + C_p + C_F}} = \frac{A v_s C_1}{C_1 + C_p + C_F + A C_F}$$

$$v_{out} = \frac{C_1}{C_F} \frac{A}{1 + (C_1 + C_p)/C_F + A} v_s = \frac{C_1}{C_F} \frac{1}{1 + \varepsilon_A^1} v_s \qquad \varepsilon_A^1 = \frac{1}{A} \frac{(C_p + C_F + C_1)}{C_F} \qquad \textbf{(4.3)}$$

Output signal as a consequence of leak current I_L in the pulse period τ.

$$v_{outL} = \frac{C_1 + C_p}{C_F} \frac{1}{1 + \varepsilon_A^1} \frac{I_L \tau}{C_1 + C_p} = \frac{I_L \tau}{C_F(1 + \varepsilon_A^1)} = \frac{I_L \tau A}{C_1 + C_p + C_F(1 + A)} \qquad \textbf{(4.4)}$$





Final result

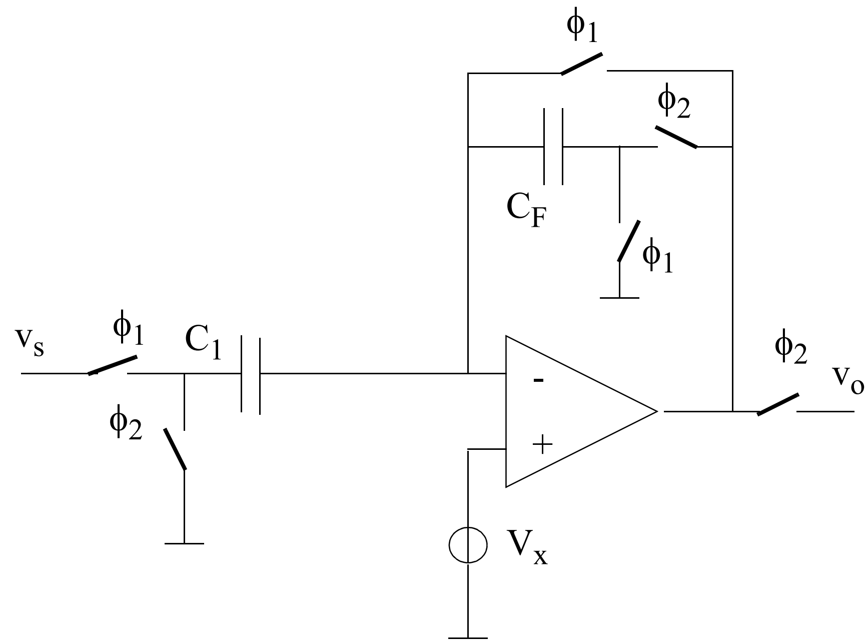
Summing (4.2), (4.3) and (4.4):

$$v_{out} = \frac{C_1}{C_F}\frac{1}{1+\varepsilon_A}v_s + \frac{I_L\tau}{C_F(1+\varepsilon_A^1)} + \frac{AV_x}{1+A} \tag{4.5}$$

Offset Compensation

ϕ_1: V_x is sampled, C_F is charged to V_x

ϕ_2: When $Q=\Delta V_s C_1$ is transferred to C_F, V_x is already across C_F with the negative charge at the amplifier output (when V_x er positive)



ϕ_1:

$$V_{C_1} = V_s - V_x \qquad V_{C_F} = V_x \qquad V_{out} = V_x$$

ϕ_2:

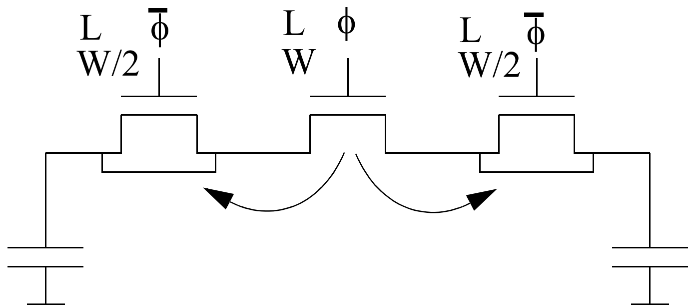
$$V_{C_1} = (V_s - V_x) + \Delta V_s = -V_x$$

$$\Delta V_{C_F} = -\frac{\Delta Q_1}{C_F} - V_x = -\frac{[-V_x - (V_s - V_x)]C_1}{C_F} - V_x$$

$$V_{out} = V_x + V_s \frac{C_1}{C_F} - V_x = V_s \frac{C_1}{C_F}$$

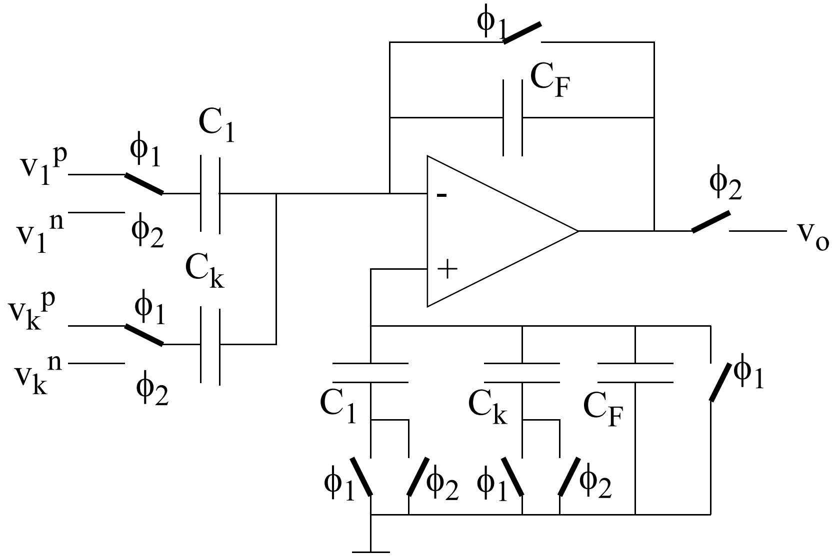
Compensation of charge injection:

Add dummy switches that are clocked in anti phase with the real switches.



Compensation of charge injection and clock feed through:

Introduce corresponding switches and capacitance on both amplifier's input terminals.



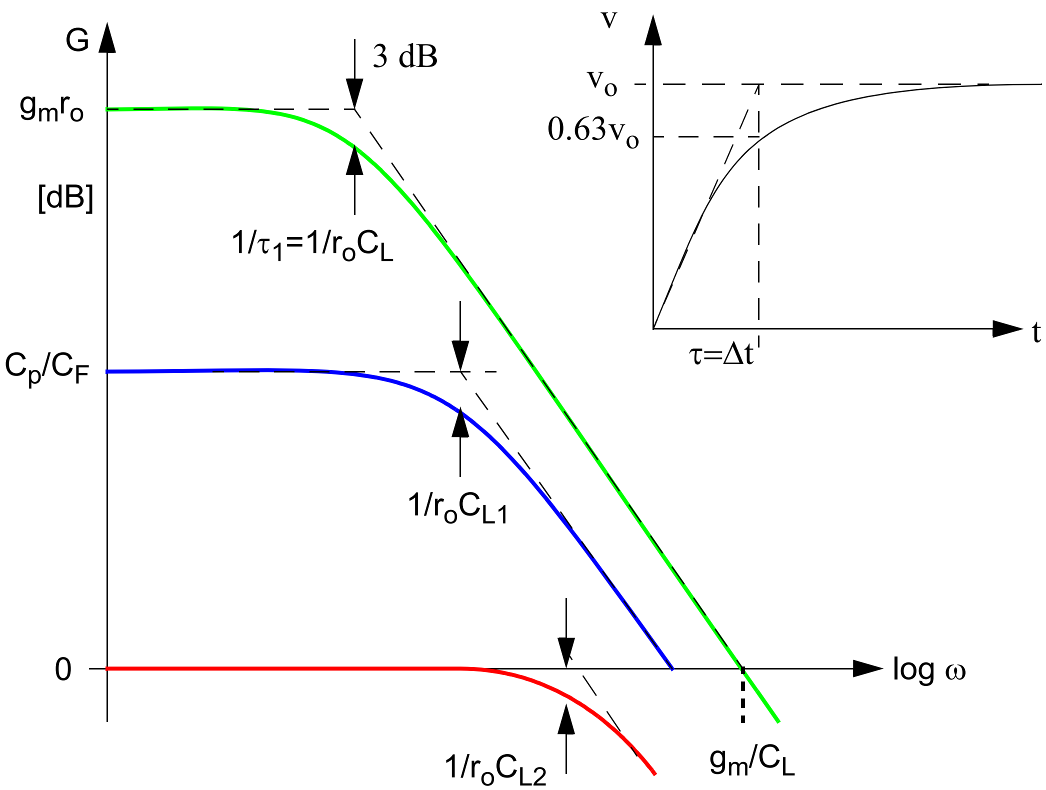
Dynamical Properties of SC Amplifiers

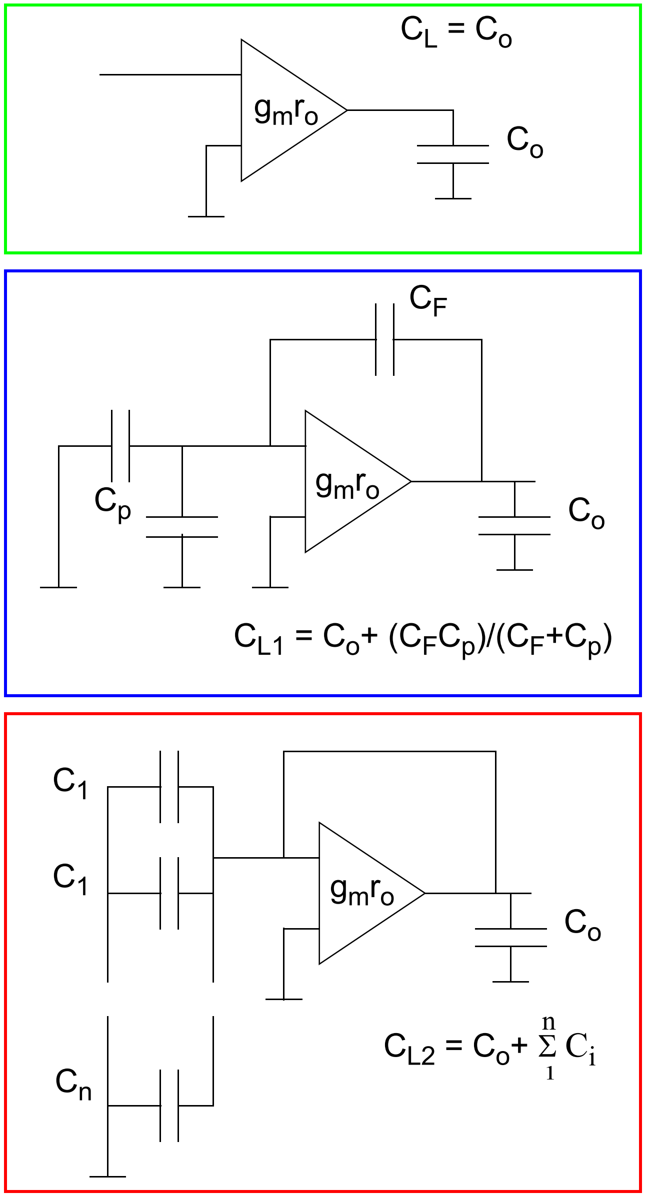
g_m: Amplifier transconductance, determined by the transconductance of the input transistors.

r_o: Amplifier output resistance

C_L: Load capacitance of the configuration.

C_p: Parallel capacitance of the input node

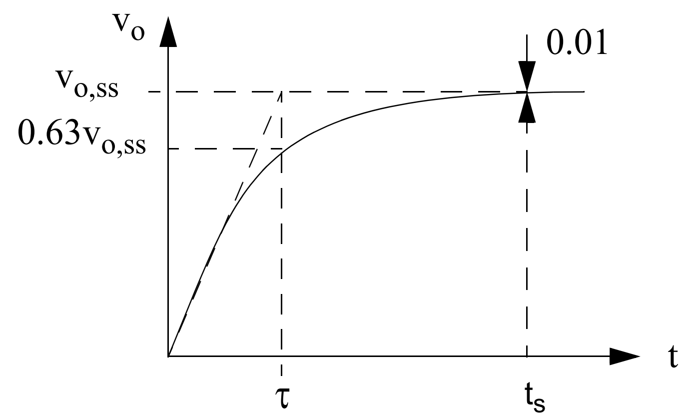




Requirements on the time constant:

$$v_o = v_{o,ss}(1 - e^{-t/\tau})$$

$$\left.\frac{dv_o}{dt}\right|_{t=0} = \left. v_{o,ss}\frac{1}{\tau}e^{-t/\tau}\right|_{t=0} = \frac{v_{o,ss}}{\tau}$$



Settling to 1% of $v_{o,ss}$ set the following requirement to t_s:

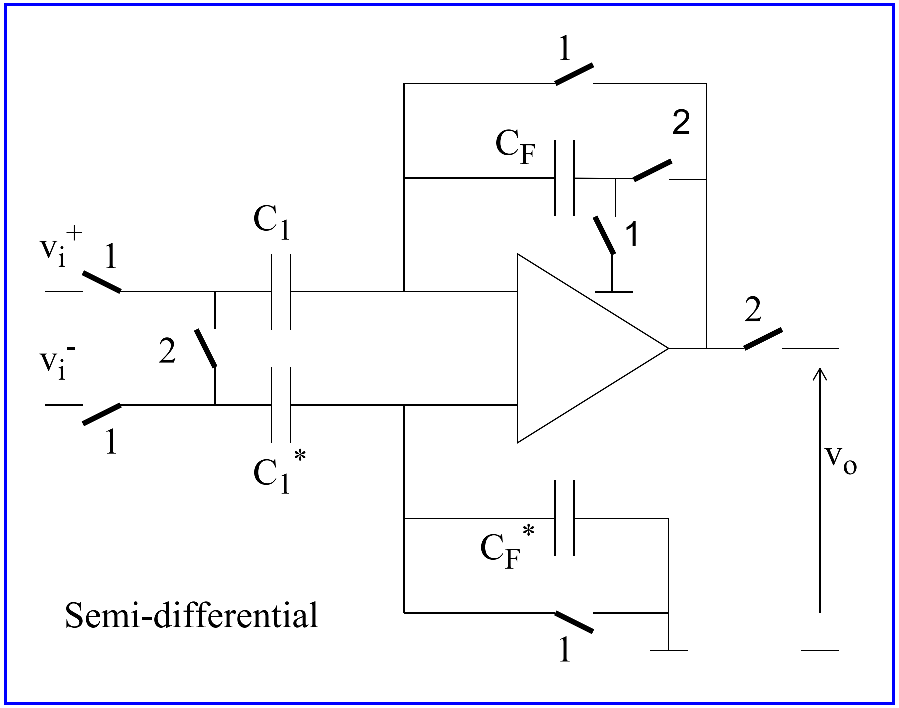
$$e^{-t_s/\tau} = 0{,}01$$

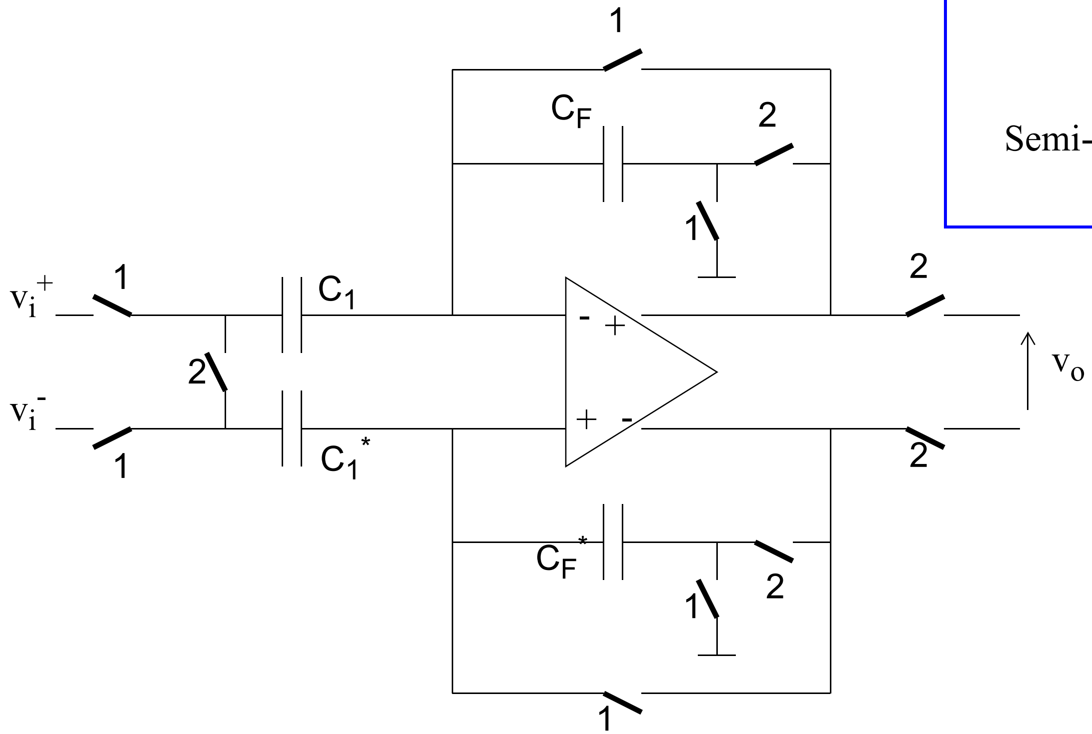
$$t_s = (-\tau)\ln 0{,}01 = 4{,}6\tau$$

$$\tau = \frac{t_s}{4{,}6}$$

Instrumental Amplifiers

- Correlated double sampling
  Phase 1: Offset and LF noise are stored at the input
  Phase 2: Subtracted from the amplified signal.
- Differential topology
  Reduces charge injection and clock feed through.
  Reduces non linearity in capacitors (distortion)
  Improves PSSR (Power Supply Rejection Ratio)

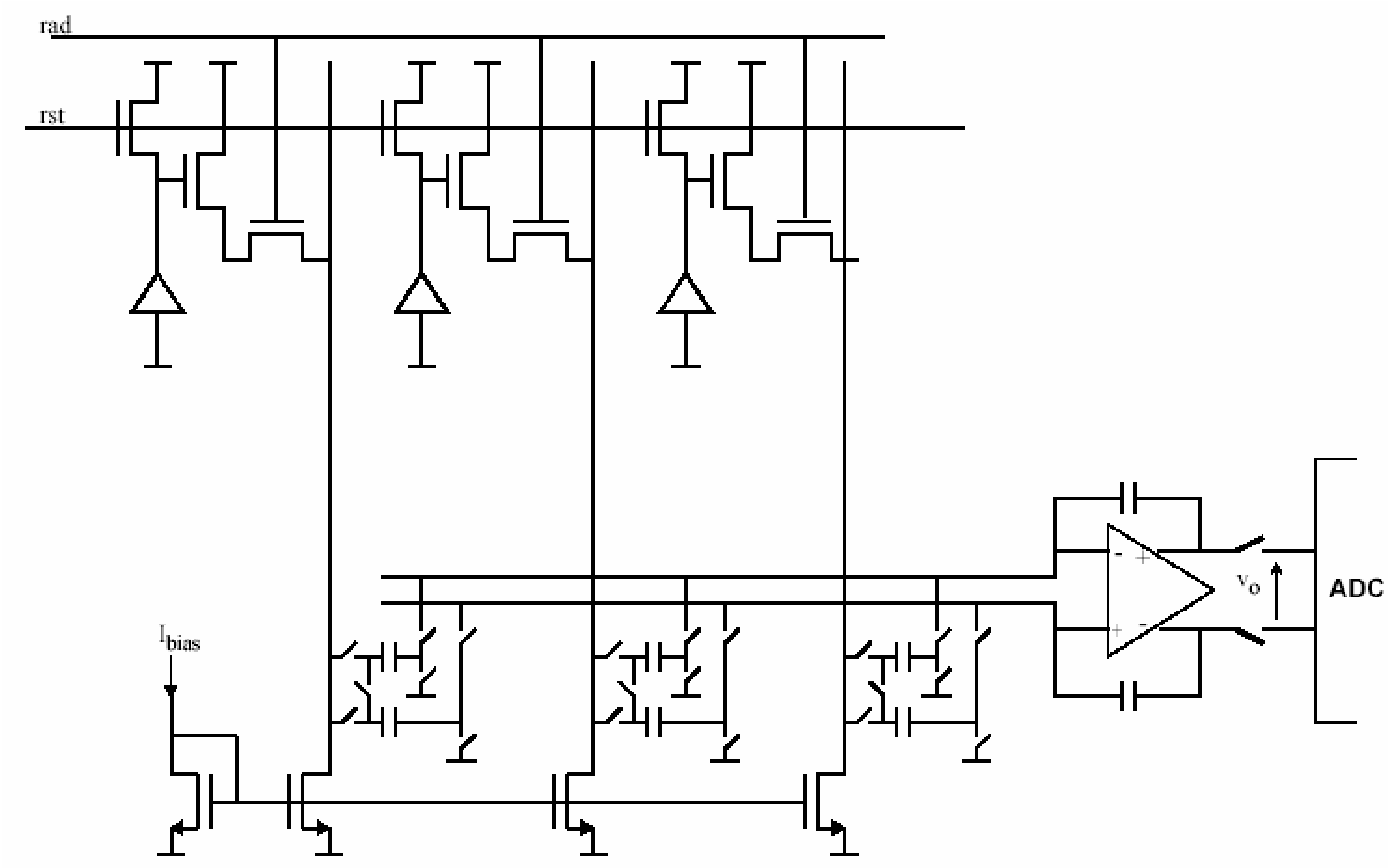




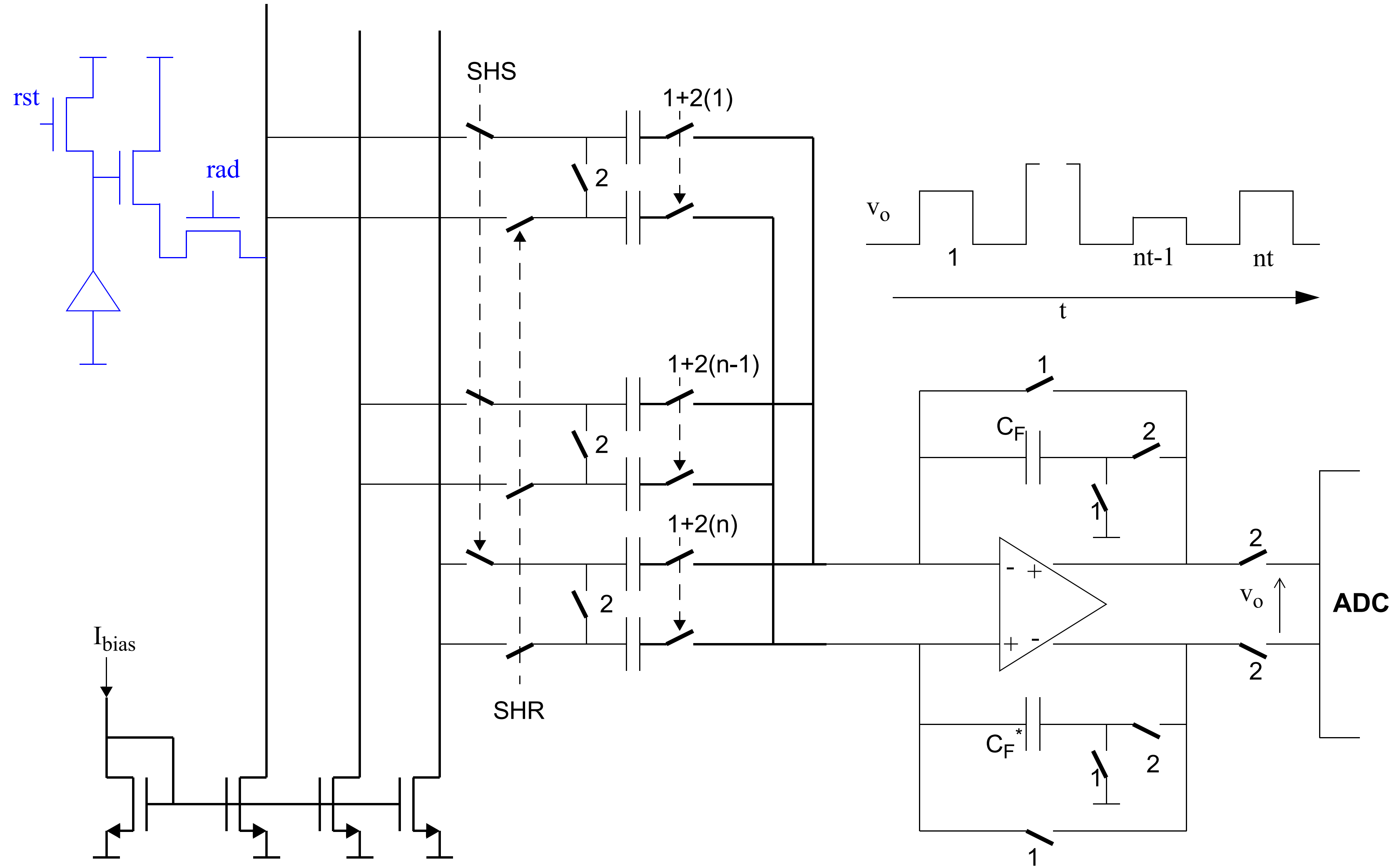
$$v_o = (v_i^+ - v_i^-)\, C_1/C_F$$

READ-OUT CHAIN ARCHITECTURE

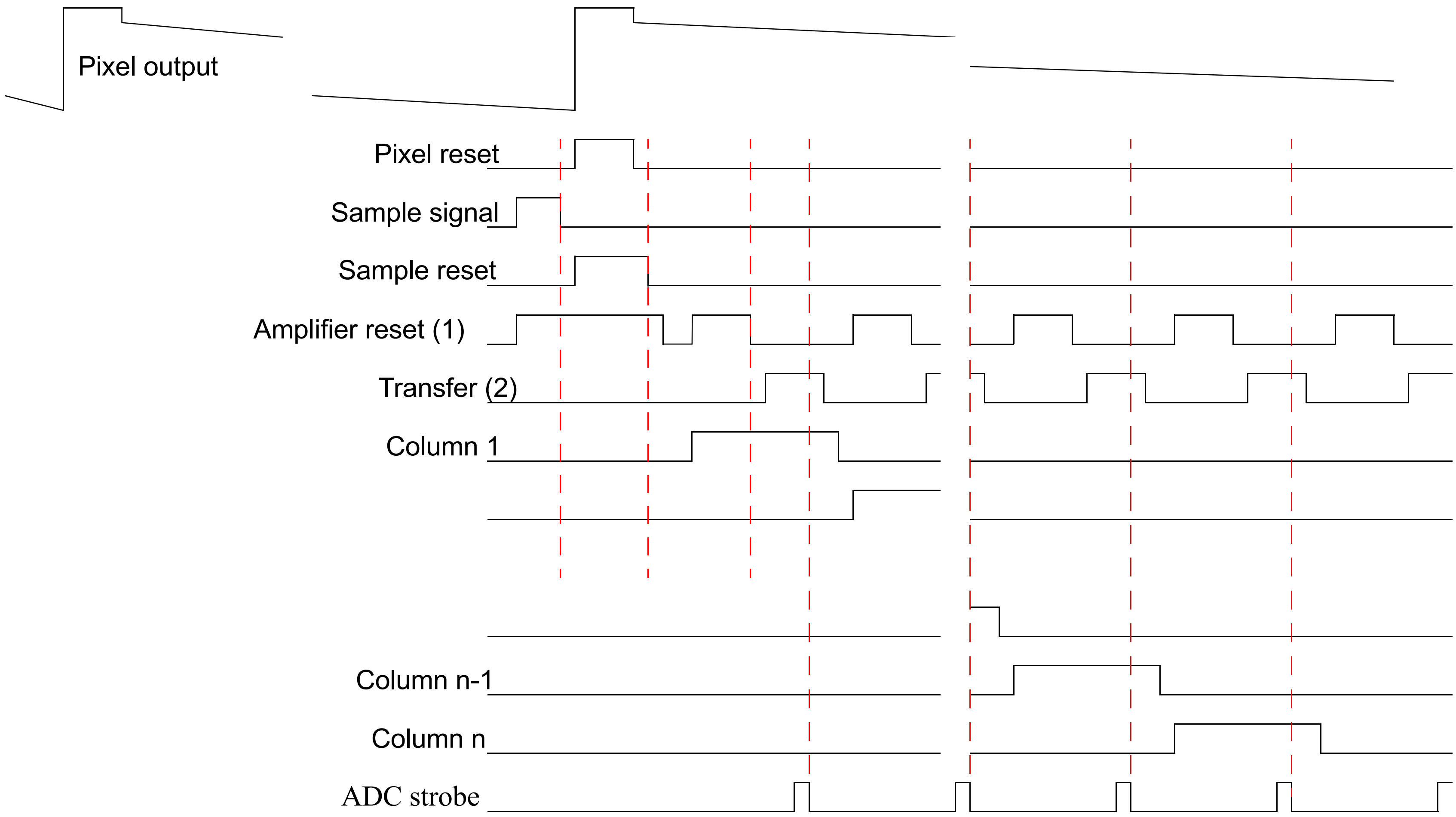
Column read out (principle)



Column read out (cont.)



Read out time diagram



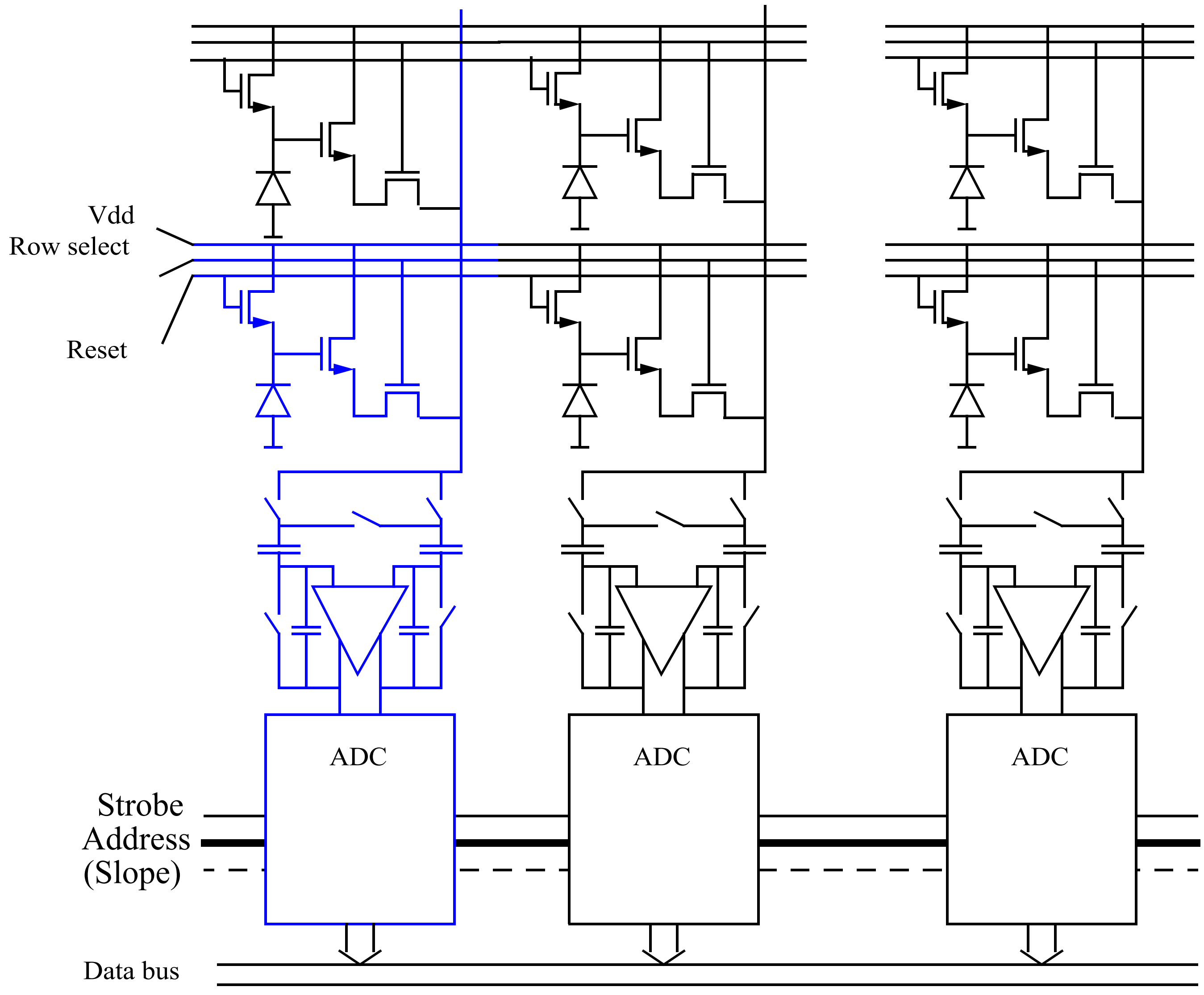
Column parallel read out (example)

Slow ADC is OK:

Successive Approximation

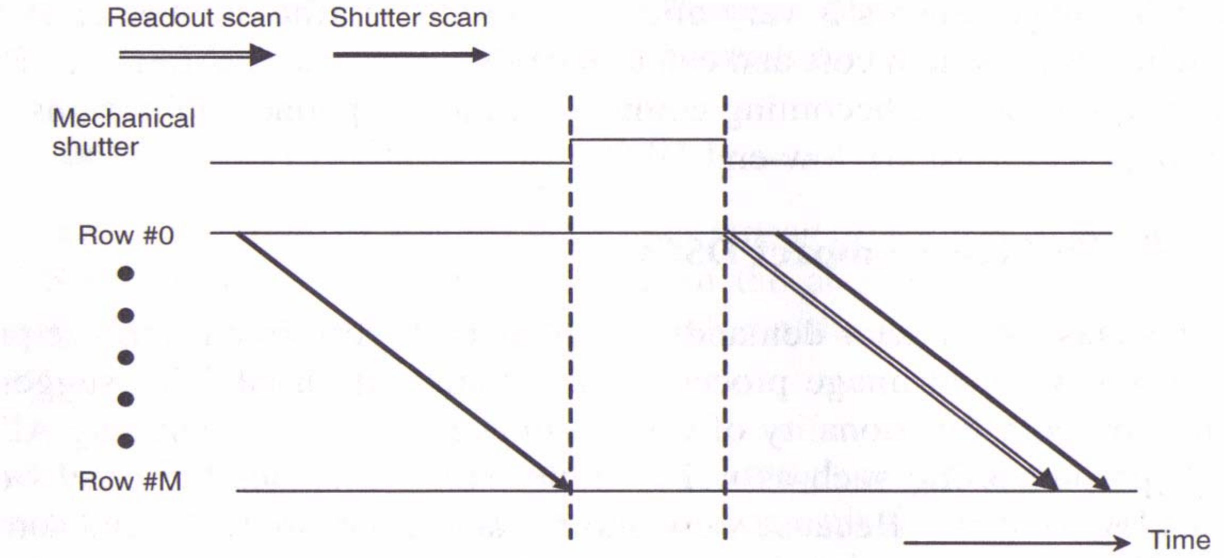
Single slope (common to all columns)

Cyclic

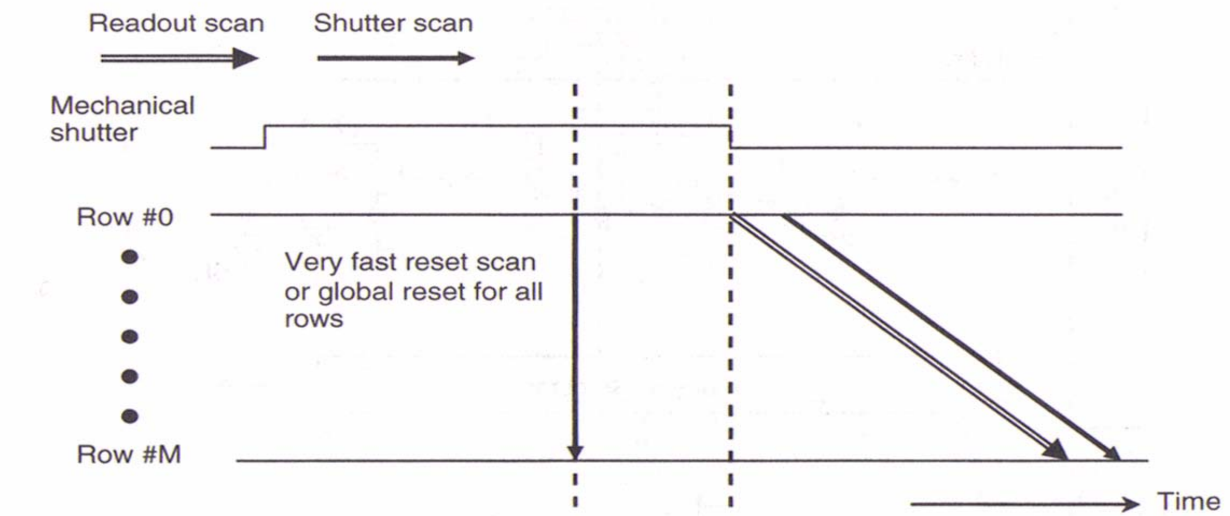


Synchronizing

Mechanical shutter Synchronized with ERS

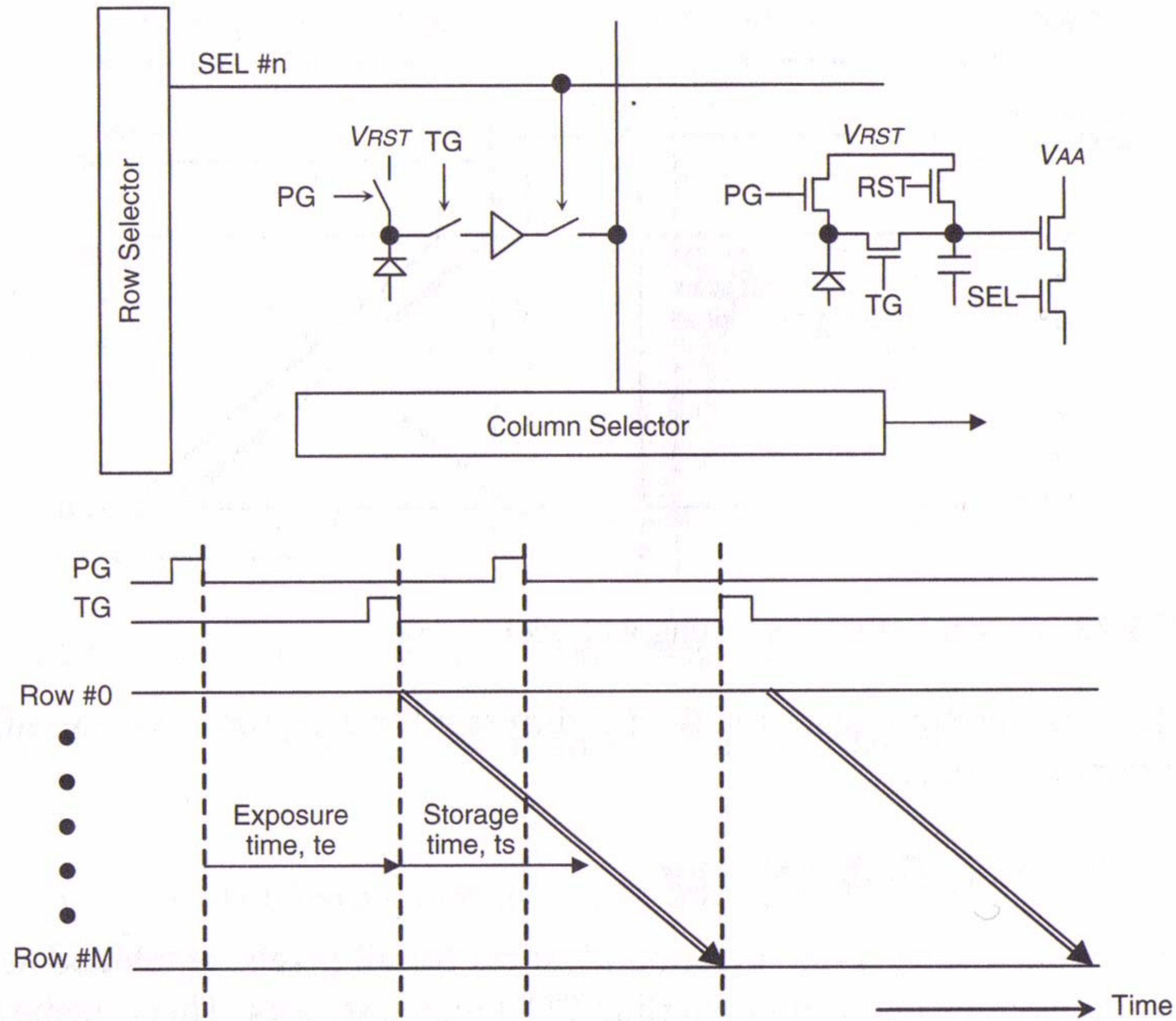


Mechanical shutter Synchronized with Global Reset



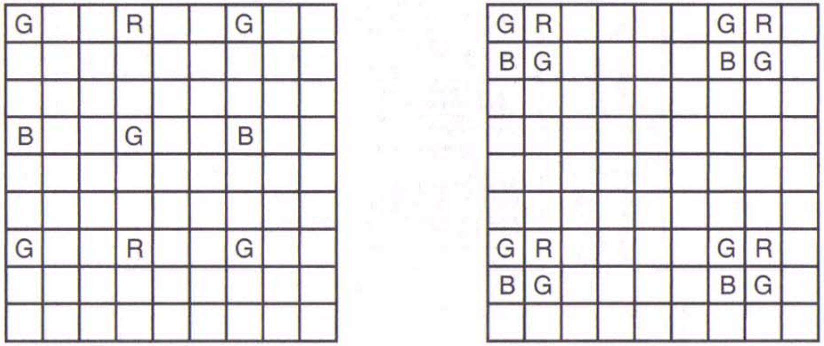
Synchronizing (cont.)

Electronic global shutter



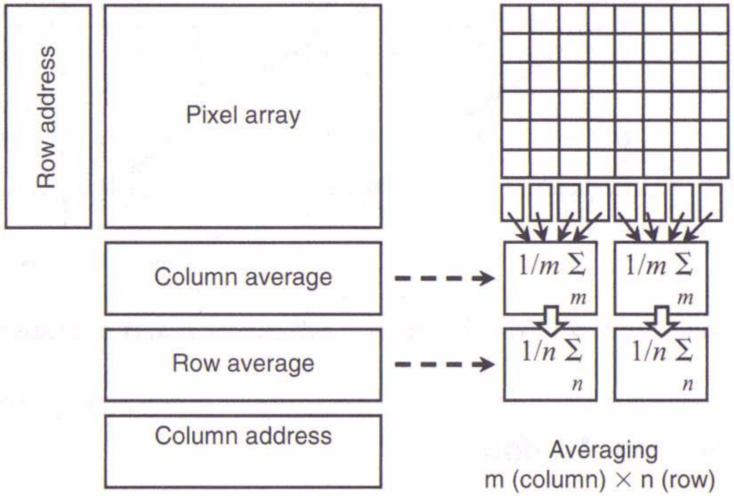
Reduced resolution but higher frame rates

Skipping
+ Simple solution
- Aliasing



(a) Constant pitch skipping (b) Pseudo-pixel pitch skipping

Binning
+ Spatial LP filter
- More complex



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