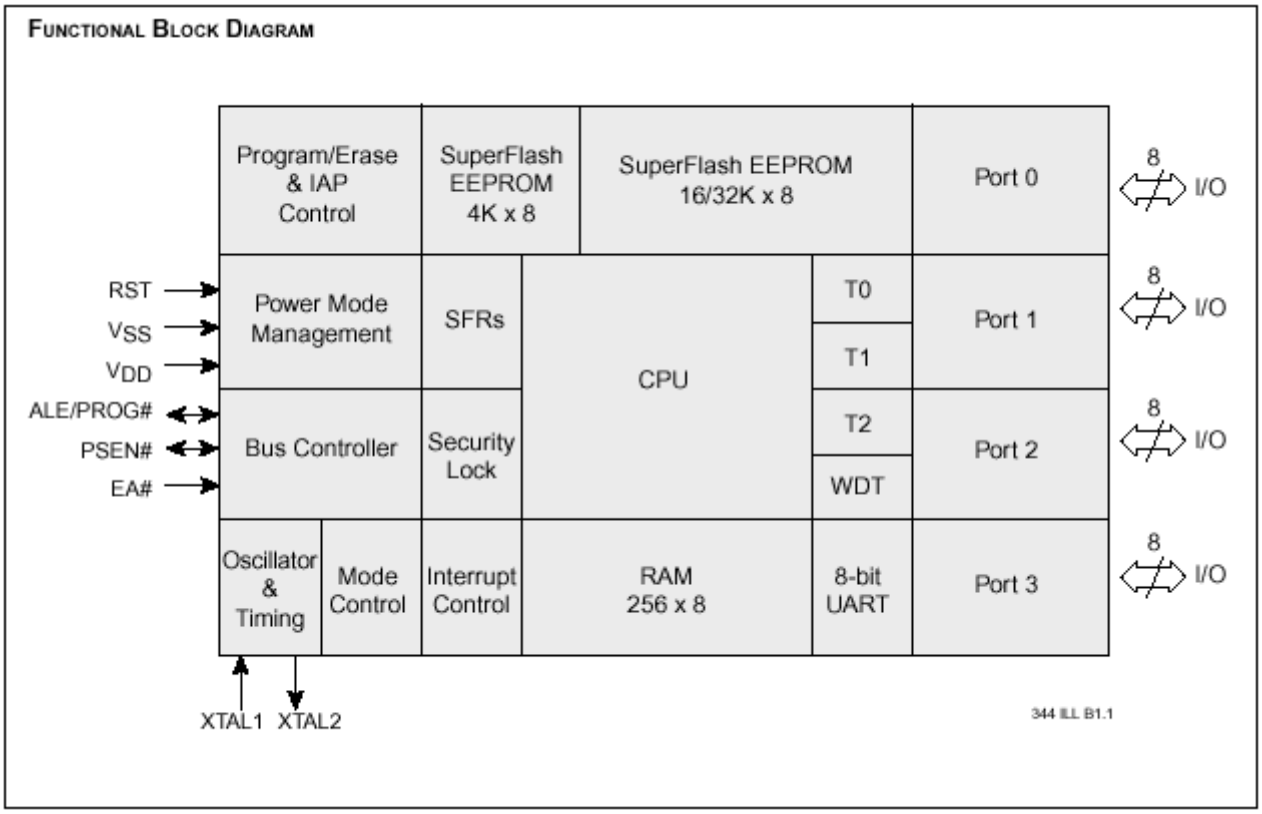
SST89C54/58 Technical Training

一. SST89C54/58 性能简介：

- ***与标准的 8052 引脚、指令和片内资源全兼容***
- 256 字节×8bit 内部 RAM
- 3 个 16 位定时/计数器(T0，T1，T2)
- 一个全双工、可编程串行通讯口(UART)
- 6 个中断源，2 个优先级
- 4 个 8 位 I/O 口(32 位 I/O 引脚)
- TTL 和 CMOS 电平全兼容
- 5V±10%供电时工作频率为 0—33MHz
- 3V±10%供电时工作频率为 0—12MHz
- 有三种封装 PDIP-40、PLCC-44 和 TQFP-44
- 有工业级（-40℃ — +85℃）和商用级（0℃—+70℃）
- ***内含 20KByte/36KByte 高性能 Flash***
  - 分为两个独立的大块(block0 和 block1，简称 B0 和 B1)
  - block0 为 16/32KByte×8bit，128 byte/sector
  - block1 为 4KByte×8bit，64 byte/sector
  - 两个大块可以分别加锁
  - 运行中可编程功能 IAP（In Application Program）

二. SST89C54/58 的优越性:

1. 内部 Flash 支持 IAP 编程，非常便于现场或远程软件修改、调试或升级，也可以用于保存数据。简化了系统设计，省去了通常外部扩展的 24XX 系列或 93XX 系列或小容量并行 E^2PROM(Flash)，元件数减少，PCB 面积也减小，系统可靠性增加，总体成本下降；
2. 保密性能好，不容易解密/仿制，后面有更详细介绍；
3. ***片内 Flash 容量大，分别为 20KB/36KB，凡是程序没有用完的剩余空间都可用于保存数据，因此空间利用率高，不浪费每一个字节；***
4. 每一颗芯片都支持 2.7V 至 5.5V 工作电压，不分型号、封装和温度范围。因此，SS89C54/58 真正是物有所值，性能/价格比极高；
5. 而且 SST 公司在全球范围内(美国、台湾、日本、韩国)有许多商业合作伙伴：IBM，Analog Devices，Rockwell International，Acer， TSMC， Lingsen， Sanyo， Seiko Epson， Anam， Samsung。



图一. SST89C54/58 内部功能框图

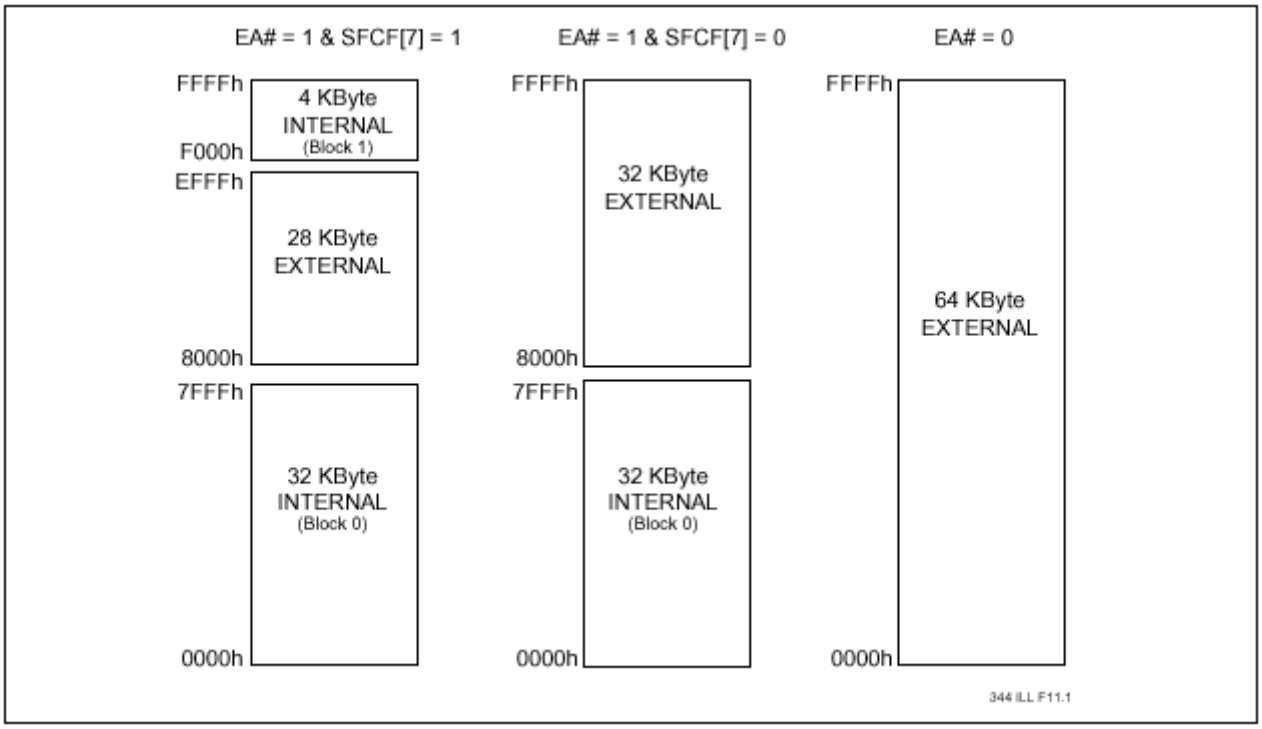
三. SST89C54/58 程序空间分配图

SST89C54/58 内部程序存储空间分别为 20K Byte/36K Byte，该空间划分为两个独立的大块：Block0 和 Block1。对 SST89C54 而言，Block0 占据从 0000H——3FFFH 的内部程序存储空间；对 SST89C58，Block0 则为 0000H-7FFFH。Block0 又可进一步细分为许多 Sector，每一个 Sector 均是 128 Byte；Block1 则无论是 SST89C54 还是 SST89C58 都是一样的，占据 F000H-FFFFH，共 4KB，其中每一个 Sector 为 64 Byte。

应该注意的是，Block0 和 Block1 的地址不是连续的，因此软件编程时一定要特别小心，一旦机器代码超过 Block0 的末地址而又不在 Block1 范围内，程序执行后果将不可预料，这个时候程序一定要首先使 SFCF.7(VIS)位置 1，用 ORG 0F000H 定位，然后用 LJMP 或 LCALL 指令保证程序正确地越过中间的***外部程序存储区***而正常进入 Block1 继续执行。

程序在 Block1 执行对 Block0 的擦除、改写指令时，在擦除、改写完成以前，Block0 始终处于忙状态之中，此时不能响应任何中断。为此，SST89C54/58 允许 Block1 映射到 Block0。Block1 映射之后，中断产生时，本来位于 Block0 的中断服务程序就自动转向 Block1 中执行。而 Block1 中的中断服务程序要么由编程器烧入，要么由程序本身写入。

图二. SST89C54/58 程序空间分布图



Re-Map [1:0][1]	MAP_EN[2,3]	Comments
11	00	Re-mapping is turned off. Program memory is in normal configuration.
10	01	1 KByte of flash memory location is re-mapped. Program access to location 0000h-03FFh is redirected to F000h – F3FFh.
01	10	2 KBytes of flash memory location are re-mapped. Program access to location 0000h-07FFh is redirected to F000h – F7FFh.
00	11	4 KBytes of flash memory location is re-mapped. Program access to location 0000h-0FFFh is redirected to F000h – FFFFh.

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1 Re-Map[1:0] are nonvolatile registers which are examined only during Reset.
2 MAP_EN[1:0] are initialized according to Re-Map[1:0] during Reset.
3 MAP_EN[1:0] are located in SFCF[1:0], they determine the Re-Mapping configuration. They may be changed by the program at run time.

四. 内部 Flash 的两种编程模式：

⑴外主模式（External Host Mode）：

在 RST 引脚保持为高的情况下，如果 PSEN 引脚强行输入一个从高电平到低电平的跳变（通常 PSEN 是输出允许取指脉冲），SST89C54/58 就进入外主模式（External Host Mode）。

在外主模式下，CPU 是停止运行的，SST89C54/58 可以简单地看作是一个普通的 Flash 芯片，如同 SST28SF040 一样。在这种方式下，其 4 个八位 I/O 口引脚的功能是经过重新定义的，P0 口输入/输出数据 D0-D7，P1 口是低八位地址 A0-A7，P2 口的 P2.0-P2.5 代表 A8-A13，A14、A15 分别是 P3.4 和 P3.5，而 P2.6、P2.7 和 P3.6 、P3.7 是编程控制信号。图三　外主模式下 I/O 引脚功能重新定义：

在外主模式下，SST89C54/58 可以接受的命令表如下：

Operation	RST	PSEN#	PROG# /ALE	EA#	P3[7]	P3[6]	P2[7]	P2[6]	P0[7:0]	P1[7:0]	P3[5:4] P2[5:0]
READ-ID	H	L	H	H	L	L	L	L	DO	AL	AH
CHIP-ERASE	H	L	⇓	H	L	L	L	H	X	X	X
BLOCK-ERASE	H	L	⇓	H	H	H	L	H	X	X	A[15:12]
SECTOR-ERASE	H	L	⇓	H	H	L	H	H	X	AL	AH
BYTE-PROGRAM	H	L	⇓	H	H	H	H	L	DI	AL	AH
BURST-PROGRAM	H	L	⇓	H	L	H	H	L	DI	AL	AH
BYTE-VERIFY (Read)	H	L	H	H	H	H	L	L	DO	AL	AH
PROG-SB1	H	L	⇓	H	H	H	H	H	X	X	X
PROG-SB2	H	L	⇓	H	L	L	H	H	X	X	X
PROG-SB3	H	L	⇓	H	L	H	L	H	X	X	X
PROG-RB0	H	L	⇓	H	H	L	L	L	X	X	X
PROG-RB1	H	L	⇓	H	H	L	L	H	X	X	X

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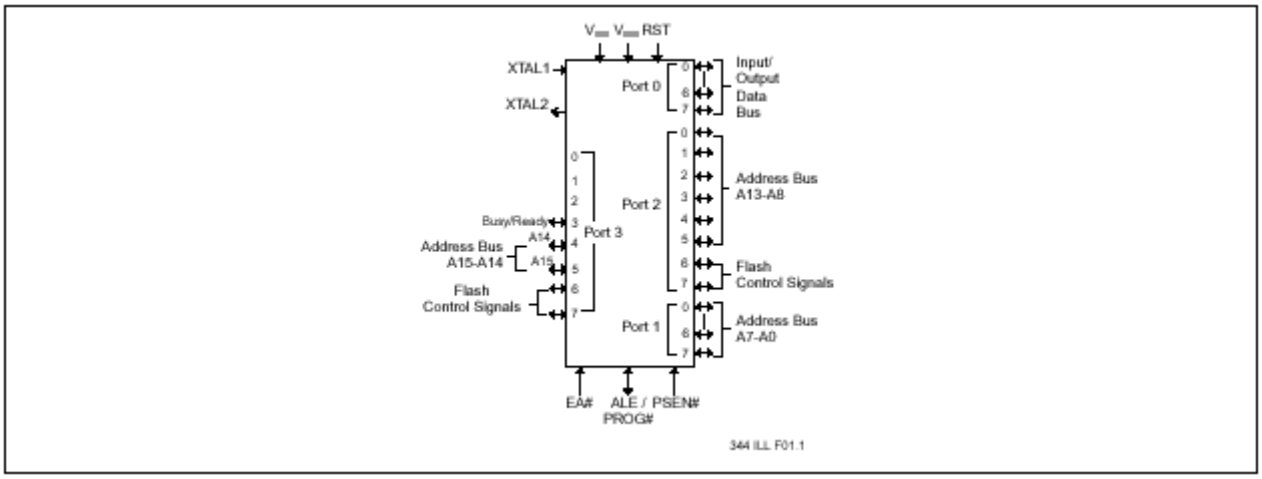
Note: Symbol ⇓ signifies a negative pulse and the command is asserted during the low state of PROG#/ALE input. All other combinations of the above input pins are invalid and may result in unexpected behaviors.

Note: L = Logic low level; H = Logic high level; X = Don't care; AL = Address low order byte; AH = Address high order byte; DI = Data Input; DO = Data Output; A[15:12] = 0xxxb for Block 0 and A[15:12] = "Fh" for Block 1.



应该注意的是，在外主模式下对 SST89C54/58 编程，所有的擦除、写入、读出等操作均是芯片内自定时，毋需外接晶体。

正因为在外主模式下 CPU 是停止工作的，而且各 I/O 口引脚功能又已经重新定义，因此这种编程方式主要是针对在编程器上对 SST89C54/58 编程。在用户电路板上，可以说看不到用户使用这种方式，否则为了下载程序或保存数据，其硬件开销太大。所以用户一般都会选择 IAP 这种模式来下载更新程序或保存数据。

(2)In Application Programming Mode（IAP)：

IAP 模式简单地说就是 CPU 一边在某一个 block 中运行程序，同时可以对另一个 block 进行擦除、写入、校验等操作。IAP 支持的命令见下表：

Operation	SFAH [7:0]	SFAL [7:0]	SFDT [7:0]	SFCM [6:0][1]
CHIP-ERASE	X	X	55h	01h
BLOCK-ERASE	AH[2]	X	55h	0Dh
SECTOR-ERASE	AH	AL	X	0Bh
BYTE-PROGRAM	AH	AL	DI	0Eh
BURST-PROGRAM	AH	AL	DI	06h
BYTE-VERIFY (Read)	AH	AL	DO	0Ch

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Notes: X = Don't Care; AL = Address low order byte; AH = Address high order byte;
DI = Data Input; DO = Data Output
All other values are in hex
[1] Interrupt/Polling enable for flash operation completion
SFCM[7] = 1: Interrupt enable for flash operation completion
0: polling enable for flash operation completion
[2] SFAH[7] = 0: Selects Block 0: SFAH[7:4] = Fh selects Block 1

与 IAP 功能有关的所有新增加的 SFR 的定义及位置介绍如下：

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
SFST	SuperFlash Status	B6h	SECD[2:0]			-	BUSY	Flash_busy	-	-	xxx00000b
SFCF	SuperFlash Configuration	B1h	VIS	IAPEN	-	-	-	-	MAP_EN		000000xxb
SFCM	SuperFlash Command	B2h	FIE	FCM							00h
SFDT	SuperFlash Data	B5h	SuperFlash Data Register								00h
SFAL	SuperFlash Address Low	B3h	SuperFlash Low Order Byte Address Register – A7 to A0 (SFAL)								00h
SFAH	SuperFlash Address High	B4h	SuperFlash High Order Byte Address Register – A15 to A8 (SFAH)								00h

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SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
0B6h	SECD2	SECD1	SECD0	–	Busy	Flash_busy	–	–	xxx00000b

Symbol	Function
SECD2	Security bit 1.
SECD1	Security bit 2.
SECD0	Security bit 3. Please refer to Table 8 for security lock options.
BUSY	Burst-Program completion polling bit. 1: Device is busy with flash operation. 0: Device is available for next Burst-Program operation.
Flash_busy	Flash operation completion polling bit. 1: Device is busy with flash operation. 0: Device has fully completed the last command, including Burst-Program.

SuperFlash Configuration Register (SFCF)

Location	7	6	5	4	3	2	1	0	Reset Val
0B1h	VIS	IAPEN	–	–	–	–	MAP_EN1	MAP_EN0	000000x

Symbol	Function
VIS	Upper flash block visibility. 1: 4 KByte flash block visible from F000-FFFF. 0: 4 KByte flash block not visible.
IAPEN	Enable IAP operation. 1: IAP commands are enabled. 0: IAP commands are disabled.
MAP_EN1	Map enable bit 1.
MAP_EN0	Map enable bit 0. MAP_EN[1:0] are initialized to default value according to Re-map [1:0] during Reset. Refer to Table 2.

SuperFlash Command Register (SFCM)

Location	7	6	5	4	3	2	1	0	Reset Val
0B2h	FIE	FCM6	FCM5	FCM4	FCM3	FCM2	FCM1	FCM0	0000000

Symbol	Function
FIE	Flash Interrupt Enable. 1: INT1# is re-assigned to signal IAP operation completion. External INT1# interrupts are ignored. 0: INT1# is not reassigned.
FCM[6:0]	Flash operation command. 000_0001b Chip-Erase. 000_0110b Burst-Program. 000_1011b Sector-Erase. 000_1100b Byte-Verify. (1) 000_1101b Block-Erase. 000_1110b Byte-Program. All other combinations are not implemented, and reserved for future use.

(1) Byte-Verify has a single machine cycle latency and will not generate any INT1# interrupt regardless of FIE.

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
0B5h	SuperFlash Data Register								00000000b

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block (Data register).

SuperFlash Address Registers (SFAL)

Location	7	6	5	4	3	2	1	0	Reset Value
0B3h	SuperFlash Low Order Byte Address Register								00000000b

Symbol	Function
SFAL	Mailbox register for interfacing with flash memory block. (Low order address register).

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
0B4h	SuperFlash High Order Byte Address Register								00000000b

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register).

★ Chip Erase:

1. MOV SFCF, #0C0H
2. MOV SFDT, #55H
3. MOV SFCM, #01H
4. 查询 SFST.2，等待芯片擦除结束
5. 用 MOVC 校验是否每个单元均为 FFh。

★ Block Erase:

1. MOV SFCF, #0C0H
2. MOV SFAH, #0F0H/#00H ; 擦除 block1/block0
3. MOV SFDT, #55H
4. MOV SFCM, #0DH
5. 查询 SFST.2，等待芯片擦除结束
6. 校验是否每个单元均为 FFh

★ Sector Erase:

1. MOV SFCF, #0C0H
2. MOV SFAH, MSB Of Sector Address
3. MOV SFAL, LSB Of Sector Address
4. MOV SFCM, #0Bh,
5. 查询 SFST.2，等待芯片擦除结束
6. 校验是否每个单元均为 FFh

★ Byte Program:

1. MOV SFCF, #0C0H
2. MOV SFAH, direct / #data8 ; MSB address of byte
3. MOV SFAL, direct / #data8 ; LSB address of byte
4. MOV SFDT, direct / #data8 ; data to be written
5. MOV SFCM, #0EH
6. 查询 SFST.2，等待芯片写入结束
7. 校验该单元写入数据是否正确

★ Burst Program:

1. MOV SFCF, #0C0H
2. MOV SFAH, direct / #data8 ; MSB address of byte
3. MOV SFAL, direct / #data8 ; LSB address of byte
4. MOV SFDT, direct / #data8 ; data to be written
5. MOV SFCM, #06H
6. 查询 SFST.3，等待该字节写入结束 ；**注意此处不是查询 SFST.2！**
7. 重复第 2 至第 6 步，直到写完整个扇区。
8. 查询 SFST.2，等待芯片扇区写入结束;
9. 校验该扇区所有数据是否写入正确

★ Byte Verify (READ):

1. MOV SFCF, #0C0H
2. MOV SFAH, direct / #data8
3. MOV SFAL, direct / #data8
4. MOV SFCM, #0CH
5. NOP
6. MOV A, SFDT; A 保存规定单元地址读出的内容

另一个更直截了当的方法是，用 MOVC 指令取出某单元地址的内容。但要注意，虽然名义上叫 Byte Verify，但实际上只是把单元内容读出来，并没有真正与原始数据作比较，还需要软件用 CJNE 或 XRL 等其他指令完成真正的比较。

★ PROG-RB0, PROG-RB1:

1. MOV SFCF, #0C0H
2. MOV SFDT, #55H
3. MOV SFCM, #08H / #09H ; PROG-RB0 / PROG-RB1
4. 查询 SFST.2，等待芯片写入结束
5. 检查 SFCF.1(MAP_EN1), SFCF.0(MAP_EN0)是否正确

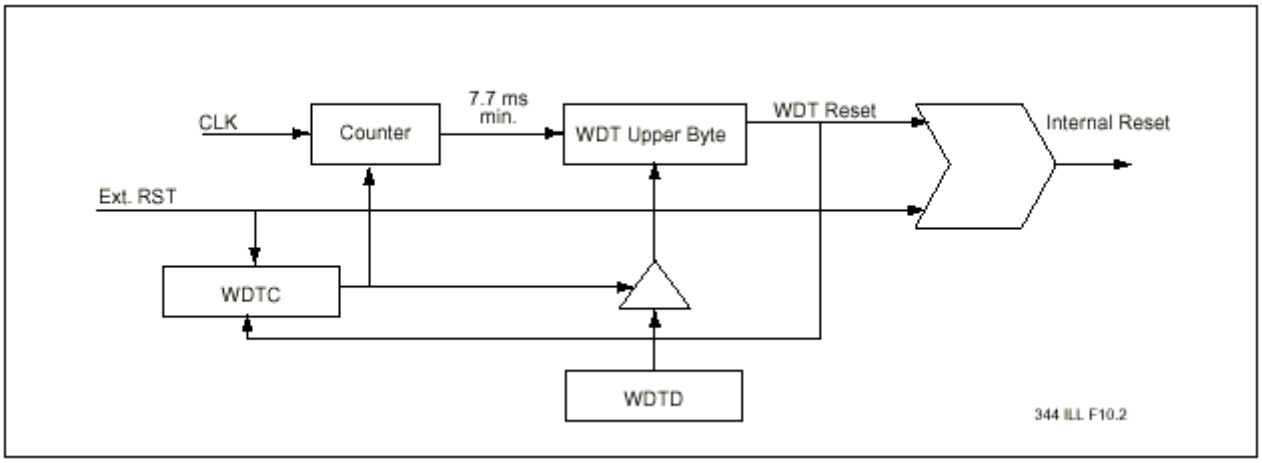
★ PROG-SB1, PROG-SB2, PROG-SB3:

1. MOV SFCF, #0C0H
2. MOV SFDT, #55H
3. MOV SFCM, #0FH / #03H / #05H ; PROG-SB1 / PROG-SB2 / PROG-SB3
4. 查询 SFST.2，等待芯片写入结束
5. 检查 SFST.7(SECD2), SFST.6(SECD1), SFST.5(SECD0)是否正确

警告：IAP 编程时，block0 一定不能对此 block0 本身进行改写，同样 block1 也不能对 block1 本身进行改写，否则 CPU 会死机。block0 和 block1 只能互相进行交叉改写。

五. Watchdog Timer

SST89C54/58 内置有一个与晶体振荡器无关的独立的看门狗（Watchdog Timer），可以保证单片机在恶劣工作环境下工作可靠，或者排除与软硬件有关的故障（死循环）。Watchdog Timer 内部框图如下：



在 Idle 状态，Watchdog Timer 暂时停止工作，中断退出 Idle 状态之后，自动恢复工作。与 Watchdog Timer 有关的寄存器如下页。

有关 Watchdog Timer 的使用请参考附录二　Watchdog.asm。

WDTC*	Watchdog Timer Control	C0h	-	-	-	-	WDRE	WDTS	WDT	SWDT	X0h
WDTD	Watchdog Timer Data/Reload	86h	WDRL								00h

* = Bit Addressable SFRs

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Watchdog Timer Control Register (WDTC)

Location	7	6	5	4	3	2	1	0	Reset Value
0C0h	–	–	–	–	WDRE	WDTS	WDT	SWDT	00000000b

Symbol	Function
WDRE	Watchdog timer reset enable. 1: Enable watchdog timer reset. 2: Disable watchdog timer reset.
WDTS	Watchdog timer reset flag. 1: Hardware sets the flag on watchdog overflow. 0: External hardware reset clears the flag. Flag can also be cleared by writing a 1. Flag survives if chip reset happened because of watchdog timer overflow.
WDT	Watchdog timer refresh. 1: Software sets the bit to force a watchdog timer refresh. 0: Hardware resets the bit when refresh is done.
SWDT	Start watchdog timer. 1: Start WDT. 0: Stop WDT.

Watchdog Timer Data/Reload Register (WDTD)

Location	7	6	5	4	3	2	1	0	Reset Value
086h	Watchdog Timer Data/Reload								00000000b

Symbol	Function
WDTD	Initial/Reload value in Watchdog Timer.

六. Security:

SST89C54/58 具有很完善的保密机制，可以很好地保护客户的程序代码和数据不会被非法解密或复制。

SST89C54/58 加密方式很灵活，内部两大块可以加密，也可以不加密，还可以单独加密，总共有 4 级加密方式，如下表。注意：加密单元内容改变之后，必须等到***下一次复位***后才起作用。

Level	Security Lock Bits				Security Status of:		Security Type
	SFST[7:5]	1[1]	2[1]	3[1]	Block 1	Block 0	
1	000	U	U	U	Unlock	Unlock	No Security Features are Enabled.
2	100	P	U	U	Hard Lock	Hard Lock	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA# is sampled and latched on Reset, and further programming of the flash is disabled.
3	110	P	P	U	Hard Lock	Hard Lock	Level 2 plus Verify disabled, both blocks locked.
	101	P	U	P			
	010	U	P	U	SoftLock	SoftLock	Level 2 plus verify disable. code in Block 1 can program Block 0 and vice versa.
	001	U	U	P	Hard Lock	SoftLock	Level 2 plus verify disabled, code in Block 1 can program Block 0.
4	111	P	P	P	Hard Lock	Hard Lock	Same as Level 3, but external boot is disabled.

Notes: 344 PGM T8.4
1 1, 2, and 3, respectively, refer to the first, second, and third security lock bits.
2 P = Programmed (Cell logic state = 1), U = Unprogrammed (Cell logic state = 0).
3 SFST[7:5] = Security Lock Decoding Bits (SECD)
4 All unused combinations default to level 4, "PPP".

一旦加密之后，内部没有加密的块或者外部程序就不能存取已加密单元部分，但加密之后的块可以存取同样加密了的另一个块，请看下图：

有两点理由请大家放心，采用 SST89C54/58 不会轻易被解密：

SFST[7:5]	MOVC Address[1]	Target Address[2]	MOVC allowed[3]
011/100/101/110/111 (Hard Lock on both blocks)	Block 0/1	Any Location	Y
	External Memory	Block 0/1	N
		External	Y
001 (Block 0 = SoftLock Block 1 = Hard Lock)	Block 0	Block 0	Y
		Block 1	N
		External	Y
	Block 1	Any Location	Y
	External	Block 0/1	N
		External	Y
010 (SoftLock on both blocks)	Block 0/1	Any Location	Y
	External	Block 0/1	N
		External	Y
000	Any Location	Any Location	Y

Notes: 344 PGM T9.3
1 Location of MOVC instruction
2 Target Address is the location of the instruction being read
3 **Y** = Indicates MOVC instruction is allowed; **N** = Indicates MOVC instruction is not allowed;

(1) SST89C54/58 加密单元的物理地址是未知的，而且每颗芯片加密单元的具体物理地址是不一样的，SST 公司不会公开这个秘密，毫无疑问这增加了解密的难度；

其他目前市场上比较流行的 FLASH 单片机就不是这样，其加密单元都是独立的，一般只有两三个比特位，一个很小的区域，而程序存储区域一般都很大，所以在专用设备下，加密单元很容易与程序存储区域本身区分开来。

(2) SST89C54/58 是一种新产品，**这至少可以保证你的产品在最近一两年之内不会被解密或仿制**。

七. Power Saving Modes：

SST89C54/58 支持三种省电模式：Idle，Power down 和 Standby（Stop），并且 SST89C54/58 支持**外部低电平中断退出 Power down 状态**，这是一个非常有用的功能。

Mode	Initiated by	Current Drain	State of MCU	Exited by
Idle Mode	Software (Set IDL bit in PCON)	25% of I_{DD} level when device is fully active	CLK is running. Interrupts, serial port and timers/counters are active. Program Counter is stopped. ALE and PSEN# signals at a HIGH level during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits Idle mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked Idle mode. If needed in a specific application, a user could consider placing two or three NOP instructions after the instruction that invokes idle mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Power Down Mode	Software (Set PD bit in PCON)	Typically 15 microamps. And V_{DD} can be reduced by ext. hardware to 2V during (after entry and before exit) Power Down mode.	CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and PSEN# signals at a LOW level during Power Down. External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits Power Down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked Power Down mode. If needed in a specific application, a user could consider placing two or three NOP instructions after the instruction that invokes Power Down mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Standby (Stop Clock) Mode	External hardware gates OFF the external clock input to the MCU. This gating should be synchronized with an input clock transition (low-to-high or high-to-low).	Typically 15 microamps. And V_{DD} can be reduced by ext. hardware to 2V during (after entry and before exit) Standby mode.	CLK is frozen. On-chip SRAM and SFR data is maintained. ALE and PSEN# are maintained at the levels prior to the clock being frozen.	Gate ON external clock. Program execution resumes at the instruction following the one during which the clock was gated off.

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八. 开发工具：

目前在国内编程器市场占有率比较高的四大名牌厂家都已支持 SST89C54/58 的编程：HiLo 公司的 ALL-11，Gang-08；Leap 公司的 LP-10；Xeltek 公司的 SuperProIII；AdvanTech 公司的 LabTool-48。

汇编程序编译、连接定位程序不用升级或更换，只需要在汇编源文件的开始用 EQU 或 DATA 伪指令定义一下新增加的 SFR 在内部 RAM 中的地址，就可以正常使用这些特殊功能寄存器名进行各种读、写、擦除操作，请参看附录一 IAPDemo.asm。

C51 头文件清单请参看附录三 SST89C5X.h，编译、连接定位程序同样也勿需升级或更换。

仿真器：目前国内通用的仿真/开发器还暂时不支持 IAP 功能的仿真调试，但是 IAP 功能真的是很简单，很容易掌握，附录一 IAPDemo.asm 是一个完整的程序，编译之后烧录到 SST89C54/58 中可以运行验证，大家掌握之后，一定会发现 IAP 真的是不用仿真调试。

下表是国外仿真器厂家的联系地址和产品型号：

In-Circuit Emulators (ICE)

Company	Tools	Availability
Hitex Development Tools 710 Lakeway Drive, Suite 280 Sunnyvale, CA 94086 Phone: 408.733.7080 Toll Free: 800.45.HITEX Fax: 408.733.6320 Web: www.hitex.com **Hitex-Systementwicklung** Greschbachstrasse 12 D-76229 Karlsruhe, Germany Phone: +49.721.9628.133 Fax: +49.721.9628.189 Web: www.hitex.de	MX51A (to 40 MHz)	Now
Metalink Corporation 325 E. Elliot Road, Suite 23 Chandler, AZ 85225 Phone: 602.926.0797 Fax: 602.926.1198 Web: http://metaice.com	iceMaster-PE (to 16 MHz) iceMaster-AA (to 24 MHz) iceMaster-SF (to 33 MHz)	Now Now 2Q99
Nohau Corporation 51 E. Campbell Avenue Campbell, CA 95008 Phone: 408.866.1820 Fax: 408.378.7869 Web: www.nohau.com	EMUL51 (to 42 MHz)	Now
Phyton, Inc. 7206 Bay Parkway, 2nd Floor Brooklyn, NY 11204 Phone: 718.259.3191 Fax: 718.259.1539 Web: www.phyton.com	PICE-51 (to 40 MHz)	Now

Evaluation Kits

Company	Tools	Availability
PHYTEC America LLC 755 Winslow Way E, Suite 302 Bainbridge Island, WA 98110 Phone: 206.780.9047 Toll Free: 800.278.9913 Fax: 206.780.9135 Web: www.phytec.com **PHYTEC Meßtechnik GmbH** Robert-Koch-Straße 39 D-55129 Mainz, Germany Phone: +49.6131.9221.0 Fax: +49.6131.9221.33	KitCON-FlashFlex51	Now

九.附录一　IAPDemo.asm 程序清单:

```
; define SST89C54/58 added Special Function Registers:
       SFST    EQU  0B6H       ; SuperFlash Status Register
       SFCF    EQU  0B1H       ; SuperFlash Configuration Register
       SFCM    EQU  0B2H       ; SuperFlash Command Register
       SFDT    EQU  0B5H       ; SuperFlash Data Register
       SFAL    EQU  0B3H       ; SuperFlash Address Low Register
       SFAH    EQU  0B4H       ; SuperFlash Address High Register
; you may use DATA to replace above EQU, eg.  SFCF   DATA   0B1H

;name\bit    D7   D6   D5  D4  D3      D2      D1  D0
;SFST         SECD[2:0]    -- BUSY Flash_Busy  --  --
;SFCF       VIS IAPEN  --  --  --      --      MAP_EN
;SFCM       FIE               FCM

;SFST.3=BUSY, 1: Chip is busy with flash operation(burst_program)
;             0: Chip is ready for next burst_program operation
;SFST.2=Flash_Busy, 1: Chip is busy with flash operation
;                   0: Chip has completed the last command, including Burst_Program
;SFCF.7=VIS, 1: upper 4KByte Block1 is visible and can be accessed by PC
;            0: invisible. Block1 must be accessed by SFCF,SFDT,SFAL/AH,SFCM
;SFCF.6=IAPEN, 1: Enable IAP commands
;              0: Disable IAP commands
;SFCM.7=FIE, 1: INT1 will interrupt CPU when IAP operation is completed.
;            0: no INT1 interrupt generated when IAP is done.
;SFCM.[6:0] = FCM
;  000 0001 = Chip_Erase
;  000 0110 = Burst_Program
;  000 1011 = Sector_Erase
;  000 1100 = Byte_Verify
;  000 1101 = Block_Erase
;  000 1110 = Byte_Program

              ORG  0000H
              LJMP MAIN

              ORG 0040H
MAIN:         ORL SFCF,#0C0H          ; VIS=1, IAPEN=1
              MOV DPTR,#0F000H
              LCALL SECTORERASE

              MOV R3,#64          ; 64 byte/sector in Block1
```

```
                MOV R4,#00H

WRITE:          LCALL WRITEBYTE
                INC   DPTR
                INC   R4
                DJNZ  R3,WRITE

                MOV   DPTR,#0F000h
                MOV   B,#0
                MOV   R3,#64
                MOV   R4,#0

READ:           CLR   A
                MOVC A,@A+DPTR    ;If SFCF.7=VIS=1, can use MOVC instruction
                INC   DPTR        ; otherwise, MUST use Byte Verify of IAP command
                XRL   A,R4
                JNZ   FAIL
                SJMP NEXTBYTE
FAIL:           INC   B
NEXTBYTE:       INC   R4
                DJNZ R3,READ
                MOV   P1,B         ; B != 0 if there are any errors
                SJMP $

SECTORERASE:    MOV   SFCF,#0C0H
                MOV   SFAH,DPH     ; DPTR contains sector address
                MOV   SFAL,DPL
                MOV   SFCM,#0BH    ; Sector Erase
                NOP
                NOP
                NOP
                LCALL DONE
                RET

WRITEBYTE:      MOV   SFCF,#0C0H
                MOV   SFAH,DPH      ; DPTR is address of byte to be written
                MOV   SFAL,DPL
                MOV   SFDT,R4       ; R4 is the contents of byte
                MOV   SFCM,#0EH     ; Byte Program
                NOP
                NOP
                NOP
                LCALL DONE
                RET
```

```
DONE:       MOV   R0,#255       ; maximum time is 162ms for every command
LOADR1:     MOV   R1,#255       ; 637us
STATUS:     MOV   A,SFST
            JNB   ACC.2,READY   ; wait until Flash_Busy = 0
            DJNZ  R1,STATUS     ; 5 * 12 / 24 =2.5 us
            DJNZ  R0,LOADR1
            SETB  F0            ; F0 = 1 timeout of this operation
            RET                 ; F0 = PSW.5
READY:      CLR   F0
            RET
            END
```

附录二　Watchdog.asm 程序清单

```
WDTC    DATA  0C0H   ; Watchdog Timer Control Reg.
WDTD    DATA  86H    ; Watchdog Timer Data/Reload

        ORG  0000H
       LJMP  MAIN
       ORG  0100H
MAIN:  ANL  WDTC, #0F7H; Disable WDT during initialization
       MOV  WDTD, #val ; Load your interval value to WDTD
       ORL  WDTC, #8   ; Enable WDT reset
;-----------------------
       ORL  WDTC, #1    ; Start WDT
; ·····························add your main program here
;-----------------------
       ANL  WDTC, #0FEH  ; Stop WDT if you want
;-----------------------
       ORL  WDTC, #2      ; Refresh WDT before it resets MCU
;-----------------------
       ORL  WDTC, #4      ; Clear reset flag by WDT
; You can distinguish WDT reset from power-on reset
; by reading flag WDTC.3 = WDTS,1 is WDT reset,0 is power-on reset
       END
```

附录三　C51 头文件清单 SST89C5x.h

```
/*  BYTE Registers  */
sfr P0    = 0x80;
sfr P1    = 0x90;
sfr P2    = 0xA0;
sfr P3    = 0xB0;
sfr PSW   = 0xD0;
sfr ACC   = 0xE0;
sfr B     = 0xF0;
sfr SP    = 0x81;
sfr DPL   = 0x82;
sfr DPH   = 0x83;
sfr PCON  = 0x87;
sfr TCON  = 0x88;
sfr TMOD  = 0x89;
sfr TL0   = 0x8A;
sfr TL1   = 0x8B;
sfr TH0   = 0x8C;
sfr TH1   = 0x8D;
sfr IE    = 0xA8;
sfr IP    = 0xB8;
sfr SCON  = 0x98;
sfr SBUF  = 0x99;

sfr SFST  = 0XB6;     /* SST89C54/58 added SFRs defined here */
sfr SFCF  = 0XB1;
sfr SFCM  = 0XB2;
sfr SFDT  = 0xB5;
sfr SFAL  = 0xB3;
sfr SFAH  = 0XB4;

/*  8052 Extensions  */
sfr T2CON  = 0xC8;
sfr RCAP2L = 0xCA;
sfr RCAP2H = 0xCB;
sfr TL2   = 0xCC;
sfr TH2   = 0xCD;

/*  BIT Registers  */
/*  PSW  */
sbit CY    = 0xD7;
```

```
sbit AC    = 0xD6;
sbit F0    = 0xD5;
sbit RS1   = 0xD4;
sbit RS0   = 0xD3;
sbit OV    = 0xD2;
sbit F1    = 0xD1;
sbit P     = 0xD0;

/*  TCON  */
sbit TF1   = 0x8F;
sbit TR1   = 0x8E;
sbit TF0   = 0x8D;
sbit TR0   = 0x8C;
sbit IE1   = 0x8B;
sbit IT1   = 0x8A;
sbit IE0   = 0x89;
sbit IT0   = 0x88;

/*  IE  */
sbit EA    = 0xAF;
sbit ES    = 0xAC;
sbit ET1   = 0xAB;
sbit EX1   = 0xAA;
sbit ET0   = 0xA9;
sbit EX0   = 0xA8;

/*  IP  */
sbit PS    = 0xBC;
sbit PT1   = 0xBB;
sbit PX1   = 0xBA;
sbit PT0   = 0xB9;
sbit PX0   = 0xB8;

/*  P3  */
sbit RD    = 0xB7;
sbit WR    = 0xB6;
sbit T1    = 0xB5;
sbit T0    = 0xB4;
sbit INT1  = 0xB3;
sbit INT0  = 0xB2;
sbit TXD   = 0xB1;
sbit RXD   = 0xB0;

/*  SCON  */
```

```
sbit SM0   = 0x9F;
sbit SM1   = 0x9E;
sbit SM2   = 0x9D;
sbit REN   = 0x9C;
sbit TB8   = 0x9B;
sbit RB8   = 0x9A;
sbit TI    = 0x99;
sbit RI    = 0x98;

/*  8052 Extensions  */
/*  IE  */
sbit ET2   = 0xAD;

/*  IP  */
sbit PT2   = 0xBD;

/*  P1  */
sbit T2EX  = 0x91;
sbit T2    = 0x90;

/*  T2CON  */
sbit TF2   = 0xCF;
sbit EXF2  = 0xCE;
sbit RCLK  = 0xCD;
sbit TCLK  = 0xCC;
sbit EXEN2 = 0xCB;
sbit TR2   = 0xCA;
sbit C_T2  = 0xC9;
sbit CP_RL2= 0xC8;
```