W5500 Compliance Test Report

Version 1.0.0

http://www.wiznet.co.kr

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1.1 Overview

In the following section you will find the results of the test of the PHY IP test device[1].
Within this section, these devices shall be referred to as the Devices Under Test (DUT).
This document contains results of all tests from LAB TEST SPECIFICATION for 10 Base-T Rev.1.3.
Each test contains description of the test, list of captured data and pass/fail criteria.

Measurement was executed with scope Tektronix TDS754D with differential probe Tektronix P6246.
All tests are based upon the IEEE 802.3u and ANSI X3.263-1995 standards.

[1] The W5500 integrated the same IP which was used for the PHY IP test chip device which shows this test result.

1.2 Testing Summary

The following table summarizes the test results that are described in this document.

Test #	Test Name	Test RESULT
1.2.1	TP_IDL, silence duration and silence voltage	Pass
1.2.2	TD short circuit fault tolerance	Pass
1.2.3	Peak differential output voltage on TD circuit	Pass
1.2.4	Harmonic content, all ones (or all zeros) signal	Pass
1.2.5	Differential output waveform on the TD circuit with scaling of voltage template	Pass
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1.2.16	Link Test Pulses outside acceptance range	Pass
1.2.17	Link count max	Pass
1.2.18	Link fail effect on the transmit functions	Pass
1.2.19	Link fail effect on the receive functions	Pass
1.2.20	Transmit start-up bit loss	Pass
1.2.21	Transmit settling time	Pass
1.2.22	TD circuit common mode output voltage	Pass
1.2.23	PHY 10 Base-T dribble bit	Pass

1.2.1 TP_IDL, silence duration and silence voltage

1. Changes on Test set-up: No change to the setup that is described in the Test suites
2. Test Results:

Section 1:

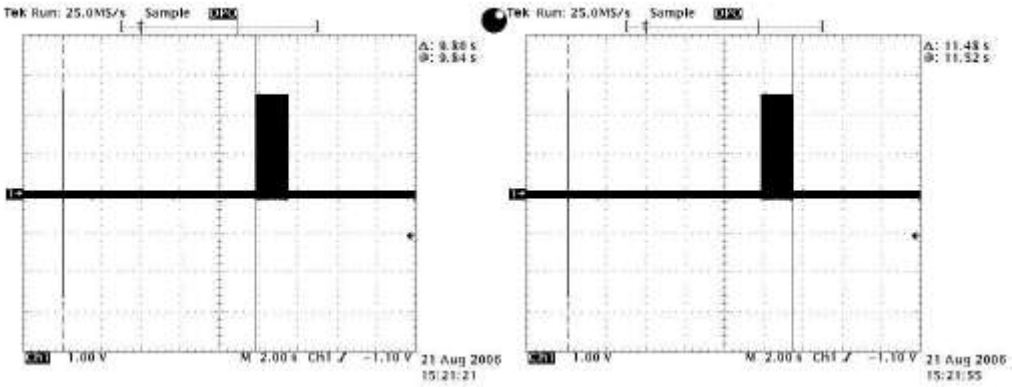

Figure 1 TP_IDL silence duration

The measured period of silence between the beginning of TP_IDL and link pulse was from 9.8mS to 11.48mS.

The period of silence (the time where differential voltage remains at 0±50mV) should be 16ms±8ms.

Conclusion: Section 1 of test passed.

Section 2.

The measured value period of silence between two capture consecutive link pulses was 11.48mS.

The period of silence (the time where differential voltage remains at 0±50mV) should be 16ms±8ms.

Conclusion: Section 2 of test passed.

Conclusion: **Test passed**

1.2.2 TD Short Circuit Fault Tolerance

1. Changes on Test set-up: No change to the setup that is described in the Test suite
2. Test Results: current on 1 Ohm,

Measurement N	1	2	3	4	5	6
Pos. amplitude current, mA	0.148	0.144	0.144	0.144	0.152	0.14
Neg. amplitude current (mA)	-0.176	-0.176	-0.168	-0.168	-0.164	-0.168

Table 1

Current should be less than 300mA.

Conclusion: **Test passed.**

1.2.3 Peak Differential Output Voltage on the TD Circuit

1. Changes on Test set-up: No change to the setup that is described in the Test suites.
2. Test procedure and Results:

Section 1: Smartbit transmits signal consisting of repeating frames of 512 bits of ALL Ones.

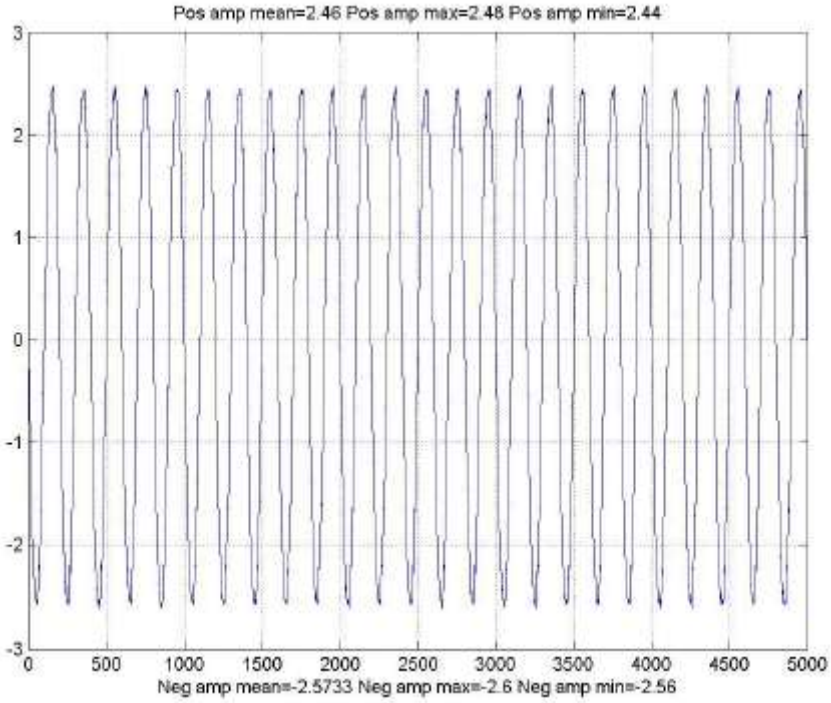

Figure 2 Transmitted signal – all ones

Amplitude was measured by scope while sourcing data from TD circuit, terminated with 100 Ohm resistive load and was shown in figure 2.

The measured peak differential voltage across the TD circuit should fall between 2.2 V and 2.8 V, and –2.2 and –2.8V for negative amplitude.

Conclusion: **Section 1 of test passed.**

Section 2: Smartbit transmits signal consisting of repeating frames of 512 bits of all fives data.

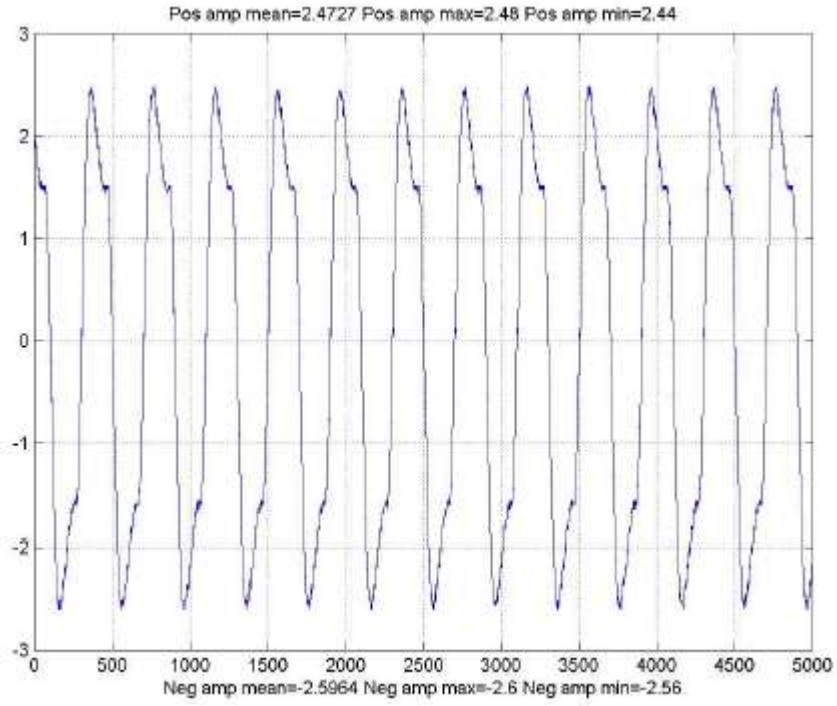

Figure 3 Transmitted signal – all fives

Amplitude was measured by scope while sourcing data from TD circuit, terminated with 100 Ohm resistive load and was shown in figure 3.

The measured peak differential voltage across the TD circuit should fall between 2.2 V and 2.8 V, and –2.2 and –2.8V for negative amplitude.

Conclusion: Section 2 of test passed

Conclusion**: Test passed**.

1.2.4 Harmonic Content, All Ones (or All Zeroes) Signal

1. Changes on Test set-up: No change to the setup that is described in the Test suites
2. Test procedure and Results:

The figure shows FFT of output signal for All Ones data signals.

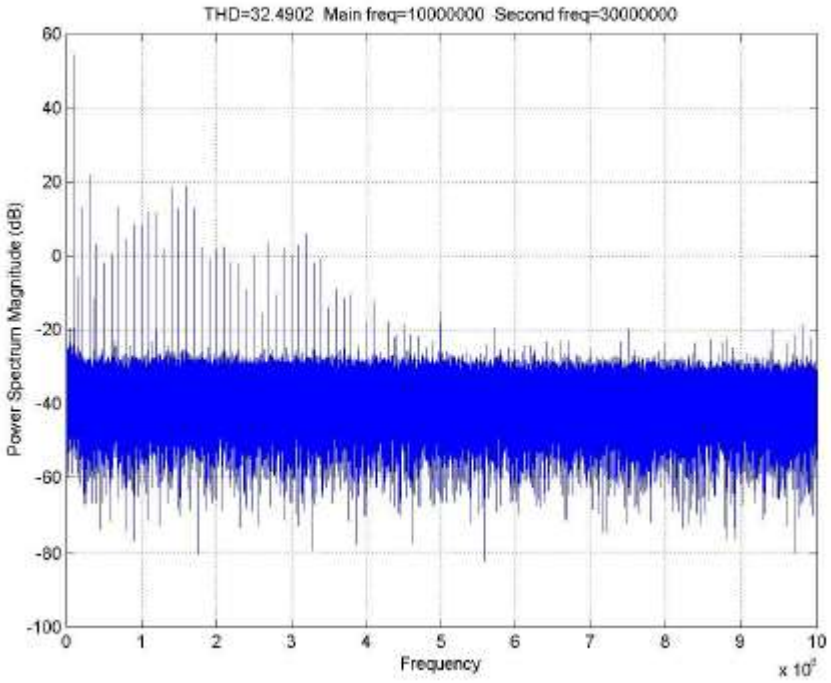

Figure 4 FFT of all one input signal

According to standard all of the harmonics shall be at least 27dB below the fundamental (10MHz).

It is harmonic that below of fundamental 32.49dB

Conclusion: **Test passed.**

1.2.5 Differential Output Waveform on the TD Circuit with Scaling of Voltage Template

1. Changes on Test set-up: No change to the setup that is described in the Test suites

2. Test procedure and Results:

2.1. Test was executed with TPM, terminated 100 Ohm.

2.2. Output waveform was captured by digital oscilloscope and transferred to Matlab and treat with script.

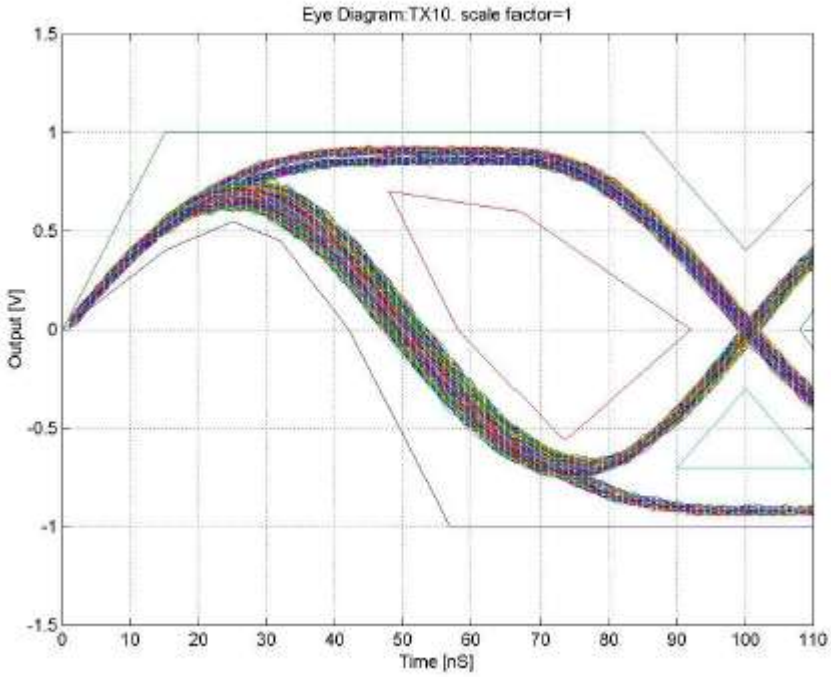

Figure 5 Eye pattern diagram

Eye diagram didn't cross template

Conclusion: **Test passed.**

1.2.6 Differential Output Waveform on the TD Circuit with Scaling of Voltage Template (inverted template)

1. Changes on Test set-up: No change to the setup that is described in the Test suites

2. Test procedure and Results:

2.1. Test was executed with TPM, terminated 100 Ohm.

2.2. Output waveform was captured by digital oscilloscope and transferred to Matlab and treat with script.

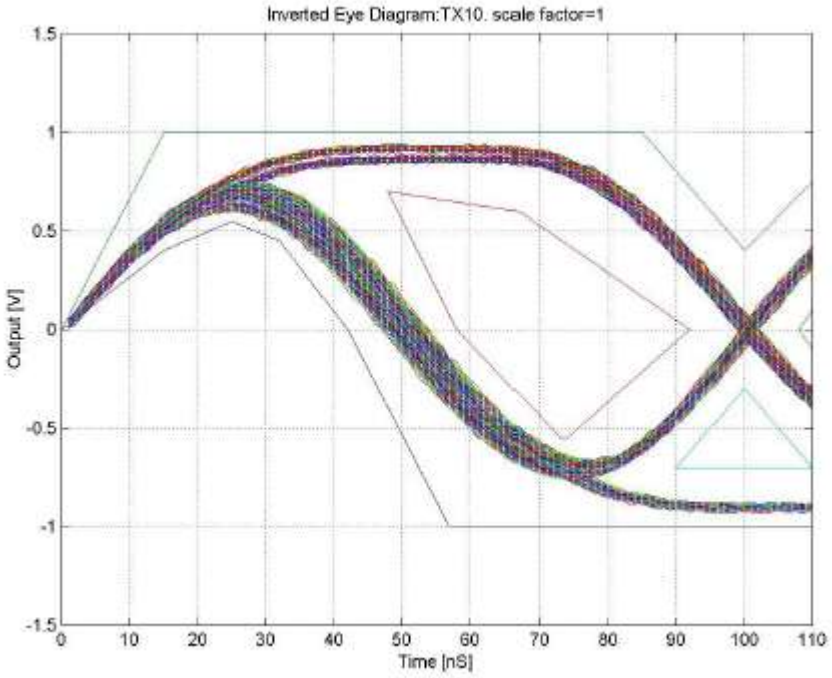

Figure 6 Invert eye pattern diagram

Eye diagram didn't cross template

Conclusion: **Test passed.**

1.2.7 Transmitter Waveform for Start of TP_IDL with specified loads, with and without the Twisted Pair

1. Changes on Test set-up: No change to the setup that is described in the Test suites.

2. Test procedure and Results:

2.1. Test was executed with four conditions measuring:

a. terminated with Load1, without twisted pair model (TPM);

b. terminated with Load1 and with TPM

c. terminated with Load2, without TPM

d. terminated with Load2 and with TPM

TP_IDLE waveform was captured by digital oscilloscope and transferred to Matlab to compare with the template.

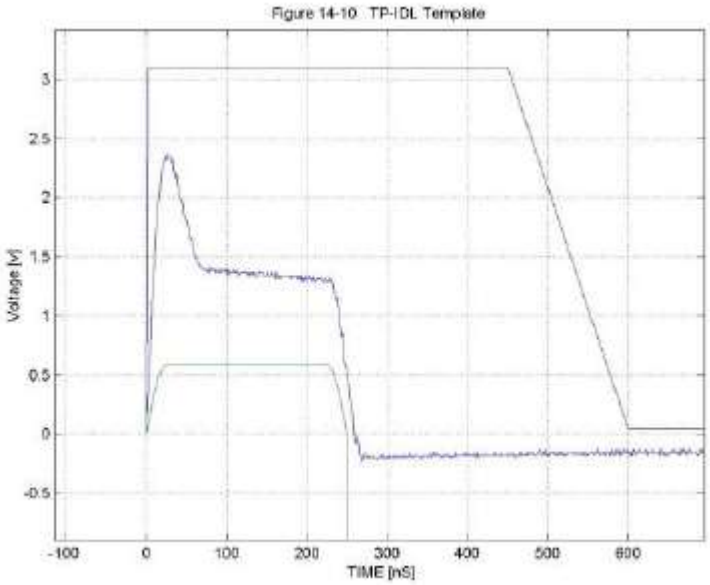

Figure 7 Termination Load1 without TPM

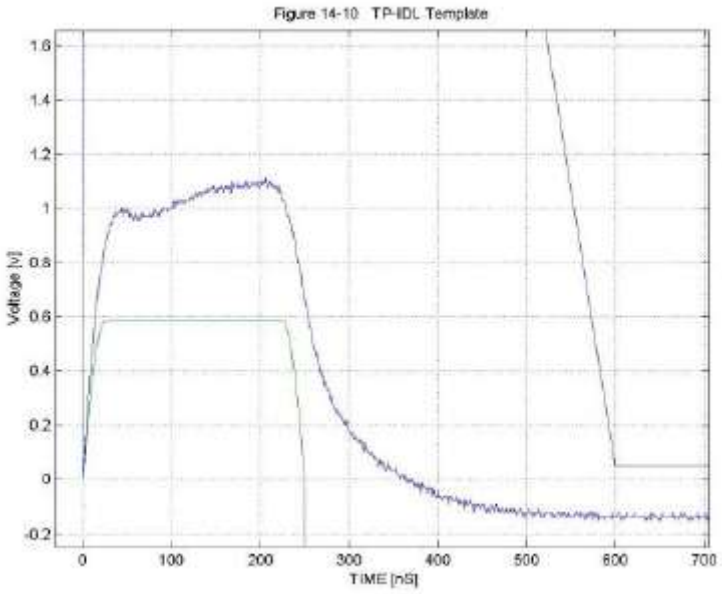

Figure 8 Termination Load1 with TPM

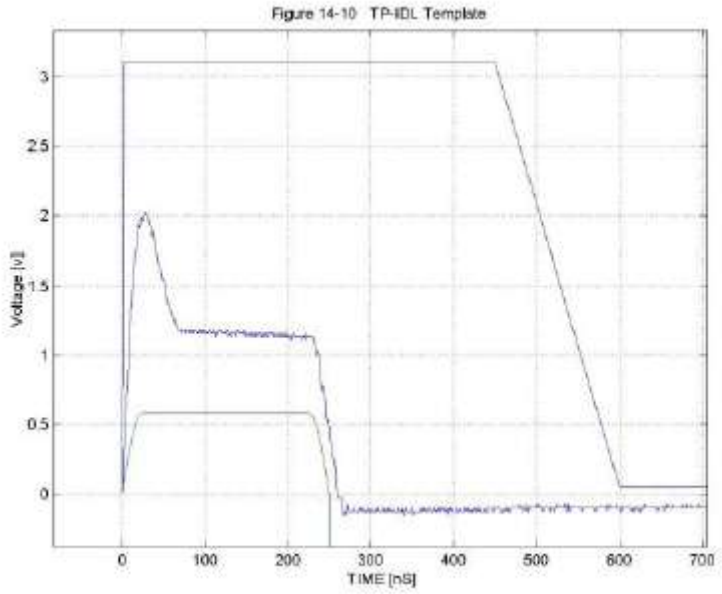

Figure 9 Termination Load2 without TPM

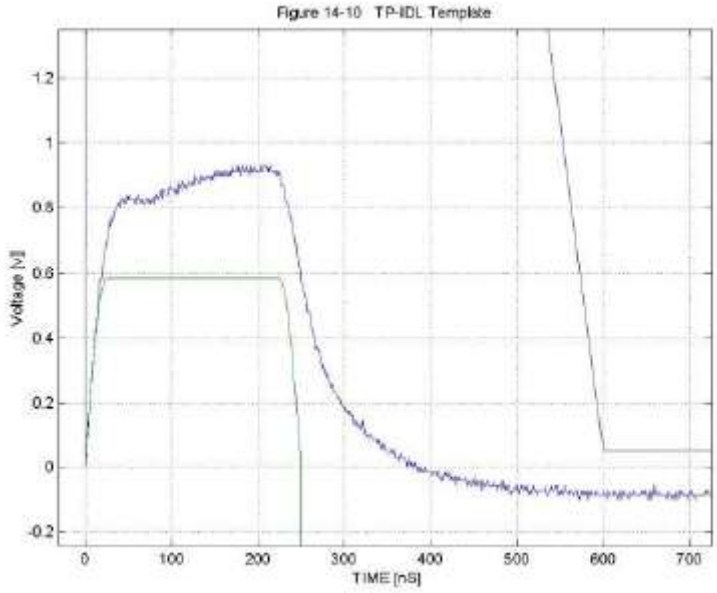

Figure 10 Termination Load2 with TPM

Conclusion: **Test Passed.**

1.2.8 Link Test Pulse Waveform, with Specified Loads, with and without TPM

1. Changes on Test set-up: No change to the setup that is described in the Test suites
2. Test procedure and Results:

Figure – Figure 15 show results of capture NLP signal for all type of load, described in standard.

All signals are inside of template.

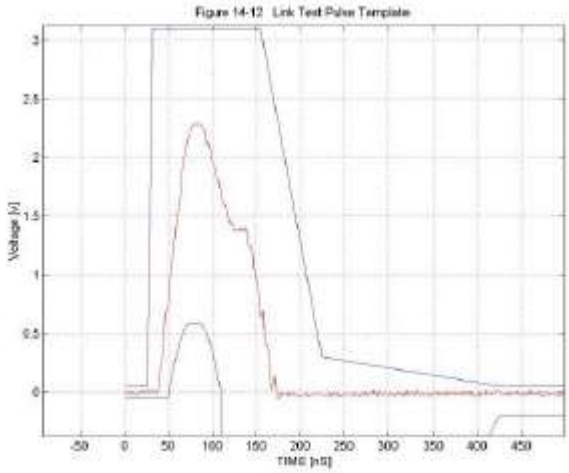

Figure 11 Output terminated with 100 Ohm

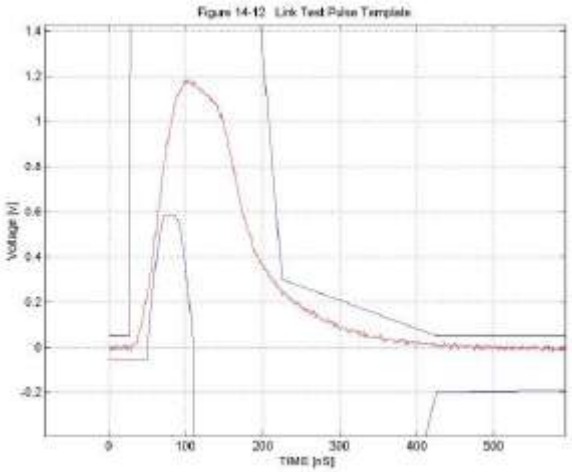

Figure 12 Output terminated TPM with 100 Ohm

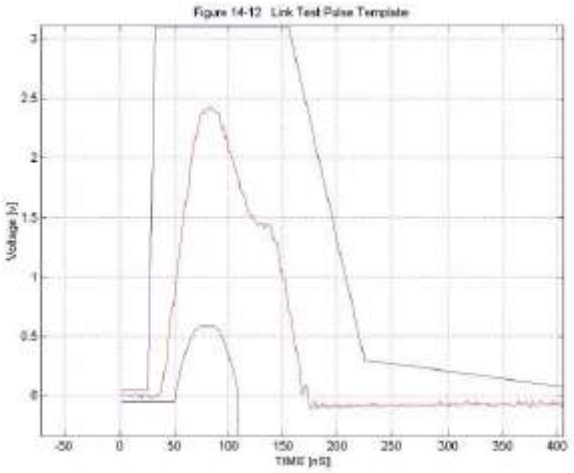

Figure 13 Output terminated with Load1

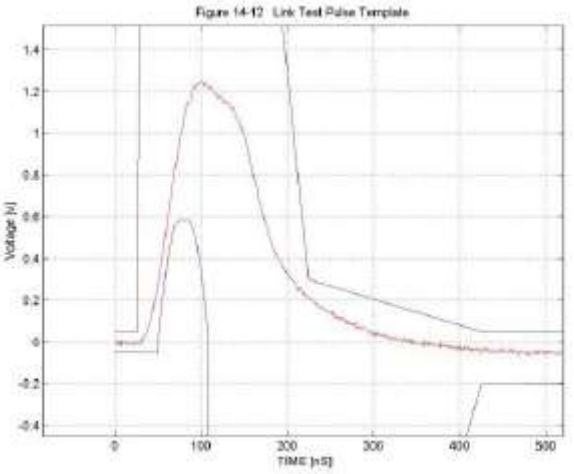

Figure 14 Output terminated TPM with Load1

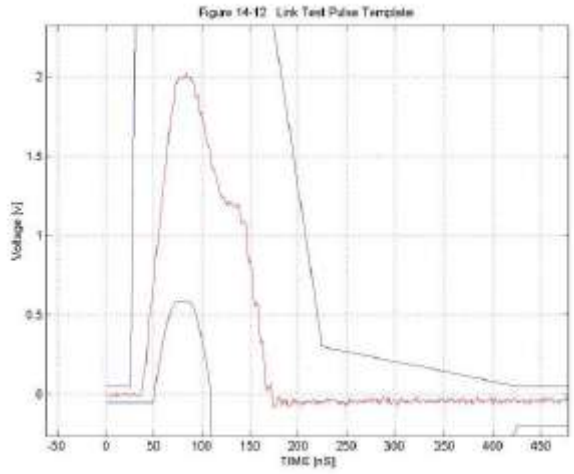

Figure 15 Output terminated with Load1

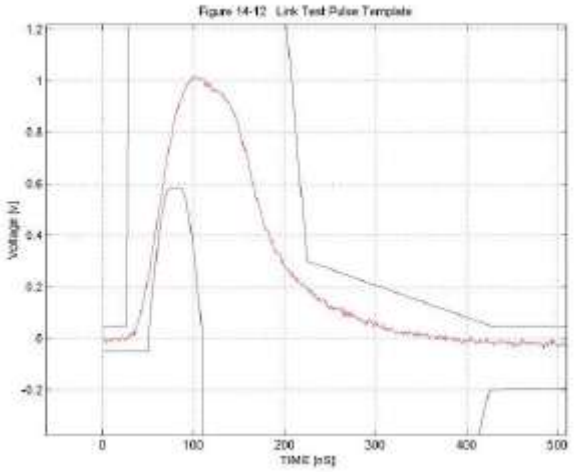

Figure 16 Output terminated TPM with Load1

Signals don't cross templates.

Conclusion: **Test passed.**

1.2.9 Transmitter Output Timing Jitter with Twisted Pair Model

1. Changes on Test set-up: No change to the setup that is described in the Test suites.
2. Test Results:

Maximum and minimum zero crossing were captured in points that shown in Table 2

8.0BT min(nS)	8.0BT max (nS)	8.5BT min (nS)	8.5BT max (nS)
795.4	802.0	846.4	852.9

Table 2

Zero crossings should occur at 8.0 BT+/-11nS (789-811) nS and 8.5 BT+/-11nS (839-861) nS after the triggering zero crossing.

Conclusion: **Test passed**

1.2.10 Transmitter Output Timing Jitter without Twisted Pair Model

1. Changes on Test set-up: No change to the setup that is described in the Test suites.
2. Test Results:

Maximum and minimum zero crossing were captured in points that shown in Table 3.

8.0BT min (nS)	8.0BT max (nS)	8.5BT min (nS)	8.5BT max (nS)
794.3	805.0	844.3	855.0

Table 3

Zero crossings should occur at 8.0 BT+/-20nS (780-820) nS and 8.5 BT+/-20nS (830-870) nS after the triggering zero crossing.

Conclusion: **Test passed**.

1.2.11 RD Circuit Short Circuit Fault Tolerance

1. Changes on Test set-up: No change to the setup that is described in the Test suites

2. Test Results:

The DUT performed normally for the remainder of the testing.

Conclusion: **Test passed.**

1.2.12 RD Circuit Signal Acceptance

1. Changes on Test set-up: No change to the setup that is described in the Test suite.
2. Test Results:

The DUT received the packets at both voltage levels without errors.

Conclusion: **Test passed.**

1.2.13 RD Circuit Link Test Pulse Acceptance

1. Changes on Test set-up: No change to the setup that is described in the Test suite. .

2. Test Results:

Results were represented in Table 4

11 NLPs were transmitted before the packet.

File Name	RCV Packets	Errors
NLP1_100frm.seq	100	0
NLP2_100frm.seq	100	0
NLP3_100frm.seq	100	0
NLP4_100frm.seq	100	0
NLP5_100frm.seq	100	0
NLP6_100frm.seq	100	0
NLP7_100frm.seq	100	0

Table 4

.

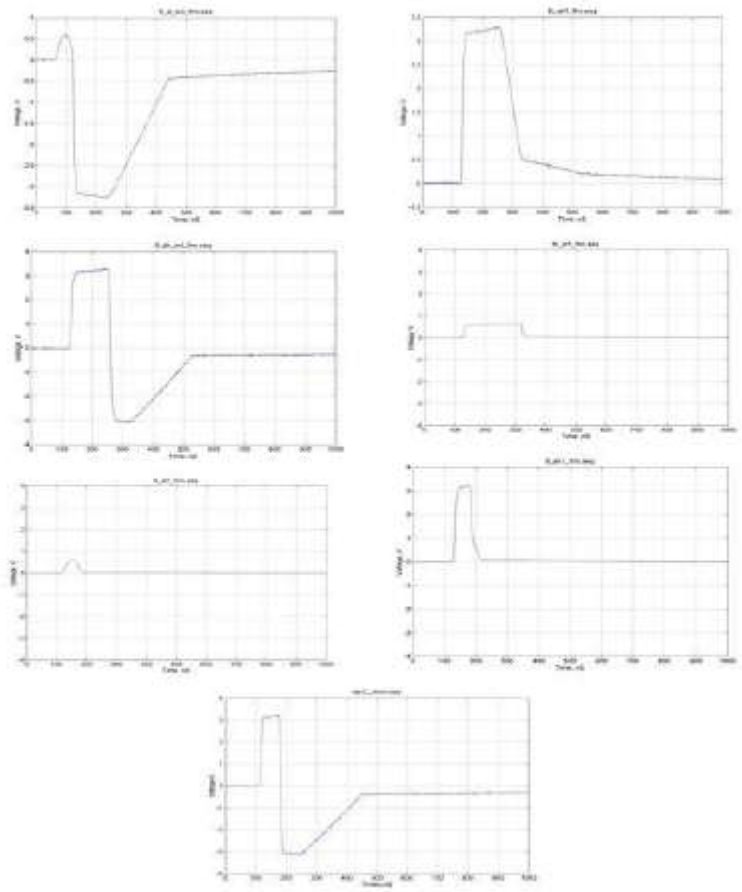

Figure 17 RD Circuit Link Test Pulse Acceptance test signals

The DUT accept all the packets in all the test signals

Conclusion: **Test passed.**

1.2.14 Range of Link Loss Timer

1. Changes on Test set-up:
2. Test procedure and Results: No change to the setup that is described in the Test suite.

Section 1

The DUT received the packet when the delay between the last NLP and the packet was 50ms.

Section 1 of test passed.

Section 2

The DUT didn't receive the packet when the delay between the last NLP and the packet was 150ms.

Section 2 of test passed.

Conclusion: **Test passed.**

1.2.15 Acceptance Range of Link Test Pulses

1. Changes on Test set-up: No change to the setup that is described in the Test suite.
2. Test Results:

Section 1

Data packets observed transmitted from DUT.

Section 1 of test passed.

Section 2

Data packets observed transmitted from DUT.

Section 2 of test passed.

Conclusion: **Test passed.**

1.2.16 Link Test Pulses Outside Acceptance Range (not in Link Test Pass state)

1. Changes on Test set-up: No change to the setup that is described in the Test suites.
2. Test Results:

Section 1

No data packets have observed transmitted from DUT.

Section 1 of test passed.

Section 2

No data packets have observed transmitted from DUT.

Section 1 of test passed.

Conclusion: **Test passed.**

1.2.17 Link Count Max

1. Changes on Test set-up: No change to the setup that is described in the Test suite.
2. Test Results:

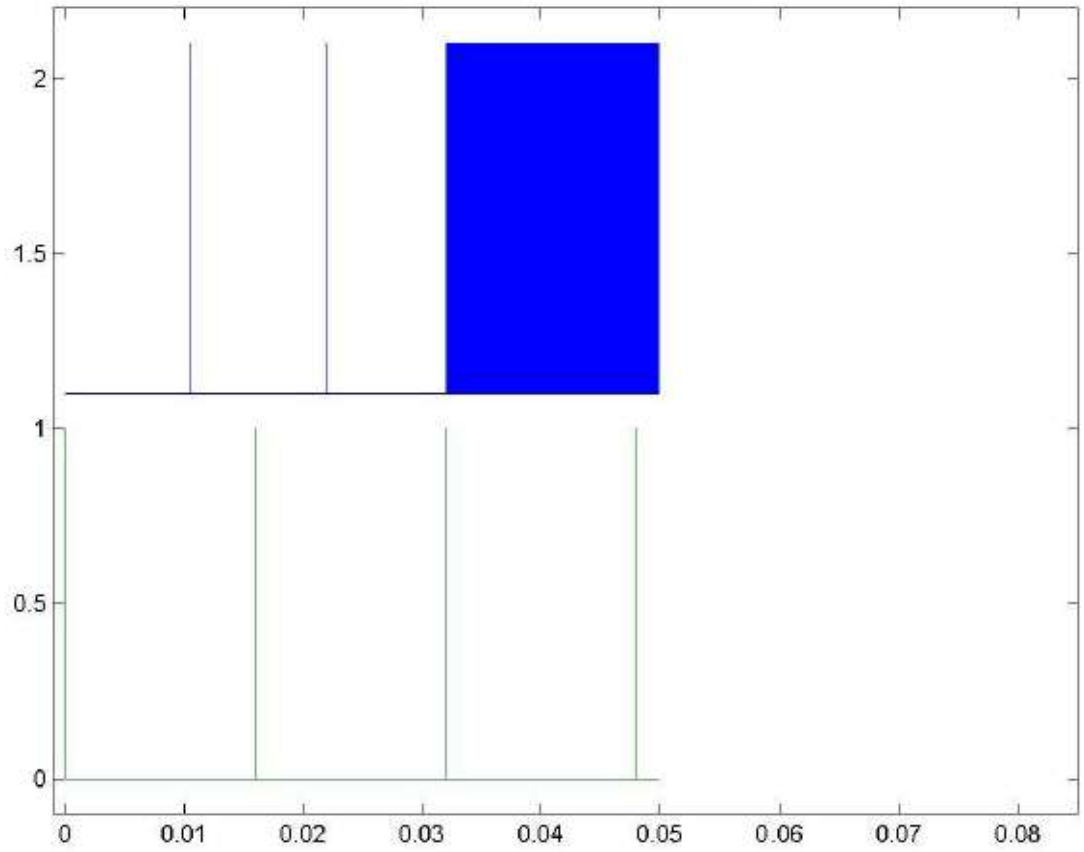

Figure 18 LC max

The DUT ceased NLP transmission and start to transmit data after receiving between 2 to 10 link test pulses.

Conclusion: **Test passed.**

1.2.18 Link Fail Effect on the Transmit Functions

1. Changes on Test set-up:

2. Test Results:

The TD circuit was transmitted NLP pulses only.

Conclusion: **Test passed**.

1.2.19 Link Fail Effect on the receive function

1. Changes on Test set-up: No change to the setup that is described in the Test suites.
2. Test Results:

DUT doesn’t accept the first packet in the series of two packets, but accept the second.
DUT doesn’t see any error frames.

Conclusion: **Test passed.**

1.2.20 Transmit start-up bit loss

1. Changes on Test set-up: No change to the setup that is described in the Test suites
2. Test Results:

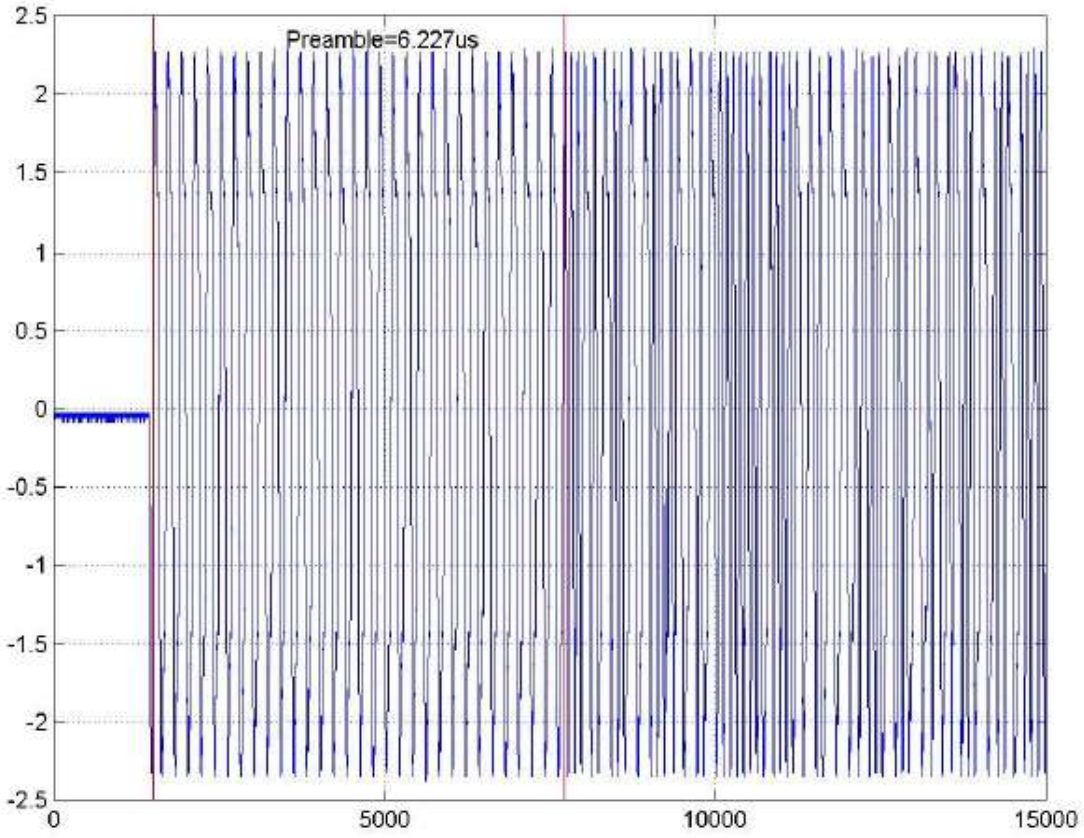

Figure 19 Preamble of packet

The time measured from the beginning of the packet to the end of SFD is 6.227 μS:

A pass shall be when the time between the first valid transition to the end of the SFD sequence is between 6.2 to 6.4μS.

Conclusion: **Test passed**.

1.2.21 Transmit settling time

1. Changes on Test set-up: No change to the setup that is described in the Test suites
2. Test Results:

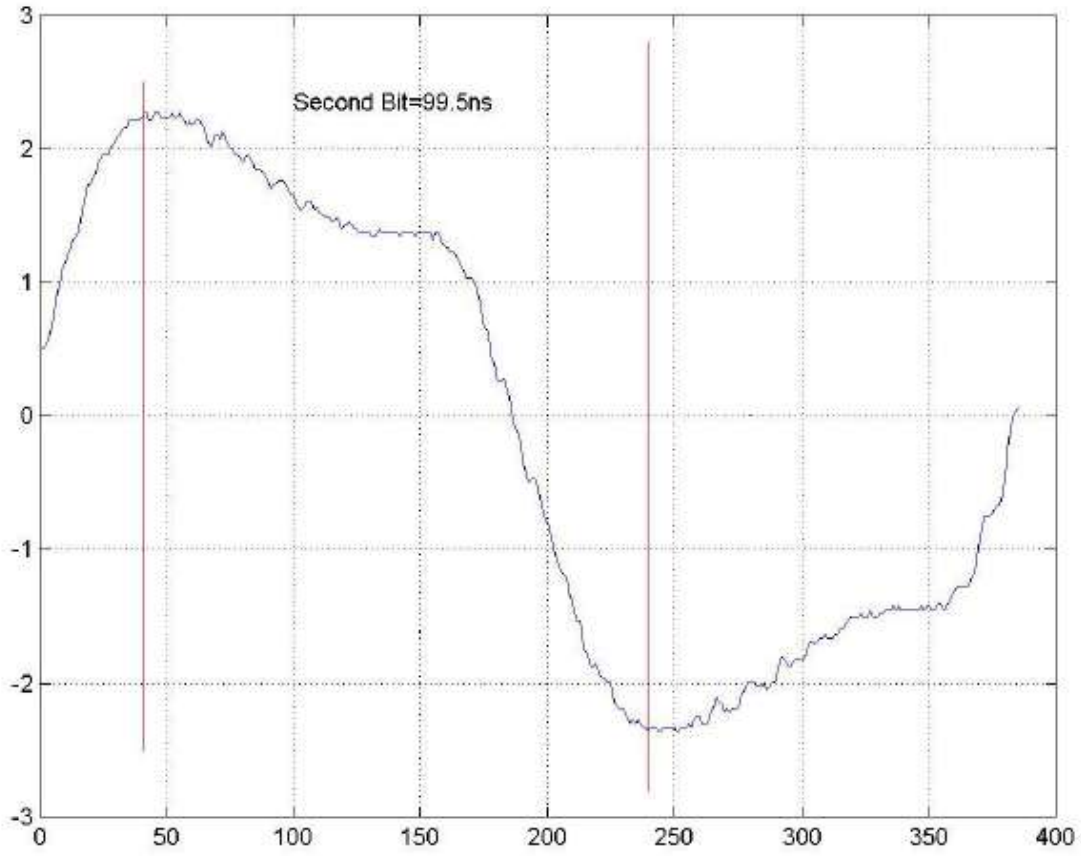

Figure 20 Transmit settling time

The timing of the second bit is 99.5nS as it should. Amplitude in second bit matched to standard requirement (should be 2.2V-2.8V).

Conclusion: **Test passed.**

1.2.22 TD circuit common-mode output voltage

1. Changes on Test set-up: The chip was sent signal consisting of repeating frames of 64 bytes of increase byte data
2. Test Results:

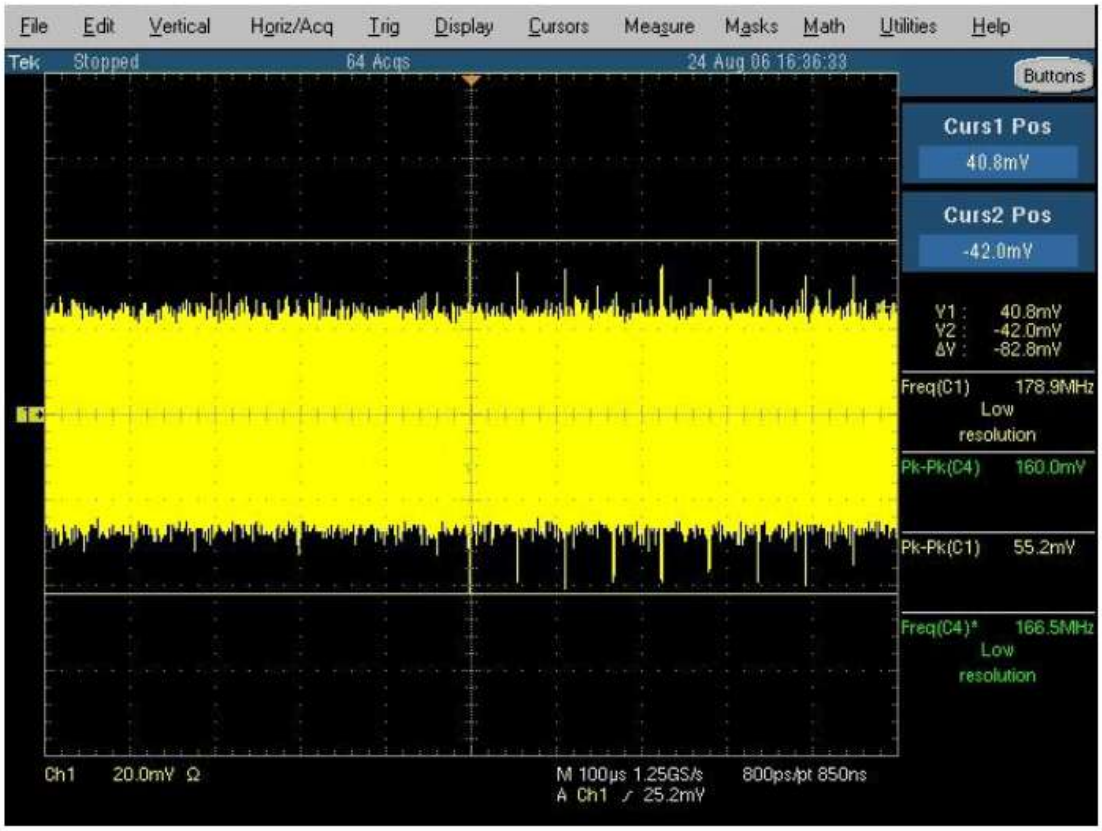

Figure 21 TD circuit common mode output voltage

Maximum measured common mode output voltage $E_{cm\ max}$= 40.8mV.

Minimum measured common mode output voltage $E_{cm\ min}$= -42mV.

The magnitude of the total common-mode output voltage of the transmitter, E_{cm} , measured as shown in Fig 21, is less than 50 mV peaks.

Conclusion: **Test Passed**.

1.2.23 PHY 10BASE-T Dribble Bit

1. Changes on Test set-up: No change to the setup that is described in the Test suite.
2. Test Results:

Test	Result	Expected result	Pass/fail
DRIB1	Normal	Normal	Pass
DRIB2	Normal	Normal	Pass
DRIB3	Normal	Normal	Pass
DRIB4	Alignment error	Alignment error	Pass
DRIB5	Alignment error	Alignment error	Pass
DRIB6	Alignment error	Alignment error	Pass
DRIB7	Alignment error	Alignment error	Pass
DRIB8	CRC error	CRC error	Pass

Table 5

DRIB1-DRIB8 tests passed

Conclusion: **Test passed.**

2 802.3 100Base-TX compliance tests

2.1 Overview

In the following section you will find the results of the test of the PHY IP test chip devices[2]. Within this section, these devices shall be referred to as the Devices Under Test (DUT). This document contains results of all tests from LAB TEST SPECIFICATION for 100 Base-T Rev.1.4.
Each test contains description of the test, list of captured data and pass/fail criteria.

Measurement was executed with scope Tektronix TDS754D with differential probe Tektronix P6246.
All tests are based upon the IEEE 802.3u and ANSI X3.263-1995 standards.

[2] W5500 integrated the same IP which was used for the PHY IP test chip device which shows this test result.

2.2 Testing Summary

- Use APB interface
- The following table summarizes the test results that are described in this document.

Test #	Test Name	Test RESULT
2.2.1	End of shell delimiter test	Pass
2.2.2	UTP Differential Output Voltage	Pass
2.2.3	Rise and Fall Times	Pass
2.2.4	Rise and fall times symmetry	Pass
2.2.5	Duty Cycle Distortion	Pass
2.2.6	Transmit Jitter	Pass
2.2.7	Waveform Overshoot	Pass
2.2.8	Adaptive equalization	Pass
2.2.9	Baseline Wander Correction	Pass
2.2.10	Bit Error Rate Verification	Pass
2.2.11	Differential output waveform on the twisted Pair Active Output Interface Template	Pass

2.2.1 End of shell delimiter test

1. Changes on Test set-up: No change to the setup that is described in the Test suite.
2. Test Results:

Section 1

The DUT received only one packet with one alignment error.

Section one passed.

Section 2

The DUT received all 32 packets without errors and SmartBit indicated them.

Section two passed.

Section 3

The DUT received 24 packets with error and SmartBit indicated 24 alignment errors and 24 CRC errors.

Section three passed.

3. Conclusion: **Test passed.**

2.2.2 UTP Differential Output Voltage

1. Changes on Test set-up: No change to the setup that is described in the Test suite

2. Test Results:

The test was executed 2 times (2 measurements).

The BandGap at these measurements was **1.216v**.

Measurement Num	Pos. ampl	Neg. ampl	Symmetry
1	0.9652	-0.9842	98.0621
2	0.9665	-0.9841	98.2110

Table 6 UTP Differential Output Voltage

Positive Vout value shall be between 950mV and 1050mV inclusive.

Negative Vout value shall be between -950mV and -1050mV inclusive.

The signal amplitude symmetry shall be between 98 and 102%.

3. Conclusion: **Test passed.**

2.2.3 Rise and Fall Times

1. Changes on Test set-up: No change to the setup that is described in the Test suite

2. Test Results:
The test was executed 5 times (5 measurements).

Figure 1 shows typical oscillogram of signal. This signal was used for measuring rise and fail time on segments AB, CD, EF and GH of oscillogram.

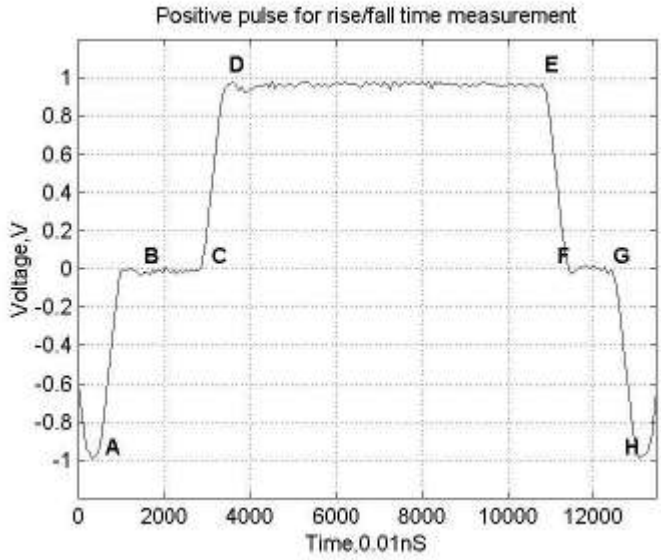

Figure 22 Measuring rise and fall time.

Results of measurements were shown in Table 7

Test number	Fall time [nS]	Rise time [nS]	Fall time [nS]	Rise time [nS]
	Segment AB	Segment CD	Segment EF	Segment GH
1	3.84	3.89	3.94	3.97
2	3.75	4.12	3.77	4.01
3	3.74	4.03	3.84	4.02
4	3.79	3.71	3.77	3.97
5	3.73	3.87	3.76	3.92

Table 7 Rise and fall times

Figure 23 shows typical oscillogram of signal opposite polarity. This signal was used for measuring rise and fail time on segments AB, CD, EF and GH of oscillogram opposite polarity.

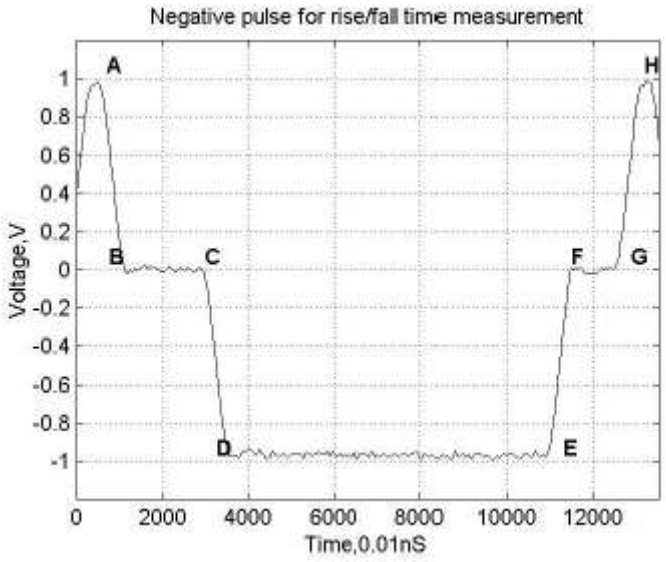

Figure 23 Measuring rise and fall time (opposite polarity).

Results of measurements were shown in Table 8

Test number	Fall time [nS]	Rise time [nS]	Fall time [nS]	Rise time [nS]
	Segment AB	Segment CD	Segment EF	Segment GH
1	3.78	4.07	3.85	3.98
2	3.78	3.79	3.82	3.93
3	4.00	4.12	3.86	4.02
4	3.85	4.09	3.84	3.84
5	3.88	3.98	3.77	4.06

Table 8 Rise and fall times-opposite polarity

According to test suite all measured rise and fall times shall be between 3ns and 5ns.

3. Conclusion: **Test passed.**

2.2.4 Rise and fall times symmetry

1. Changes on Test set-up: No change to the setup that is described in the Test suite

2. Test Results:

The test was executed 10 times (10 measurements).

Table 9 includes the results of Table 7 with addition of symmetry calculation.

The highlighted cells represent aberrant values.

The red highlighted cells are the average of the 10 measurements.

Test number	Fall time [nS] Segment AB	Rise time [nS] Segment CD	Fall time [nS] Segment EF	Rise time [nS] Segment GH	Symmetry
1	3.84	3.89	3.94	3.97	0.13
2	3.75	4.12	3.77	4.01	0.37
3	3.74	4.03	3.84	4.02	0.29
4	3.79	3.71	3.77	3.97	0.26
5	3.73	3.87	3.76	3.92	0.19

Table 9 Rise times, fall times and symmetry

Table 10 includes the results of Table 8 with addition of symmetry calculation.

Test number	Fall time [nS] Segment AB	Rise time [nS] Segment CD	Fall time [nS] Segment EF	Rise time [nS] Segment GH	Symmetry
1	3.78	4.07	3.85	3.98	0.29
2	3.78	3.79	3.82	3.93	0.15
3	4.00	4.12	3.86	4.02	0.26
4	3.85	4.09	3.84	3.84	0.25
5	3.88	3.98	3.77	4.06	0.29

Table 10 Rise times, fall times and symmetry-opposite polarity

According to test suite rise and fall time symmetry shall not exceed 0.5nS.

3. Conclusion: **Test passed.**

2.2.5 Duty Cycle Distortion

1. Changes on Test set-up: No change to the setup that is described in the Test suite

2. Test Results:

Figure 24 shows sample of oscillogram for calculation Duty Cycle Distortion (DCD).

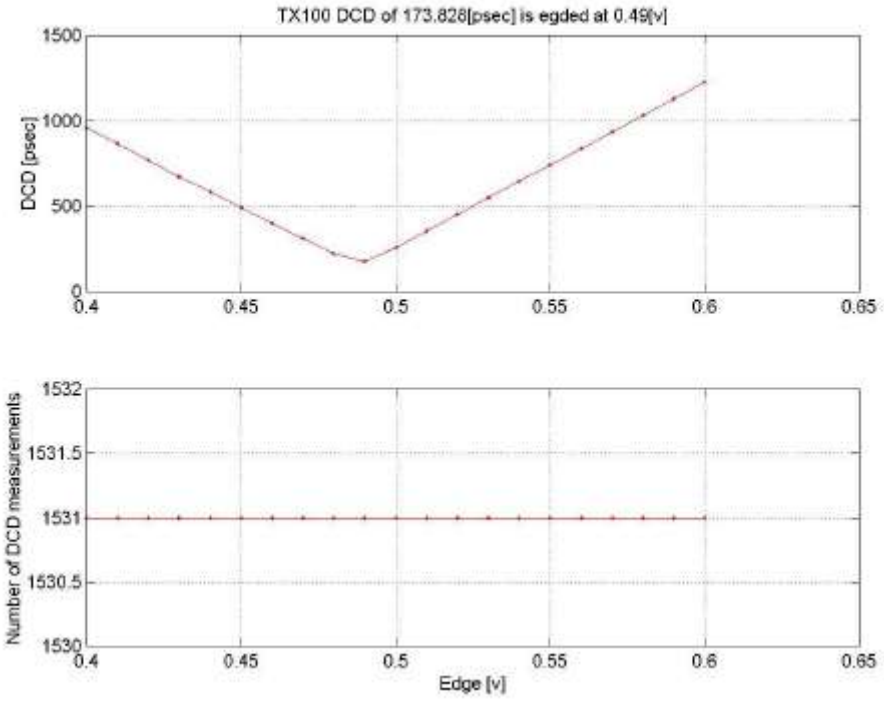

Figure 24 Oscillogram for measuring DCD.

For the DCD test, 1531 subsequences were analyzed, all of them had passed.

The maximum DCD at 0.49v was 173.82ps

3. Conclusion: **Test passed**

2.2.6 Transmit Jitter

1. Changes on Test set-up: No change to the setup that is described in the Test suite
2. Test Results:

Figures 25 and 26 shows persistence of signal.

The max jitter is 980ps

Figure 25 Jitter when trigger is 0.5v.

Figure 26 Jitter when trigger is -0.5v.

According to standard peak-to-peak transmit jitter shall not exceed 1.4nS.

3. Conclusion: **Test passed.**

2.2.7 Waveform Overshoot

1. Changes on Test set-up: No change to the setup that is described in the Test suite
2. Test Results:

The maximum overshoot is 1.3913%.

3. Conclusion: **Test passed**

2.2.8 Adaptive equalization

1. Changes on Test set-up: No change to the setup that is described in the Test suite

2. Test results:

Test_Name	Length,m	RcvGoodPkt	CRCErr	AlignErr	Oversize	Undersize
test_25.2.2_hitr	test_25.2.2_hitr	0	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	5	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	10	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	15	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	20	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	25	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	30	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	35	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	40	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	45	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	50	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	55	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	60	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	65	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	70	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	75	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	80	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	85	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	90	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	95	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	100	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	105	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	110	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	115	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	120	500000	0	0	0
test_25.2.2_hitr	test_25.2.2_hitr	125	499709	291	0	0
test_25.2.2_lotr	test_25.2.2_lotr	0	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	5	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	10	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	15	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	20	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	25	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	30	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	35	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	40	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	45	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	50	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	55	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	60	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	65	500000	0	0	0

test_25.2.2_lotr	test_25.2.2_lotr	70	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	75	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	80	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	85	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	90	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	95	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	100	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	105	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	110	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	115	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	120	500000	0	0	0
test_25.2.2_lotr	test_25.2.2_lotr	125	500000	0	0	0

Table 11 Adaptive equalization

3. Conclusion: **Test passed.**

2.2.9 Baseline Wander Correction

1. Changes on Test set-up: No change to the setup that is described in the Test suite

2. Test Results:

Test_Name	Length	RcvGoodPkt	CRCErr	AlignErr	Oversize	Undersize
Section 1						
test_25.2.3_bi_hitr	0meters	20000	0	0	0	0
test_25.2.3_bi_hitr	80meters	20000	0	0	0	0
test_25.2.3_bi_hitr	100meters	20000	0	0	0	0
Conclusion: Section 1 passed						
Section 2						
test_25.2.3_bi_lotr	0meters	20000	0	0	0	0
test_25.2.3_bi_lotr	80meters	20000	0	0	0	0
test_25.2.3_bi_lotr	100meters	20000	0	0	0	0
Conclusion: Section 2 passed						
Section 3						
test_25.2.3_uni_hitr	0meters	20000	0	0	0	0
test_25.2.3_uni_hitr	80meters	20000	0	0	0	0
test_25.2.3_uni_hitr	100meters	20000	0	0	0	0
Conclusion: Section 3 passed						
Section 4						
test_25.2.3_uni_lotr	0meters	20005	0	0	0	0
test_25.2.3_uni_lotr	80meters	20005	0	0	0	0
test_25.2.3_uni_lotr	100meters	20005	0	0	0	0
Conclusion: Section 4 passed						

Table 12 Baseline wander correction

According to test suite there shell be no more than 7 errors for any iteration.

3. Conclusion: **Test passed.**

2.2.10 Bit Error Rate Verification

1. Changes on Test set-up: No change to the setup that is described in the Test suite

2. Test Results:

Test_Name	Length	RcvGoodPkt	CRCErr	AlignErr	Oversize	Undersize
Section 1						
test_25.2.4_hitr	75meters	20000000	0	0	0	0
test_25.2.4_hitr	100meters	20000000	0	0	0	0
Conclusion: Section 1 passed						
Section 2						
test_25.2.4_lotr	75meters	20000000	0	0	0	0
test_25.2.4_lotr	100meters	20000000	0	0	0	0
Conclusion: Section 2 passed						

Table 13 Bit error rate verification

According to test suite there shell be no more than 7 errors for any iteration.

3. Conclusion: **Test passed.**

2.2.11 Differential output waveform on the twisted Pair Active Output Interface Template

1. Changes on Test set-up: No change to the setup that is described in the Test suite

2. Test Results:

Figure 6 shows eye diagrams with scaling of twisted pair output template for TX 100BASE-T output signal.

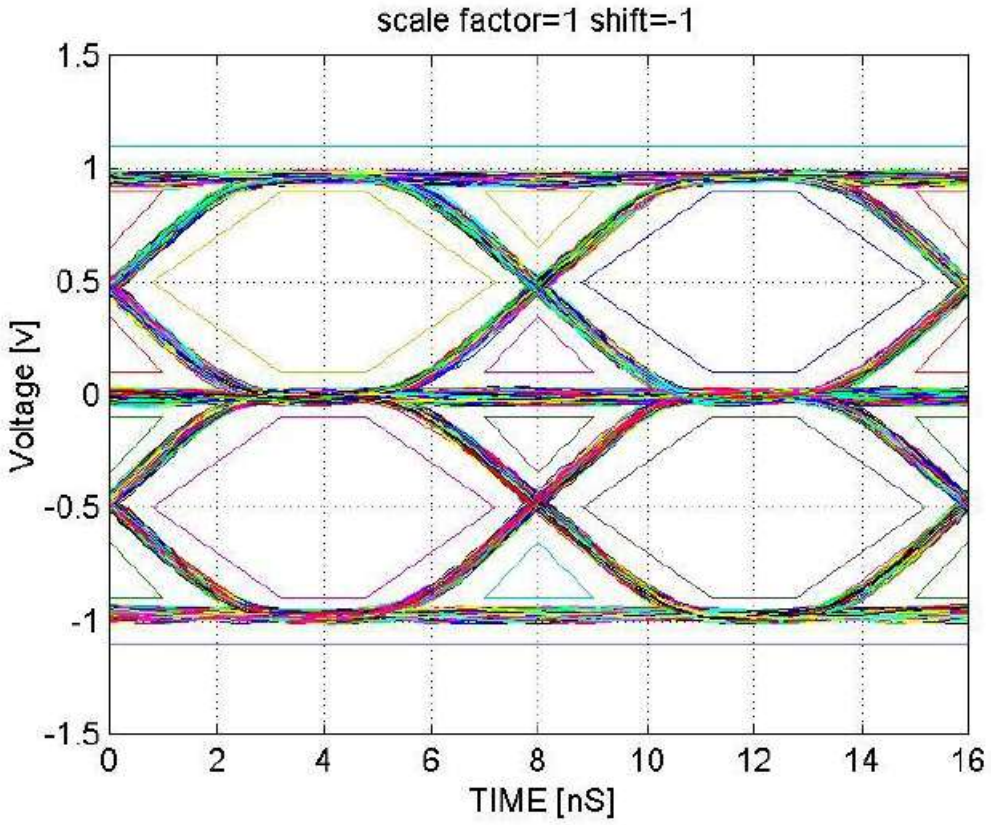

Figure 27 Eye diagram

Eye diagram doesn't cross template.

Conclusion: **Test passed.**

Document History Information

Version	Date	Descriptions
Ver. 1.0.0	26MAR2015	Initial Release

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