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Paul C. Davis (S'60-M'61) was born in Glenville, W. Va., on March 14, 1937. He received the B.S.E.E. degree from West Virginia University, Morgantown, in 1959, the M.S. degree from Massachusetts Institute of Technology, Cambridge, in 1961, and the Ph.D. degree in electrical engineering from Lehigh University, Bethlehem, Pa., in 1968

He has been a Teaching Assistant at M.I.T. and served two years as an army

officer in the Ordnance Guided Missile School, Huntsville, Ala. In 1962 he became a Member of the Technical Staff, Bell Laboratories, Reading, Pa. He has been engaged in characterization and modeling of transistors and in the design of linear and digital integrated circuitry.

Dr. Davis is a member of Eta Kappa Nu and Tau Beta Pi, and an associate member of Sigma Xi.



Stanley F. Moyer was born in Hamburg, Pa., on September 8, 1931. He graduated from Capitol Radio Engineering Institute, Washington, D.C. in 1956. He has also attended Albright College, Reading, Pa., and Lafayette College, Easton, Pa.

In 1956 he joined Bell Laboratories, Reading, Pa., where he has worked on the development of germanium diffused base transistors, silicon transistors, and field-effect transistors. Since 1966, he has worked

on the development of silicon monolithic integrated circuits.



Veikko R. Saari was born in Brooklyn, N.Y., on April 24, 1928. He received the B.S. and M.S. degrees in physics from the University of Minnesota, Minneapolis, in 1951 and 1956, respectively.

Since 1956 he has been working on the design of solid-state circuits at Bell Laboratories, Holmdel, N.J.

Mr. Saari is a member of the American Association of Physics Teachers.

Relationship Between Frequency Response and Settling Time of Operational Amplifiers

B. YESHWANT KAMATH, STUDENT MEMBER, IEEE, ROBERT G. MEYER, MEMBER, IEEE, AND PAUL R. GRAY, MEMBER, IEEE

Abstract—The effects of pole-zero pairs (doublets) on the frequency response and settling time of operational amplifiers are explored using analytical techniques and computer simulation. It is shown that doublets which produce only minor changes in circuit frequency response can produce major changes in settling time. The importance of doublet spacing and frequency are examined. It is shown that settling time always improves as doublet spacing is reduced whereas the effect of doublet frequency is different for 0.1 and 0.01 percent error bands. Finally it is shown that simple analytical formulas can be used to estimate the influence of frequency doublets on amplifier settling time.

I. Introduction

N MANY applications of operational amplifiers, the settling time is an important parameter [1]. The settling time is the time taken for the output of the amplifier to settle to within 0.1 or 0.01 percent after the

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The authors are with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, Calif. 94720.

application of an input step. This test is usually done in a unity-gain configuration with a 10-V step input and thus the error bands on the output are 10 and 1 mV, respectively, for 0.1 and 0.01 percent accuracy. These tests are important in specifying the operational amplifier for use in such applications as A/D and D/A converters.

The settling time of an amplifier is composed of two distinct periods [1]. The first period is called the slew time during which the amplifier output makes the transition from the original output voltage to the vicinity of the new value. During this period the amplifier acts in a grossly nonlinear fashion and the length of this period is generally determined by the current available to charge the amplifier compensation capacitance. The second portion of the settling time is the period after slew limiting when the amplifier output is near its final value and the circuit acts in a quasi-linear fashion. It has been shown [2], [3] that this period is significantly affected by the presence of pole-zero pairs (called doublets) in the amplifier transfer function. In high-speed operational amplifiers, the slew time can be very short and this second

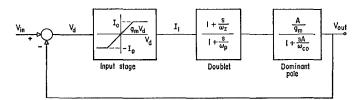


Fig. 1. Operational amplifier model for calculation of transient response.

period in the quasi-linear region can dominate the settling time of the amplifier.

The circuit behavior described above is difficult to evaluate in practice. Direct measurements of these aspects of amplifier performance are difficult to perform and the effects of different parameters in the circuit are difficult to isolate. In this paper the effect of doublets on the frequency response and settling time of a fast operational amplifier is investigated using analytical techniques and computer simulation.

II. THEORY

Doublets in an amplifier transfer function can arise from a number of causes. For example, bypassing one side of an active load at high frequencies [4] leads to the introduction of a pole-zero pair with an octave separation. The use of a feedforward capacitor to bypass a lateral p-n-p transistor [2] can cause the creation of a doublet with ± 30 percent mismatch between pole and zero frequencies.

Previous analyses of the effects of a doublet have assumed linear operation of the circuit in question [1]-[3]. However, the application of a 10-V step to an operational amplifier results in quite nonlinear operation during the slewing period, and a linear analysis cannot be justified for this case. A model which represents the situation in a practical amplifier is shown in Fig. 1. The amplifier is connected in a unity-gain feedback loop. The differential input stage is modeled as shown with maximum available current I_0 and a transfer characteristic slope of g_m for values of $\left|V_d\right|$ less than (I_0/g_m) . For values of $|V_d| > (I_0/g_m)$, the input stage limits at a current I_0 . This is the major source of nonlinearity in the circuit during the transient response. A doublet is assumed present in the amplifier frequency response together with the dominant pole produced by the compensation capacitor. These are shown schematically in Fig. 1. Since this portion of the circuit is assumed to act linearly, the precise details of the circuit arrangement are not critical. However, to conform to the practical example considered later, a current I_1 is assumed fed from the input stage to the circuit producing the doublet, and a current I_2 is assumed fed from this circuit to the output. The use of voltage variables does not change the results of the analysis.

In this analysis, the higher frequency poles near and beyond crossover have been neglected. These poles are certainly important since they limit the bandwidth and slew rate of the amplifier through the compensation capacitor. They can also have a very strong effect on settling time if the phase margin is allowed to become too small. However, in an optimum design, these poles will produce only a slightly underdamped response, and this response will be short in duration compared to the transients introduced by the doublet. A closely spaced doublet is assumed and the doublet frequency is assumed much less than the amplifier unity-gain frequency.

The circuit of Fig. 1 is analyzed in the Appendix where it is shown that the response to a step input of amplitude V is:

$$V_{\text{out}}(t) \simeq V(1 - k_1 \exp[-\omega_{co}t] + k_2 \exp[-(t/\tau_2)]),$$

for $t > T_s$ (1)

where

$$k_2 \simeq \frac{\omega_z - \omega_p}{\omega_{co}} \tag{2}$$

$$au_2 \simeq \frac{1}{\omega_z}$$
 (3)

 T_s slewing period

 ω_z doublet zero frequency

 ω_p doublet pole frequency

 ω_{eo} $A \times \text{(amplifier dominant pole)} \simeq \text{unity-gain bandwidth}$

A open-loop low frequency gain.

Equation (1) indicates the presence of a slow settling component in the output with a time constant $(1/\omega_z)$ and a magnitude k_2V . Equation (2) indicates that for a given fractional doublet spacing (for example, $\omega_z = 1.3 \omega_p$) the magnitude of the slow settling component is proportional to the doublet frequency, and the magnitude of the input step. However, (3) indicates that the time constant of the slow settling component is inversely proportional to the doublet frequency. Thus lower frequency doublets will give a response which persists for a longer period but with a smaller amplitude. Higher frequency doublets will give a response which dies out faster but has a larger amplitude. The relative importance of these trends will depend on the particular situation. If settling to 0.1 percent only is important, a lower frequency doublet may give a slow-settling component which is always within the error band and thus does not degrade performance. For settling to 0.01 percent the same doublet may cause great increases in settling time. A higher frequency doublet is likely to produce settling time degradation in all cases but its effect will die away much sooner [3].

III. COMPUTER SIMULATION

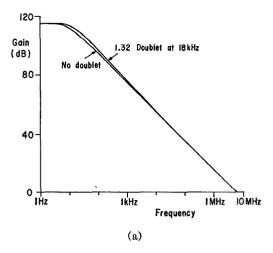
The analytical expressions derived above use a greatly simplified model of the operational amplifier. In order to check the validity of these approximations and to further investigate these effects, computer simulations were performed on the μ A 772 operational amplifier [2]. This amplifier was chosen because it is a high speed amplifier with a fast settling time and the effects of

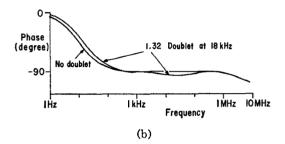
artificially introduced doublets are easy to distinguish. The amplifier itself has a doublet due to the use of feedforward but a doublet compression scheme which is an integral part of the amplifier makes the effect of this doublet undetectable. In order to observe the effect of a doublet on the response of the amplifier, one half of the active load was bypassed with a capacitor in a similar fashion to the LM 118 [4]. By varying the magnitude of the capacitor and a resistor in series with it, doublets were introduced at different frequencies with different pole-zero separations. The open-loop unity-gain frequency was kept constant in all cases at $\omega_{co} = 6.1 \text{ MHz}$ by small adjustments in the value of the compensation capacitor. The compensation capacitor used was larger than the one in the original μA 772 to allow for these adjustments.

The program used was the SPICE program developed at the University of California, Berkeley, spice has a general nonlinear transient analysis capability with comprehensive large-signal device models. The computed open-loop gain and phase response for the basic amplifier are shown in Fig. 2(a) and (b) together with the response when a doublet at 18 kHz is included. Even with the addition of such a doublet with 32 percent mismatch between pole and zero frequencies, the change in the frequency response is small. For a smaller doublet (such as 8 percent pole-zero mismatch) the effect on frequency response is indiscernable on these scales. In Fig. 2(c) an expanded graph is shown of phase versus frequency for the amplifier with and without doublets. The doublets used here were at 18 kHz with pole-zero mismatches of 32, 20, and 8 percent. It is apparent that the 8 percent doublet has very little effect on the frequency response, but it will be shown to have a significant effect on the settling time.

In Fig. 3(a) the computed transient response is shown with a 10-V input step (-5 to +5 V) for the original circuit in a unity-gain voltage follower configuration. On this scale, the addition of doublets produces an almost imperceptible change in response. In Fig. 3(b), this response is shown on an expanded scale to allow observation of 0.1 percent (10 mV) settling time. This is seen to be about 0.43 μ s for the case of no doublet, with about 0.2 μ s of this being slewing time and the rest being caused by overshoot. Because of the neglect of higher frequency poles, this overshoot is not predicted by the analysis in the Appendix.

Also shown in Fig. 3(b) are response curves with doublets added to the amplifier. It is apparent that the doublet at 180 kHz with 32 percent spacing produces the worst degradation of settling time with a value of 1.56 μ s. The 32 percent doublet at 18 kHz gives a settling time of 0.80 μ s, even though it persists much longer due to its longer time constant. The much smaller initial value of the slow settling component due to the 18 kHz doublet results in its decaying below 10 mV sooner than is the case for the 180 kHz doublet.





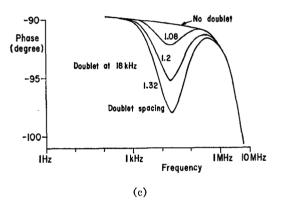


Fig. 2. Computed open-loop frequency response of the amplifier with and without doublets. (a) Gain versus frequency. (b) Phase versus frequency. (c) Expanded phase versus frequency.

The graphs of Fig. 3(b) are shown even further expanded in Fig. 3(c) so that 0.01 percent (1 mV) settling times can be determined. In this case, for any given fractional doublet spacing, the lower frequency doublet has by far the worst effect on settling time. This possibility was pointed out in Section II. Even though the higher frequency doublets give larger initial amplitudes of the slow settling component, the very slow decay for the lower frequency doublets makes them much more significant for 1-mV settling time. The worst case is for the 32 percent doublet separation at a frequency of 18 kHz giving a 1-mV settling time of 14.14 μ s.

These results are illustrated in Fig. 4 where computed settling times are shown as a function of doublet spacing

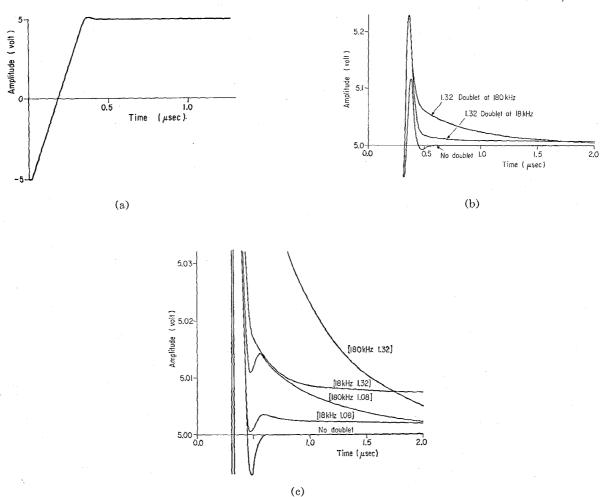


Fig. 3. Computed unity-gain transient response of the amplifier to a 10-V input step from -5 to +5 V. (a) Linear voltage scale. (b) and (c) Expanded voltage scale.

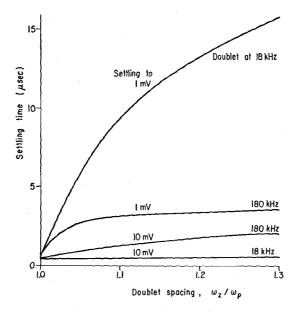


Fig. 4. Computed unity gain settling time versus doublet spacing for two different doublet frequencies and settling accuracies. Input step from -5 to +5 V.

TABLE I

	Doublet Spacing	$ au_2 \ (\mu \mathrm{S})$		$rac{k_2 {V}_2}{({ m mV})}$		10-mV Settling Time (μs)		1-mV Settling Time (μs)	
		computer	predicted	computer	predicted	computer	predicted	computer	predicted
Doublet at	1.08	8.09	8.14	2.46	2.28	0.44	0.47	7.3	6.7
18 kHz	1.2	6.53	7.29	$6.\overline{25}$	5.81	0.48	0.51	12.0	12.8
	1.32	6.15	6.88	9.97	9.19	0.80	0.57	14.2	15.2
Doublet at	1.08	0.825	0.812	24.6	24.2	0.77	0.72	2.62	2.59
$180~\mathrm{kHz}$	1.2	0.708	0.726	67.2	62.9	1.34	1.34	3.01	3.01
	1.32	0.654	0.683	106	98.7	1.56	1.56	3.05	3.14
No Doublet						0.43		0.56	0.22

for two different doublet frequencies (18 and 180 kHz). This shows clearly that for 10-mV settling, the 180-kHz doublet gives the worst degradation whereas for 1-mV settling the long time constant associated with the 18-kHz doublet causes this to be the worst case. These tests were repeated for negative steps from +5 to -5 V and similar results were obtained.

The computed results are summarized in Table I. The consistent trend towards smaller settling time is apparent as the doublet spacing is reduced. Also shown in Table I are values of τ_2 and k_2V calculated from (2) and (3) together with values determined from the computed responses. The values of τ_2 were simply determined from the tail of the exponential decay and the values of k_2V were determined by extrapolating back from the region of the exponential decay. Quite close agreement is seen in the values determined from the two methods.

Finally, Table I shows calculated values of settling time using (1). These show good agreement with the computed values.

IV. Conclusions

It has been shown that frequency doublets in the transfer function of an operational amplifier may cause severe degradation of settling time while only causing minor changes in the frequency response of the amplifier. The effect of the doublet depends both on its frequency and the pole-zero spacing. Reduction of the pole-zero spacing of the doublet reduces its effect, but pole-zero frequency mismatches as small as 8 percent can cause significant increases in settling time.

The effect of the doublet frequency on settling time is more complex. For 0.01 percent settling, a lower frequency doublet can potentially cause the worst performance degradation because of its long time constant. However, for 0.1 percent settling, the smaller amplitude of a lower frequency doublet may mean that it is always within the error band and has little effect. In that case a higher frequency doublet would cause more settling time degradation because of its larger amplitude, even though it decayed faster.

Finally, it has been shown quite generally that the simple formulas derived here can be used to predict the influence of frequency doublets on operational amplifier settling time.

APPENDIX

The circuit of Fig. 1 is to be analyzed for a step input of magnitude V where in general

$$V > I_0/g_m. (4)$$

In this situation, the initial voltage V_d applied to the differential input stage is sufficient to cause limiting and a constant current I_0 is supplied to the doublet and output stage. Computer simulation shows that in practice this occurs. The period when the input stage is limiting represents the slewing period of the amplifier and the feedback loop is effectively open during this period. When the output voltage $V_{\rm out}$ approaches within I_0/g_m of V, the differential stage enters its linear region and the amplifier settles to its final value with the feedback loop closed. Assumptions made are that the doublet is closely spaced and the doublet frequency is much less than the amplifier unity-gain frequency, i.e., $\omega_z \ll \omega_{co}$.

Consider the slewing period where the input stage is limiting. Then

$$I_1(s) = \frac{I_0}{s} \tag{5}$$

$$I_1(s) = \frac{I_0}{s} \frac{1 + (s/\omega_z)}{1 + (s/\omega_p)}$$
 (6)

$$V_{\text{out}}(s) = \frac{A/g_m}{1 + (sA/\omega_{co})} I_2(s).$$
 (7)

Taking inverse Laplace transforms

$$I_2(t) = I_0 \left[1 - \left(1 - \frac{\omega_p}{\omega_r} \right) \exp \left[-\omega_p t \right] \right]$$
 (8)

$$V_{\mathrm{out}}(t) = rac{I_0 A}{g_m} \left[1 - rac{1 - (\omega_p/\omega_z)}{1 - (A\omega_p/\omega_{co})} \exp\left[-\omega_p t \right]
ight]$$

$$+\frac{1-(\omega_{co}/A\omega_z)}{(\omega_{co}/A\omega_p)-1}\exp\left[-(\omega_{co}/A)t\right]$$
 (9)

At time T_s , the output V_{out} reaches $(V - (I_0/g_m))$ and

the differential input stage enters its linear region. The whole amplifier then begins settling as a linear feedback loop with initial conditions determined as follows.

$$I_1(T_s) = I_0 \tag{10}$$

$$V_{\text{out}}(T_s) = V - \frac{I_0}{g_m}. \tag{11}$$

Using

$$\exp\left[-\omega_n T_s\right] \simeq 1 - \omega_n T_s \tag{12}$$

and

$$\exp\left[-(\omega_{co}/A)T_s\right] \simeq 1 - \frac{\omega_{co}}{A}T_s,$$
 (13)

in (9) we have

$$T_s = \left(V \frac{g_m}{I_0} - 1\right) \frac{\omega_z}{\omega_p \omega_{co}}$$
 (14)

Using (14) and (12) in (8) gives

$$I_2(T_s) = I_0 \frac{\omega_p}{\omega_s} + \frac{\omega_z}{\omega_{co}} g_m \left(V - \frac{I_0}{g_m} \right) \left(1 - \frac{\omega_p}{\omega_s} \right). \tag{15}$$

With the amplifier operating linearly, the circuit equations are given by

$$V_{\text{out}}(s) = \frac{A/g_m}{1 + (As/\omega_{co})} I_2(s)$$
 (16)

$$I_2(s) = g_m \frac{1 + (s/\omega_z)}{1 + (s/\omega_p)} (V_{in}(s) - V_{out}(s))$$
 (17)

where initial conditions at $t = T_s$ are given by (10), (11), and (15). An analysis gives for $t > T_s$

$$V_{\text{out}}(t) \simeq V(1 - k_1' \exp \left[-\omega_{co}(t - T_s)\right] + k_2' \exp \left[-\omega_a(t - T_s)\right])$$
 (18)

where

$$k_1' \simeq \frac{(\omega_{co}/\omega_z) - 1}{(\omega_{co}/\omega_a) - 1} \left[1 - \frac{\omega_z}{\omega_p} \left(1 - \frac{I_0}{g_m V} \right) \right]$$
 (19)

$$k_2' \simeq \frac{(\omega_a/\omega_z) - 1}{1 - (\omega_a/\omega_{co})} \left[1 - \frac{\omega_a\omega_z}{\omega_{co}\omega_p} \left(1 - \frac{I_0}{g_m V} \right) \right] \tag{20}$$

$$\omega_a \simeq \omega_z \left[1 + \frac{1 - (\omega_p/\omega_z)}{(\omega_{co}/\omega_z) - 1} \right] \tag{21}$$

Equation (18) can be written as

$$V_{\text{out}}(t) \simeq V(1 - k_1 \exp [-\omega_{co}t] + k_2 \exp [-\omega_a t]),$$

for
$$t > T_s$$
. (22)

Since $\omega_a \ll \omega_{co}$, the last term represents the slow settling component and is the term of interest.

For typical values normally encountered, the term in parentheses in (20) is approximately unity. Thus

$$k_2 = k'_2 \exp\left[\omega_a T_s\right],\tag{23}$$

i.e.,

$$k_2 \simeq \frac{(\omega_a/\omega_z) - 1}{1 - (\omega_a/\omega_{co})} (1 + \omega_a T_s). \tag{24}$$

For typical component values $\omega_a T_s \ll 1$. In extreme cases, this term may be as large as 0.2 or 0.3. However, the effect of this factor on calculated settling time is much less because settling time is related to the logarithm of k_2 . Thus

$$k_2 \simeq \frac{(\omega_a/\omega_z) - 1}{1 - (\omega_a/\omega_{co})}.$$
 (25)

It is interesting to note that (25) is the same result as obtained in earlier work [1], [2] assuming completely linear operation of the amplifier.

Using equation (21) and assuming $\omega_z \ll \omega_{co}$, (25) can be further simplified to

$$k_2 \simeq \frac{\omega_z - \omega_p}{\omega_{co}}. (2)$$

From (21) it can be seen that

$$\omega_a \simeq \omega_z, \quad \text{if } \omega_z \ll \omega_{co}.$$
 (26)

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B. Yeshwant Kamath (S'72) was born in Mangalore, India, on August 26, 1948. He received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Madras, India, in 1969, and the M.S.E.E. degree from Syracuse University, Syracuse, N.Y., in 1971. He is presently at the University of California, Berkeley, studying towards the Ph.D degree in electrical engineering.

grated circuits.

His interests are in bioelectronics and in-

Robert G. Meyer (S'64-M'68), for a photograph and biography, please see p. 166 of the August 1974 issue of this JOURNAL.

Paul R. Gray (S'65–M'69), for a photograph and biography, please see p. 313 of this issue.