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# Three-Stage CMOS OTA for Large Capacitive Loads With Efficient Frequency Compensation Scheme

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## 1 Introduction

This project is based on the design and simulation of a real integrated analog circuit, starting from an accurate analysis of the papers presented on the IEEE library and choosing one of them.

Following the guidelines of the course, the optimal project in terms of feasibility and relevance has been identified on a three-stage operational transconductance amplifier and its compensation scheme, which has been published by Grasso, Palumbo, and Pennisi in 2006. The choice of this kind of circuit makes it possible to perform some interesting analysis to judge its performances for both time and frequency response. To realize and simulate this circuit, it was used the Virtuoso environment.

First of all, the paper has been carefully studied in all its main topics (stages, frequency response, compensation technique, etc...) to have a clear view of the theory that underlies the circuit designed by the paper owners.

One of the first constraints of the project has been the adaptation of the circuit to the available technology, which is different from the one used in the paper. To do this, a paper-and-pencil analysis has been preparatory to make the better design chooses before the effective implementation on Virtuoso.

Later on, the circuit has been first implemented as a schematic using the available CMOS libraries, understanding which are the best performances reachable on our circuit with this kind of technology. In this way, a first comparison with the paper result has been done.

The main step of this project was done concerning its layout realization. The layout has been designed following the design rules and using the interdigitated structure approach when useful. The compensation network components have been redesigned in order to take into account the changing on transistor transconductances. At this point, again, simulations and comparison with the paper were performed.

Finally, some conclusions have been done based on the result obtained in the various part of the project.

## 2 Theory

On this section has been quickly reported and explained the main topics which stands at the basis of the project.

### 2.1 Why three stage OTAs?

In all its applications, an operational transconductance amplifier (OTA) is an amplifier with a differential input power that produces a proportional output power and for this reason, it behaves as an ideal voltage-controlled current source (as represented in figure 1). As the classical operational amplifier, it has a high impedance differential input stage, and that it is usually used with negative feedback to control the frequency response and ensure its stability.

One of the most important parameters for a feedback amplifier is its DC open loop gain, which should be high enough to minimize the closed loop gain error. From this constrain born the necessity of building an amplifier with three stages. Due to the decrease in supply voltages, cascode topologies are not suitable for IC applications demanding both high gain and swing. Presently, amplifiers exhibiting DC gains over 100 dB can profitably be implemented with a cascade of three simple stages.

Generally, the first stage, in addition to providing a gain, usually must also provide a high common mode rejection. The intermediate stages in a cascade of stages amplifiers must provide most of the gain in voltage. In addition to this, the intermediate stages sometimes perform other functions, such as the conversion of the signal from differential mode to single-ended and the dc level translation of the signal to allow the output signal to assume both positive and negative values. Finally, the main task of the last stage (or output stage) is to supply the current required by the load efficiently. A configuration that lends itself well to this function is, for example, the source follower.

Therefore, multistage amplifiers and their frequency compensation have become increasingly important in modern technology. However, in designing a multistage opamp with multiple feedback loops, special care must be taken to ensure stability. For this reason, a lot of different compensation technique has been proposed during the year, allowing to get a stable three-stage amplifier.

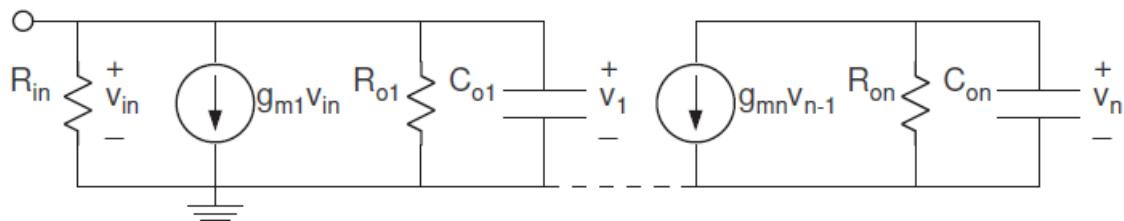


Figure 1: Generic n-stage small signal model.

## 2.2 Stability

In a feedback amplifier, the closed loop gain is generally a function of frequency and defined as:

$$A(jw) = \frac{a(jw)}{1 + \beta(jw)a(jw)} \quad (1)$$

Since the loop gain is a complex number it can be also written as:

$$T(jw) = |\beta(jw)a(jw)|e^{j\Phi(w)} \quad (2)$$

The loop gain and the open and closed loop gains are represented in figure 2.

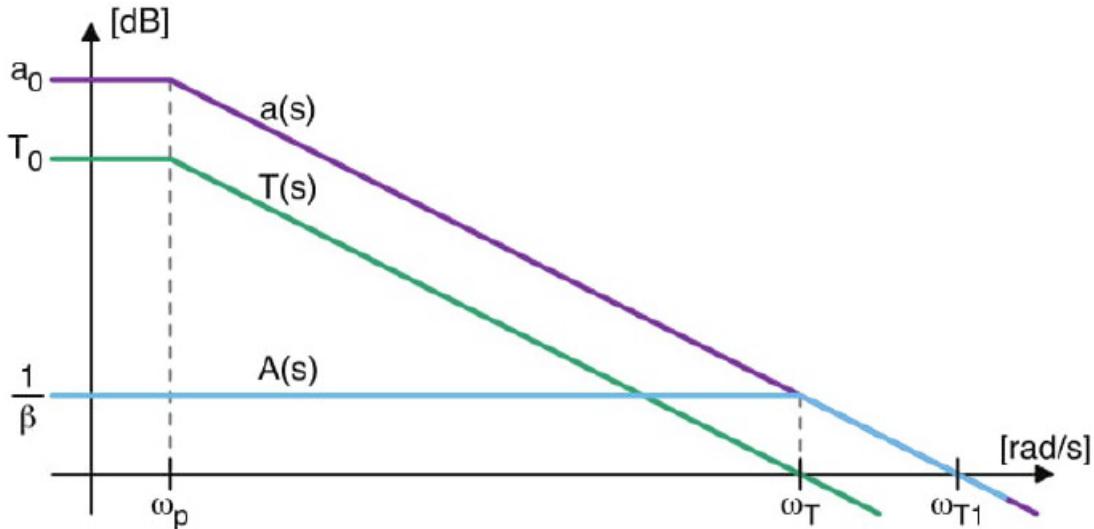


Figure 2: Feedback amplifier gains.

How the loop gain varies with the frequency determines the stability or instability of the feedback amplifier. To understand this fact, consider the frequency at which the phase angle  $\phi(\omega)$  becomes  $180^\circ$ . At this frequency ( $\omega_{180}$ ), the loop gain will be a number real with a negative sign, so at this frequency the feedback will become positive.

On the other hand, if at the frequency  $\omega_{180}$  the magnitude of the loop gain is equal to unity, it follows that  $A(j\omega)$  becomes infinite. This means that the amplifier will have a non-zero output even for a null input; what is called an oscillator by definition has been created. Here the purpose is exactly the opposite, therefore we must avoid the so-called Barkhausen oscillation condition which, as we said, occurs for modulus equal to:

$$|\beta(j\omega_{osc})a(j\omega_{osc})| = 1 \quad (3)$$

Instead for the phase:

$$\angle \beta(j\omega_{osc})a(j\omega_{osc}) = (2n + 1)\pi \quad (4)$$

In the complex plan this is equivalent to saying that we must avoid the point  $(\sigma, \omega) = (-1, 0)$ , which is the critical point for stability. The distance from the critical point is expressed through the phase margin and the gain margin. These parameters are represented by the Bode diagrams in figure 3.

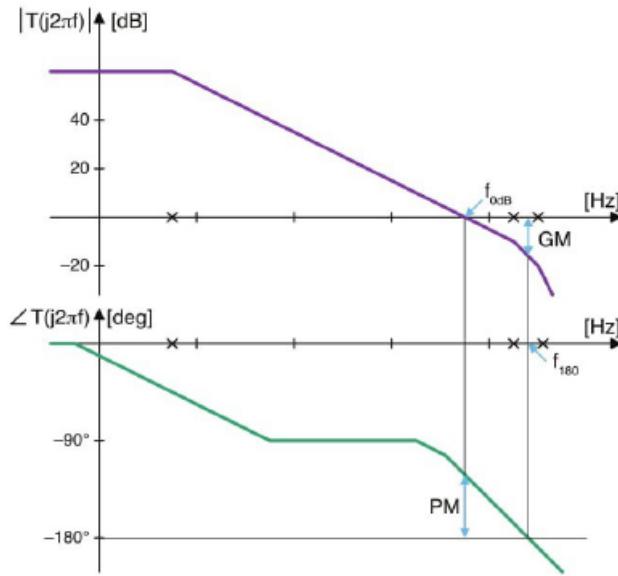


Figure 3: Gain and phase margins.

To evaluate the value of the phase margin, we look for the crossing pulsation and see if at this frequency value we have the phase angle greater or less than  $-180^\circ$ ; in the first case the amplifier is stable, in the second case it is unstable. The phase margin is evaluated as:

$$PM = 180 + \angle T(j\omega_T) \quad (5)$$

Mathematically, the amplifier is stable if  $PM > 0$ . However, in feedback amplifiers it is desirable to have phase margin above  $60^\circ$  but not too much high, as a compromise between the stability of the loop and the settling time in the transient response. Typically the minimum acceptable phase margin is  $45^\circ$ . To have a phase margin of  $45^\circ$  it must happen that only one pole (the dominant one) is to the left of the crossing pulsation, while the second coincides with it. By moving the second pole to the left the phase margin decreases, by moving the second pole to the right the phase margin increases. Therefore all the poles, apart from the dominant one, must be to the right of the crossing pulsation and the distance between it and the second

pole defines the value of the phase margin.

If the circuit in question does not meet the requirements on the phase margin it is necessary to use techniques to increase it, called compensation techniques.

### 2.3 Compensation

Currently, amplifiers exhibiting a dc gain in excess of 100 dB can be profitably implemented by cascading several simple transconductance gain stages. However, the design of such amplifiers is a challenging task since the increased number of high impedance nodes (and, in turn, of low-frequency poles) may result in instability. When three stages are used to implement the operational transconductance amplifier (OTA) and the last stage is the only inverting one, the nested Miller compensation, NMC, topology can be used. This technique employs two compensation capacitors that exploit the Miller effect to split low-frequency poles and achieve the desired phase margin and transient response. However, this solution results in bandwidth reduction and high power consumption, especially in CMOS technology.

In recent years, many compensation techniques improving the basic NMC topology have been proposed, in figure. The most efficient of these exploits additional transconductance stages to implement active compensation networks. In this manner, optimized bandwidth is achieved at the expense of increased circuit complexity and dissipation.

In this report, a simple compensation strategy, which uses passive components only, is exploited to design a three-stage OTA suitable for driving high capacitive loads and the scheme is represented in figure 5.

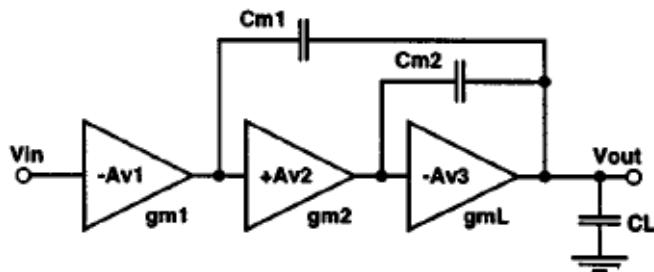


Figure 4: Classic Nested Miller Compensation.

Basically, this compensation technique is obtained starting from the classic Nested Miller Compensation, figure 4, and inserting two resistor to compensate the RHP zeros and the feedforward feature using  $g_{mf}$  in the opportune positions. In this way, by choosing smartly their value, a double pole-zero compensation is achieved and the system behaves a simple first-order. This means that the phase margin is almost equal to 90° if the parasitic pole is much higher than the gain-bandwidth product. The mathematical meaning of what has been said so far will be done during the analysis of the complete three-stage circuit.

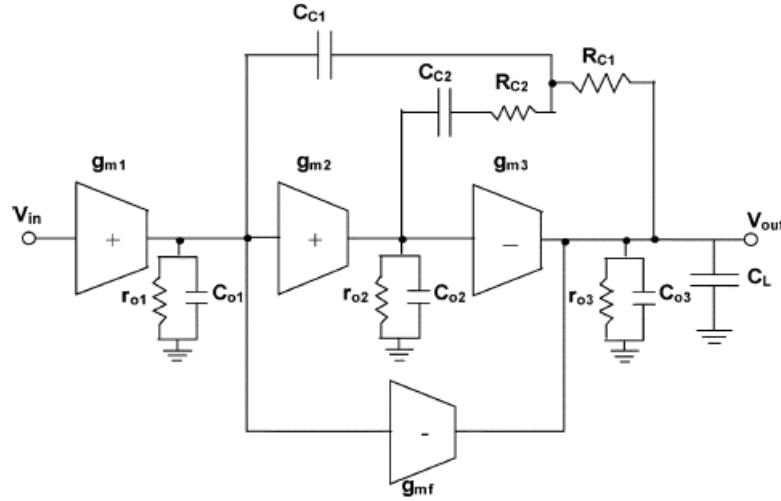


Figure 5: The adopted compensation technique.

## 2.4 The proposed three-stage OTA

The OTA circuit and its compensation network are represented in figure 6:

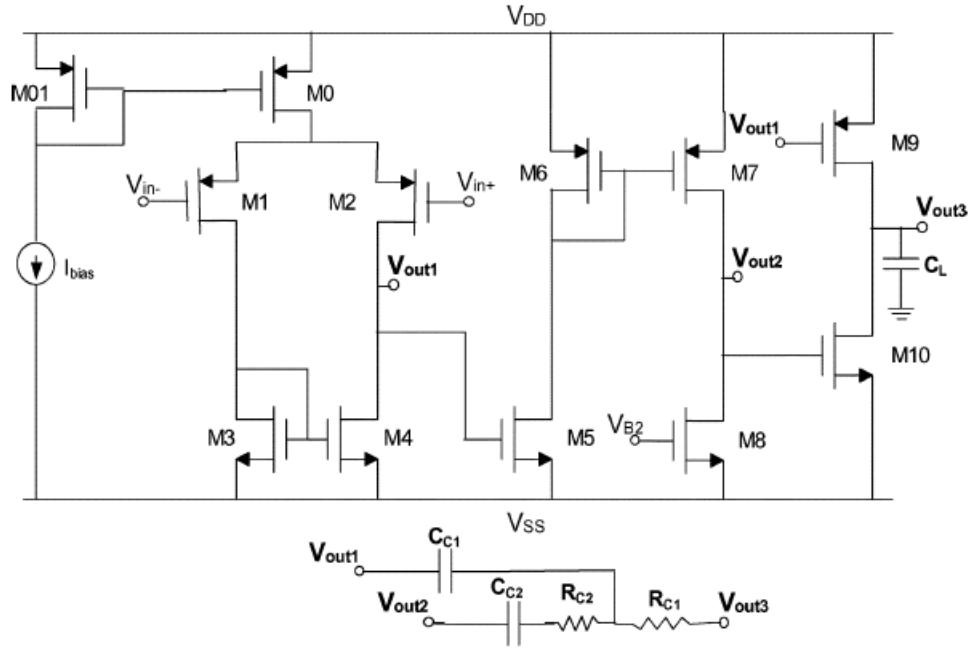


Figure 6: The implemented OTA

Assuming the approximation that each stage has a gain of  $A_{vi} = g_{mir_{oi}}$ , it can be

found that the transfer function of the compensated circuit has the following form:

$$A_v(s) = A_0 \frac{a_2 s^2 + a_1 s + 1}{\left(1 + \frac{s}{\omega_{p1}}\right) (b_2 s^2 + b_1 s + 1) \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (6)$$

$A_0$  is the DC gain and it is approximately equal to:

$$A_0 = g_{m1} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} \quad (7)$$

Regarding the numerator, the complete expression is given considering:

$$a_1 = R_{C1} C_{C1} + \left( R_{C2} - \frac{1}{g_{m3}} + \frac{g_{mf}}{g_{m2} g_{m3}} + R_{C1} \right) C_{C2} \quad (8)$$

$$a_2 = \frac{(1 + g_{m2} R_{C2}) g_{m3} R_{C1} - 1 + g_{mf} R_{C1}}{g_{m2} g_{m3}} C_{C1} C_{C2} \quad (9)$$

This two terms provides two zeros on the compensated transfer function.

The dominant pole is given by the Miller effect on  $C_{C1}$  and so it is around the frequency:

$$\omega_{p1} \approx \frac{1}{r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} C_{C1}} \quad (10)$$

Also, at the denominator it can be seen that there are two additional poles, which depends on  $C_{c2}$  and  $C_L$  and can be found considering:

$$b_1 = \left( R_{C2} + \frac{1}{g_{m2}} - \frac{1}{g_{m3}} + \frac{g_{mf}}{g_{m2} g_{m3}} \right) C_{C2} \quad (11)$$

$$b_2 = \frac{1 - g_{m2} R_{C1}}{g_{m2} g_{m3}} C_{C2} C_L \quad (12)$$

In addition, there is an high-frequency pole given by the contribution of the  $C_{o2}$ , at the frequency:

$$\omega_{HF} = \frac{R_{C1}}{1 - g_{m2} R_{C1}} C_{o2} \quad (13)$$

The compensation strategy is based on two simple considerations. The first one is that the two zeros can be made both negative, ensuring the absence of RHP zeros and consequently avoiding the related stability issues. But the main advantage is that properly choosing the values of component of the compensation network, their

values can be adjusted to exactly cancel out the two higher poles by a double pole-zero superimposition. This result can be obtained fixing:

$$R_{C1} = \frac{1}{g_{m3}} \quad (14)$$

while equating the coefficients of the second-order polynomials at the nominator and denominator of the compensated transfer function, we get:

$$R_{C2} = \frac{C_L}{g_{m3}C_{C2}} - \frac{g_{mf}}{g_{m3}g_{m2}} \quad (15)$$

$$C_{C1} = \frac{g_{m3} - g_{m2}}{g_{m2}} C_{C2} \quad (16)$$

These are the three design equation that have to be imposed in order to get the double pole-zero cancellation. Their value will be calculated later on by the inspection of the Virtuoso simulation results. In this way, ideally, OTA behaves as a simple first order system with 90° phase margin.

Some interesting consideration can be done regarding the previous design formula. To ensure positive values of  $R_{c2}$  and  $C_{c1}$ , must satisfy the constrains:

$$C_{C2} < C_L \left( \frac{g_{m2}}{g_{m3}} \right) \quad (17)$$

$$g_{m3} > g_{m2} \quad (18)$$

Moreover, it is worth noting that unlike conventional compensation strategies where  $C_{C1}$  is proportional to  $C_L$ , now  $C_{C1}$  is proportional to  $C_{C2}$ . For this reason, conclude that this compensation method is optimum for driving high capacitive load.

On the other side, assume that a phase margin almost equal to 90° is achieved if the parasitic pole is much higher than the GBW product. This condition is ensured by:

$$C_{C2} \gg \frac{g_{m1}g_{m2}}{(g_{m3} - g_{m2})^2} C_{o2} \quad (19)$$

Of course, using this principle the process tolerances will cause imperfect cancellation, causing a slower settling or even instability. This means that it is important to make an analysis regarding the component mismatch and their influence on amplifier performances.

Looking at the gate of M9, it is driven by the output of the first stage: a pseudo class-AB is implemented in order to drive the load with a very high current. As a result, in theory the slew-rate depends on the current available from the first stage

charging  $C_{C1}$ . Moreover, looking at this connection, the feedforward connection required in the compensation network is already implemented without the needing of extra transistor.

The OTA was designed using a triple-metal double-poly  $0.35\ \mu m$  n-well CMOS process. The transistor aspect ratio are reported in table 4. It is possible to see that there is a double supply voltage, equal to  $\pm 1.5\ V$  and the current  $I_{bias} = 10\ \mu A$ , with a total current dissipation of the circuit that correspond to  $150\ \mu A$ .

In order to analyze the stages, the transconductances are  $g_{m1} = 296\ A/V$ ,  $g_{m2} = 478\ A/V$  and  $g_{m3} = g_{mf} = 1.23\ mA/V$ . Consequently, to obtain a gain-bandwidth product of  $1.5\ MHz$  with a capacitive load of  $500\ pF$ , get  $C_{C1} = 30\ pF$ , and from the design equations, it is possible to set  $R_{C1} = 800\ \Omega$ ,  $R_{C2} = 18\ k\Omega$  and  $C_{C2} = 20\ pF$ . All of these values are obtained following the design equations. But of course, optimization can be obtained, like set the value  $R_{C2} = 20\ k\Omega$  to slightly reduce peaking in the step response.

The prototype of the circuit in exam was fabricated and experimentally characterized with different performance parameters, in table 1.

PARAMETER	VALUE
Technology	$0.35\ \mu m$ CMOS
Area	$0.075\ mm^2$
Power supply	$1.5\ V$
Loading Capacitance	$500\ pF$
Input Offset Voltage	$2.3\ mV$
DC Gain	$113\ dB$
Gain-bandwidth Product	$1.4\ MHz$
Phase Margin	$75^\circ$
CMRR @ DC	$78\ dB$
Positive(Negative) Slew Rate	$2.2(-1.8)\ V/\mu s$
Positive(Negative) Settling time at 1%	$810(740)\ ns$
HD2/HD3 @ $100kHz$ , $400mVpp$	$-54.25 / -60.36\ dB$
HD2/HD3 @ $100kHz$ , $500mVpp$	$-48.20 / -56.71\ dB$

Table 1: OTA MAIN PERFORMANCE PARAMETER

It is also possible to analyze the case of the effects of an imperfect double pole-zero cancellation, caused by process tolerances. Indeed, the presence of a double pole-zero in the loop gain can lead to a slower settling or even instability.

This approximation is represented with the generic transfer function:

$$A(s) = \frac{\omega_{GBW}}{s} \cdot \frac{1 + b_1s + b_2s^2}{1 + a_1s + a_2s^2} \quad (20)$$

The effect of mismatch on coefficients  $b_i$  through parameters  $\delta_{1,2}$  as:

$$b_1 = a_1(1 + \delta_1) = \frac{2\xi}{\omega_n}(1 + \delta_1) \quad (21)$$

$$b_2 = a_2(1 + \delta_2) = \frac{1}{\omega_n^2}(1 + \delta_2) \quad (22)$$

where there are introduced the damping factor  $\xi$  and the poles frequency  $\omega_n$  in the rightmost expressions.

The factor  $\xi$  is always greater than 1, so this ensures that the poles are real and are located approximately at the frequency  $1/a_1 = \omega_n/2\xi$  and  $a_1/a_2 = 2\xi\omega_n$ .

In order to derive  $\omega_{GBW}$  is possible to impose that  $a_1/a_2 > \omega_{GBW}$ , the second doublet is at the right of the gain-bandwidth product. Assuming pessimistically  $\omega_n \cong \omega_{GBW}$ , the lower frequency doublet is about  $2\xi$  lower than  $\omega_{GBW}$ , or for higher frequency could be greater. Therefore, the possible mismatch of parameters  $a_1$  and  $b_1$  could worsen the settling time and modify the actual unity-gain frequency.

Consider now the pessimistic case in which the mismatches are all uncorrelated and assuming that the values of the circuit parameters are uniformly distributed within  $\pm 20\%$  of their nominal value. So it is possible to evaluate the variations of parameters  $\delta_1$  and  $\delta_2$ . Taking into account the distribution of over 1000 iterations, there are set  $C_L/C_{C2} = 2.5$ ,  $g_{m3}/g_{m2} = 2.5$ ,  $\omega_{GBW}/\omega_n = 0.95$ , and  $\xi = 2$ , it could be evident that  $\delta_1$  is almost insensitive to the parameter mismatches, due to the fact that its variation is very limited. Thus, the adopted compensation technique attenuates the effects of mismatches on the imperfect cancellation of the lower pole-zero doublet, so limiting the worsening of the settling time.

On the other hand the parameter  $\delta_2$  is more affected by mismatches since its value varies a lot. Nevertheless  $\delta_2$  is responsible for the imperfect cancellation of the highest pole-zero doublet located well beyond the gain-bandwidth product.

Finally, the area of paper layout is  $0.075 \text{ mm}^2$  and the 80% of it is occupied by the compensation network.

### 3 Paper and pencil analysis

Pen and paper analysis of the proposed circuit is necessary before implementation and simulation on Virtuoso environment. The analysis was focused on single stages and their behavior in DC, on the frequency response of the non-compensated circuit, and the input and output ranges of the circuit. Transistor sizing was not necessary since it was already made available in the paper. Regarding the compensation network, as seen before, the design formula was already provided in order to make directly their computation.

#### 3.1 Single stages analysis

The first stage, represented in figure 7, is composed by a PMOS differential pair polarized by the current mirror  $M_0 - M_{01}$  and having the mirror  $M_3 - M_4$  as load in order to obtain a large gain.

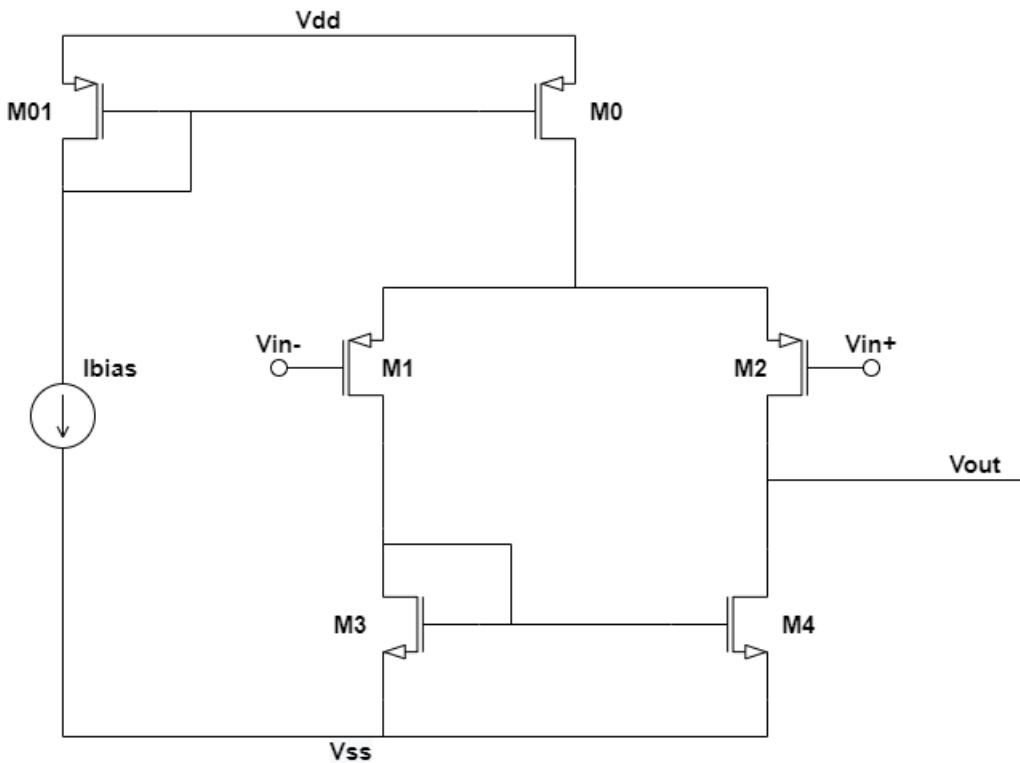


Figure 7: First stage.

This stage has a differential input and a single output. In order to polarize the differential pair in the right way, we must choose the aspect ratio of the transistor in such a way that:

$$\left(\frac{W}{L}\right)_{M_0} = 2 \left(\frac{W}{L}\right)_{M_{01}} \quad (23)$$

$$\left(\frac{W}{L}\right)_{M3} = \left(\frac{W}{L}\right)_{M4} \quad (24)$$

In this way, ideally, on  $M_0$  flows two times  $I_{bias}$  which is equally divided between  $M_1$  and  $M_2$  if the differential pair is perfectly symmetric. Finally, the same current is mirrored by  $M_3$  and  $M_4$ . This is also ensured by the feedback action.

With this kind of configuration, the main advantage with respect to the classical one is that we don't need a bias voltage for the  $M_3 - M_4$  load, but on the other side the issue is that only single output is possible. The choose of a PMOS pair allows to have a lower noise than NMOS pair, however the gain is reduced ( $k_p < k_n$ ).

In theory, the differential pair works ideally if the structure is perfectly symmetric. Of course, this is not achievable in the reality because of the component mismatch. For this reason, the common mode is not perfectly rejected and not only the differential voltage is amplifier, causing a non infinite Common Mode Rejection Ratio of the stage. Also, the mismatch is cause of the offset voltage, which is the non-zero input voltage for which the output assume a null value.

Another parameter to take into account is the CMR, defined as the input voltage range for which all the transistors work in linearity and determines a specification on amplifier use; their limits, defined as  $CMR^+$  and  $CMR^-$ , will be found later on. By the analysis of the small signal model of the circuit, it can be found that:

$$A_1 = g_{m1,2}(r_{o4}/r_{o2}) \quad (25)$$

Note that the gain is non-inverting, as required for the proposed compensation network.

If a better gain is desired, a cascode differential pair with cascode load can be used. The considerations are identical with the previous case, but the gain can be doubled. However, it cannot be used in a low-voltage system as the one proposed since many devices must be maintained in saturation and the CMR is greatly limited.

Regarding the second stage, it is represented in figure 8. In this case a simple common source cannot be used since it has an inverting gain and it is not suitable with the proposed compensation technique, in which only the third and last stage is inverting. For this reason, a mirror source is also used. How does the second stage behaves? When  $v_{out1}$  grows, the same happens for  $i_{d5} = i_{d6}$ , which is mirrored by  $M_6 - M_7$  obtaining that also  $i_{d7}$  grows. On the other side,  $i_{d8}$  is constant because fixed by  $V_{b2}$ , which means that the output node of the second stage grows. For this reason, this is a non inverting stage.

What about its gain? Analyzing the circuit, comes out that:

$$A_2 = g_{m5}(r_{o7}/r_{o8}) \quad (26)$$

This is exactly the same gain of the common source but with a plus sign.

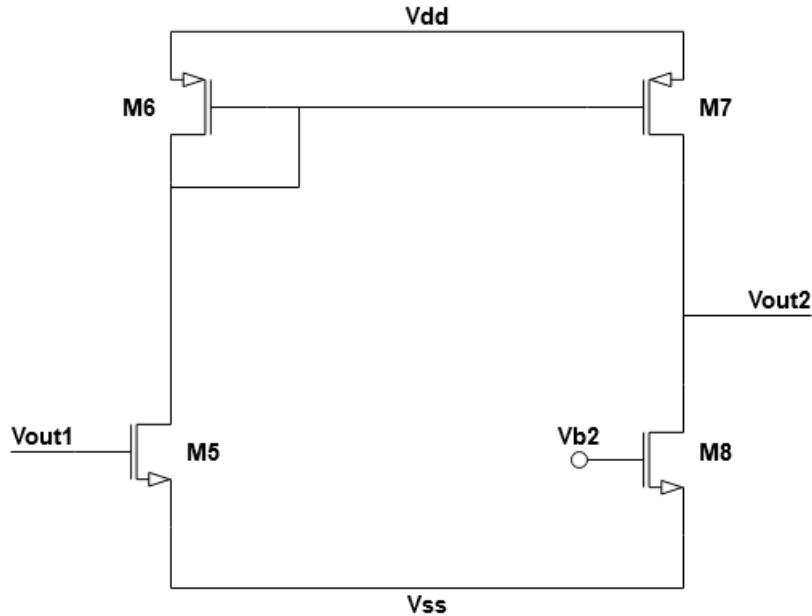


Figure 8: Second stage.

Finally, the third stage is a simple common source with active load, as reported in figure 9.

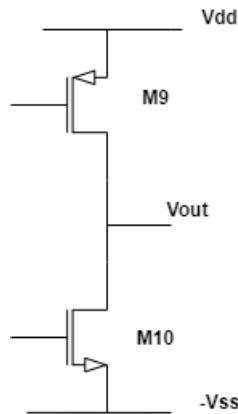


Figure 9: Third stage.

Easily, its gain is inverting and equal to:

$$A_3 = g_{m10}(r_{o9} // r_{o10}) \quad (27)$$

Putting them together, the total DC gain is equal to:

$$A_{tot} = G_{m1}R_{o1}G_{m2}R_{o2}G_{m3}R_{o3} \quad (28)$$

Where the previous parameters are reported in table 2.

	<b>1</b>	<b>2</b>	<b>3</b>
$G_m$	$g_{m1,2}$	$g_{m5}$	$g_{m10}$
$R_o$	$r_{o4} // r_{o2}$	$r_{o7} // r_{o8}$	$r_{o9} // r_{o10}$

Table 2: Transconductances and output resistances.

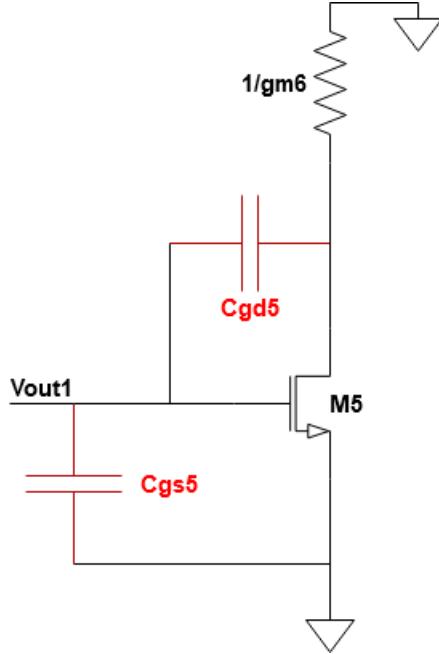
### 3.2 Frequency response of non-compensated circuit

Looking again at the single stages, the non-compensated circuit exhibits three poles as represented in table 3.

	<b>1</b>	<b>2</b>	<b>3</b>
$\omega_p$	$\frac{1}{R_{o1}C_{o1}}$	$\frac{1}{R_{o2}C_{o2}}$	$\frac{1}{R_{o3}C_{o3}}$

Table 3: Poles.

The output resistances are the ones founded before, in the theoretical gain evaluation. What about the output capacitance? Looking at 10, it is possible to find the theoretic expression of  $C_{o1}$ .

Figure 10:  $C_{o1}$  evaluation.

Cannot apply Miller at all the second stage since it is not an inverting stage. However, I can use it for  $M_5 - M_6$ , finding that:

$$C_{o1} = C_{gs5} + C_{gd5} \left[ 1 + g_{m5} \left( \frac{1}{g_{m6}} // r_{o5} \right) \right] \quad (29)$$

Instead, for the output of the second stage it can be easily applied Miller at the common source  $M_9 - M_{10}$ , finding that:

$$C_{o2} = C_{gs10} + C_{gd10} (1 + A_3) \quad (30)$$

And, of course, therefore as the output of the third stage is the output of the OTA and this one is designed to drive a large capacitive load, we can say that:

$$C_{o3} \approx C_L \quad (31)$$

Also, using Miller it can be found that RHP zeros are presents and located at high frequency and they can sometimes be cause of instability. Moreover, having three poles related to three high impedance node bring to a probably instability situation, according to what was said during the stability section. In order to solve this issue, compensation is applied. If it behaves as explained before, double pole-zero cancellation, the system behaves as a first order system and exhibits only one dominant pole at very low frequency. The expected results should be something with a phase margin of around 90 degrees.

### 3.3 Aspect ratios

Regarding the transistor dimensions, they were already provided by the paper as reported in table 4.

Transistor	Aspect ratio
M0	$2 \times (40/1)$
M01	$40/1$
M1, M2	$4 \times (40/1)$
M3, M4	$40/0.7$
M5	$2 \times (40/0.7)$
M6, M7	$50/0.7$
M8	$40/1$
M9	$4 \times (40/0.7)$
M10	$8 \times (40/0.7)$

Table 4: Paper aspect ratios.

Unfortunately, the paper doesn't report precisely the specification values taken into consideration to decide the size of the transistors. Typically, the design chooses are related to DC gain, GBW, CMR, Slew Rate, and so on. For example, as it will be seen later, the compensation network will be designed starting from a desired GBW product.

For the  $W/L$  ratio, in order to obtain a large DC gain, we should consider that the transconductance is given by:

$$g_m = 2\beta_n \left( \frac{W}{L} \right) v_{od} = \frac{I_D}{\beta_n v_{od}^2} \quad (32)$$

This is the reason for which, for example,  $M_1$ ,  $M_2$  and  $M_{10}$  are very wide transistors, since they are related to the stage transconductances as shown on table 2.

Now, since the technology used in the paper is a  $0.35\mu m$  CMOS while the available on our version of Virtuoso is the  $0.6\mu m$  CMOS, a re-scaling of the dimensions is necessary. To do this, this project is done considering the length at least equal to the double of the minimum length, in order to avoid short channel effects.

In fact, since this circuit must provide an high gain, small channel devices are not useful because in this case the output resistance decrease. Instead, they are used when we have constrain on physical dimensions and frequency operation range. Any-way, on paper, the length of the shortest transistors is  $0.7\mu m = 2 \cdot 0.35\mu m$ . For this reason, we considered the smallest length of  $1.2\mu m = 2 \cdot 0.6\mu m$ . Based on this constrain, for first we associated  $0.7\mu m$  with  $1.2\mu m$ . Making a proportion, the  $1\mu m$  length has been associated to:

$$0.7 : 1.2 = 1 : x \implies x = 1.714 \quad (33)$$

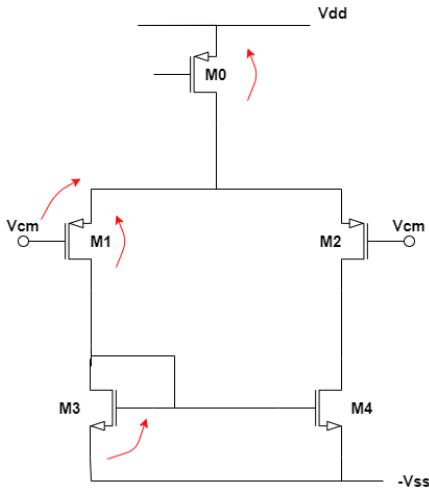
Since on our version of Virtuoso every dimension has to be a multiple of  $0.15\mu m$ , a length of  $1.65\mu m$  has been considered. In this way, fixing all the transistor lengths, to maintain true the ratios on table 4, the aspect ratio of our project are the ones reported in table 5.

Transistor	Aspect ratio
M0	$2 \times (66/1.65)$
M01	$66/1.65$
M1, M2	$4 \times (66/1.65)$
M3, M4	$68.55/1.2$
M5	$2 \times (68.55/1.2)$
M6, M7	$85.65/1.2$
M8	$66/1.65$
M9	$4 \times (68.55/1.2)$
M10	$8 \times (68.55/1.2)$

Table 5: Project aspect ratios.

### 3.4 Input and output range

In this section the Common Mode Range(CMR) and the Output Range(OR) are going to be analysed. The goal is to understand which are the maximum and minimum available values for the input bias voltage and the output voltage swing upper and lower limits. First of all, the CMR is going to be analysed:



By considering the highlighted potentials in the figure on left, it's possible to evaluate which the CMR is. In fact by doing some KVL node equations:

$$\begin{cases} V_{CM} + V_{SG,M1} - V_{GS,M3} - (-V_{SS}) \geq V_{OD,M1} \\ V_{DD} - (V_{SG,M1} - V_{CM}) \geq V_{OD,M0} \end{cases} \quad (34)$$

Figure 11 CMR potential analysis

After some algebraic steps, the found lower and upper limits are showed below:

$$\begin{cases} V_{CM} \geq V_{THN} - |V_{THP}| + \sqrt{\frac{I_{BIAS}}{2 \cdot \beta_N \cdot \frac{W}{L} |_3}} - V_{SS} \\ V_{CM} \leq V_{DD} - \sqrt{\frac{2 \cdot I_{BIAS}}{\beta_P \cdot \frac{W}{L} |_1}} - |V_{THP}| \end{cases} \quad (35)$$

Where:  $W$  is the channel width,  $L$  is the channel length,  $V_{THN,P}$  are the threshold voltages.

Example:

$$\begin{aligned} V_{THN} &= 0.7V \\ V_{THP} &= 0.8V \\ V_{SS} &= 1.5V \\ I_{BIAS} &= 10\mu A \\ \beta_N &= 50\mu A/V^2 \\ \beta_P &= 26\mu A/V^2 \\ \frac{W}{L} |_1 &= 160 \\ \frac{W}{L} |_3 &= 57.125 \end{aligned}$$

Results:

$$\begin{aligned} V_{CM} &\geq -1.558V \\ V_{CM} &\leq 0.63V \end{aligned}$$

Now the Output Range OR is going to be analysed, in order to do that it is necessary to look at the third stage potential, as in the image below:

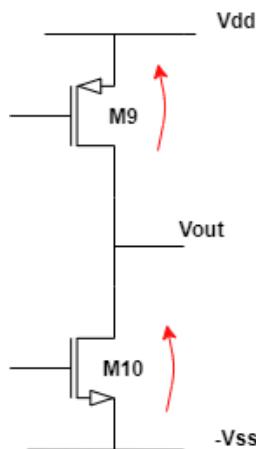


Figure 12 Third stage KVL

The upper and lower limits are represented by the following two equations:

$$\begin{aligned} V_{max}^{out} &\leq V_{DD} - V_{OD,M9} \\ V_{min}^{out} &\geq -V_{SS} + V_{OD,M10} \end{aligned}$$

Example:

$$\begin{aligned} |V_{DD,SS}| &= 1.5V \\ |V_{OD9,10}| &= 150mV \end{aligned}$$

Then:

$$V_{out} \in [-1.35V; 1.35V]$$

These limits were evaluated in order to ensure that the output stage will have its transistors in saturation region. However, that range doesn't ensure that the other stages transistors will remain saturated.

## 4 Schematic

After the preliminary and theoretical analysis, now it's time to start with Virtuoso implementation. The design has been divided in two steps: the first regarding only the schematic and using the already available CMOS library while the second one with the complete layout realization. On this section, the simple schematic design and simulation is reported.

For the schematic design, the aspect ratios on table 5 have been used. Virtuoso environment allows to use the multiplier, which automatically takes "n" times the defined width of the transistor.

For first, the non-compensated schematic has been realized using the *ami06* NMOS and PMOS models already present. The transistor has been imported from the *AnalogParts* library. The schematic view is reported on figure 13.

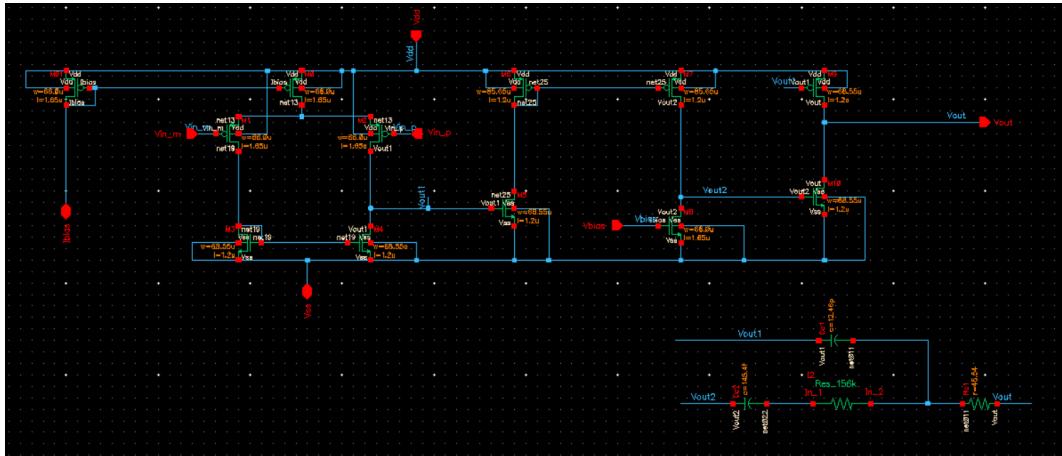


Figure 13: Three stage OTA schematic.

Since the paper doesn't specify nothing about the voltage and current biasing, it is supposed to have them externally with ideal sources on the simulation cellview using additional pins. Anyway, some possible internal implementation will be presented later on.

The compensation network has been designed using the design formula reported in the theory section. To do this, a DC simulation has been performed, using the *DC operating point* tool. Looking at the single stages, the transconductances reported in table 6 have been found.

$g_{m1}$	$117.4 \mu A/V$
$g_{m2}$	$251.7 \mu A/V$
$g_{m3}$	$21.8mA/V$
$g_{mf}$	$7.8mA/V$

Table 6: Simulated transconductances.

With the Matlab auxiliary and using the simulated transconductances, the component values of compensation network have been found as shown on table 7. To do this, a starting goal has been fixed for the project regarding the Gain-Bandwidth Product:

$$F_{GBW} = 1.5 \text{ MHz} \quad (36)$$

In fact, it is used on  $C_{c1}$  evaluation remembering that:

$$C_{c1} = \frac{g_{m1}}{2\pi\omega_{GBW}} \quad (37)$$

$C_{c1}$	12.46 pF
$C_{c2}$	145.5 fF
$R_{c1}$	45.8 Ω
$R_{c2}$	156.2 kΩ

Table 7: Compensation network design.

Also, two other parameters were found. The damping factor depends both on transconductances and compensation network values and it is given by:

$$\xi = \frac{1}{2} \left( \frac{C_L}{C_{C2}} + \frac{g_{m3}}{g_{m2}} - 1 \right) \left[ \frac{C_L}{C_{C2}} \left( \frac{g_{m3}}{g_{m2}} - 1 \right) \right]^{-\frac{1}{2}} = 3.2467 \quad (38)$$

Since the value on paper is 2.1, this result is coherent.

On the other side, in order to ensure a phase margin of at least 90 degree, the following constrain has to be imposed:

$$C_{C2} \gg \frac{g_{m1}g_{m2}}{(g_{m3} - g_{m2})^2} C_{o2} \quad (39)$$

The value of  $C_{o2}$  has been found with:

$$C_{o2} = C_{gs10} // C_{ds8} \quad (40)$$

Where these values has been found by the *DC operating point* analysis on the transistors. This verification has been done performing the difference between the first and the second member of the relation, founding that it is ensured because:

$$C_{C2} - \frac{g_{m1}g_{m2}}{(g_{m3} - g_{m2})^2} C_{o2} = 1.97 \times 10^3 \quad (41)$$

Making a comparison with the paper values, it is evident as in this work one capacitor is strongly greater than the other one: this is due to the such higher transconductance of the final stage, which cause also a much higher total bias current. At the

same way, a big  $R_{c2}$  is present. For this reason, it will be implemented on layout with a series of multiple smaller resistance. This is the reason for which on figure 13 the  $R_{c2}$  is represented by a self-made symbol.

## 4.1 Simulations

The schematic is analyzed to understand the behaviour under different conditions, to analyze the performance parameters, and therefore compare it with the ones described in the paper.

### DC Sweep

At first it is performed a DC sweep analysis in order to understand the correct working point for the  $V_{b2}$  and  $V_{inp}$  generators.

The two input generators are imposed to be equal,  $V_{inp} = V_{inm}$ , so the two pins are connected together, and at last proceed with the simulation.

Launch/ADE-L/Setup/Model Libraries useful to choose the correct models *ami06N.m* and *ami06P.m*. Therefore, choose Analysis/DC/Component parameter and select at first  $V_{b2}$  generator to sweep, with start-stop of  $-1.6V$  and  $+1.6V$ , step size of  $500\mu$  and linear sweep type. At last select the output  $V_{out}$  and from the behaviour in figure 14, the optimum bias point found is  $V_{b2} = -748 mV$ .

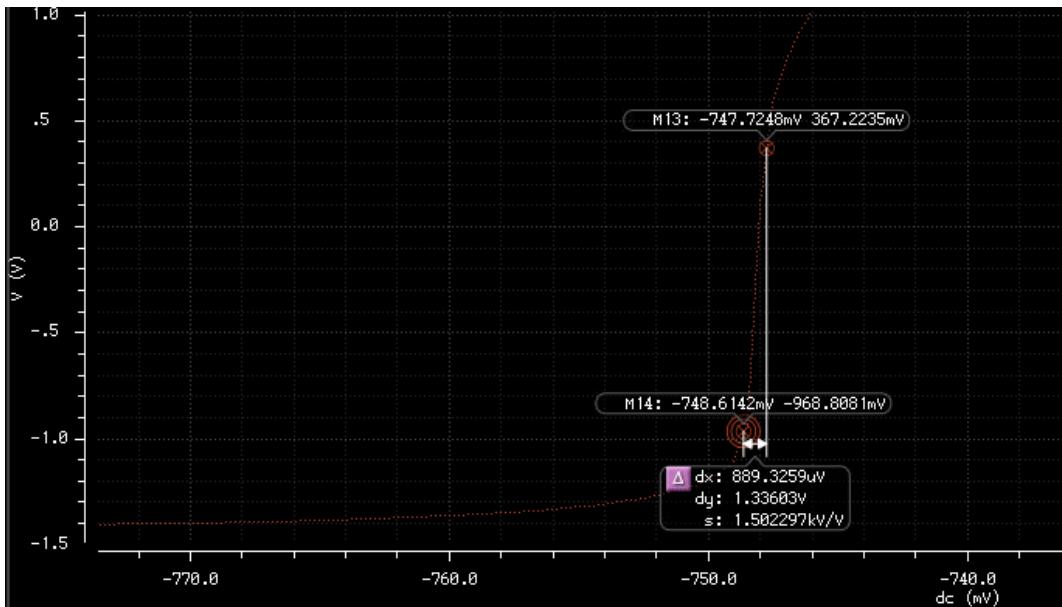
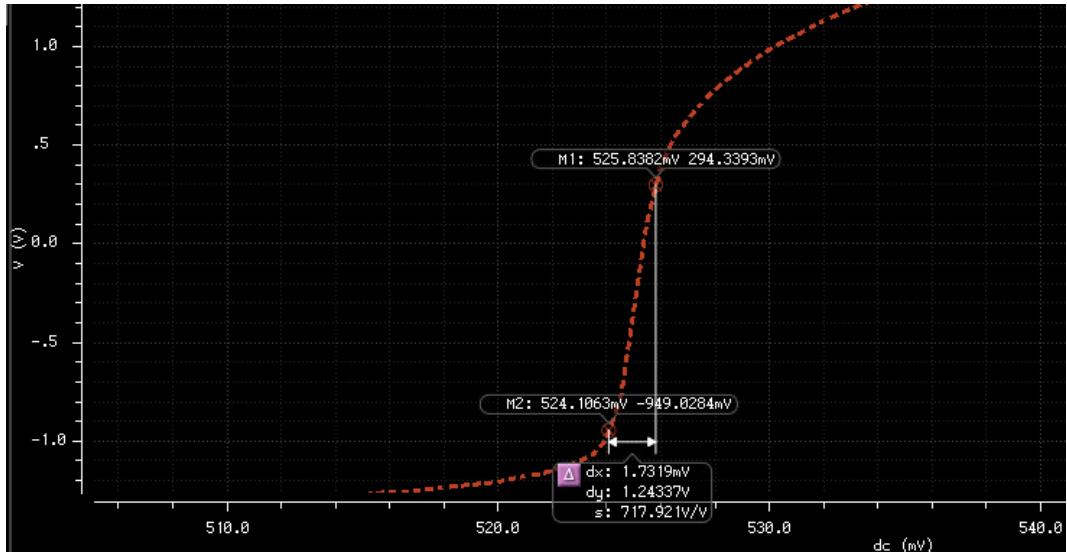


Figure 14: DC sweep of  $V_{b2}$

The sweep simulation is also repeated to obtain a  $V_{inp} = 525 mV$ , in figure 15.

Figure 15: DC sweep of  $V_{inp}$ 

### Input Offset Voltage

To perform this simulation, set  $V_{out} = V_{inm}$  (closed loop configuration) and  $V_{inp}$  with DC Voltage= 0 and also AC Magnitude= 0. Launch the simulation in order to obtain the operating point, so when it is finished choose Results/Print/DC Node Voltage and select  $V_{out}$ . Therefore, the input offset voltage is equal to  $-277 \mu V$ , that it is generally a very small value for an OTA offset. For example, on paper results an offset of  $2.3 mV$  is reported.

### AC Open Loop

Simulation in open loop is done to obtain gain and phase. Therefore, Choose Analysis/AC, sweep variable is the frequency, with a range from  $1 Hz$  to  $5 MHz$ , sweep type Logarithmic within 20 points per decade. Thus, proceed Results/Direct plot/AC Gain and Phase of  $V_{out}$  vs  $V_{inp}$ , in figure 16.

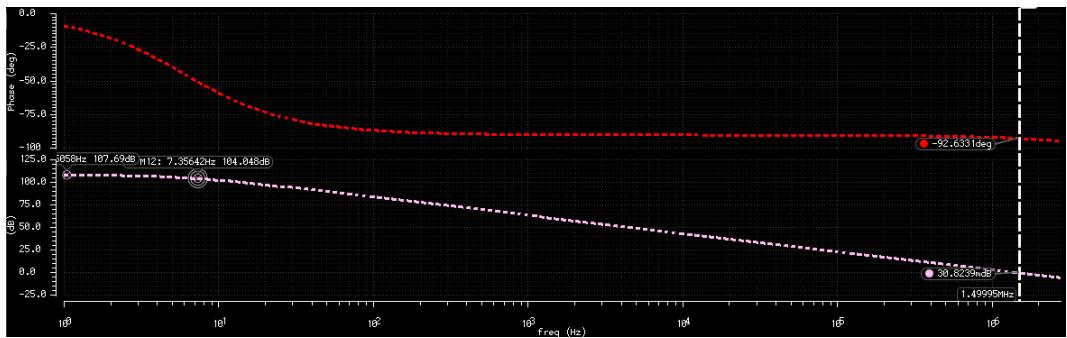


Figure 16: AC Gain and Phase in Open Loop

Notice that the DC open loop gain is  $107.7 db$ , while the first pole has  $f = 7.35 Hz$

corresponding at gain  $104.7 \text{ dB}$ . At last the transition frequency, the frequency when the gain equal to  $0 \text{ dB}$ ,  $f_T = 1.499 \text{ MHz}$  at the phase  $-92.6^\circ$ . In this situation is possible to understand that the phase margin,  $PM = (180 - 92.6)^\circ = 87.4^\circ$ , very large value so the system is in stability.

The compensation works correctly, in fact 2 poles are canceled by two zeros, so is possible to notice first order behaviour of the system.

The DC gain obtained is a little less respect the one obtained in the paper,  $113 \text{ dB}$ , maybe due to the fact of specific technology for the implementation in exam.

While the PM obtained is greater respect the one computed in the paper, that it is  $PM_{paper} = 75^\circ$ .

### Closed Loop

In order to obtain the GBW is used the closed loop configuration, and there are repeated the same simulations steps done before in open loop. On the other hand, the cut frequency,  $f_T(-3\text{dB}) = 1.65 \text{ MHz}$  with a phase= $49^\circ$ , in figure 17.

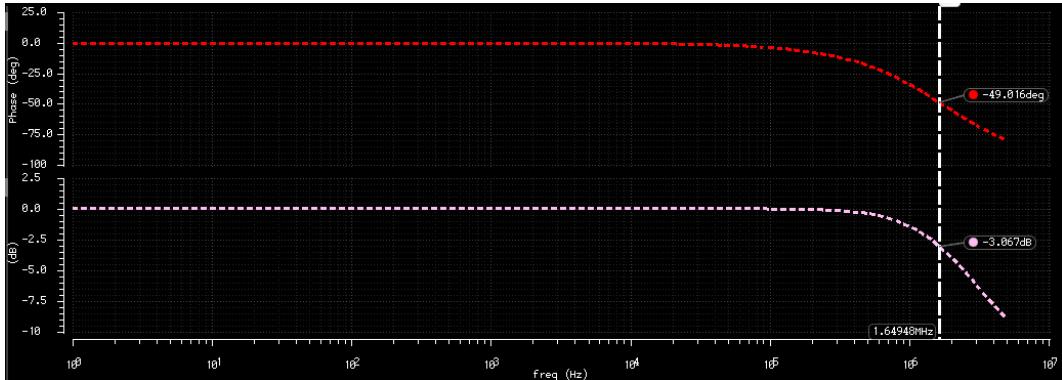


Figure 17: GBW

The GBW obtained is greater respect the one computed in the paper, that it is  $GBW_{paper} = 1.4 \text{ MHz}$ .

### Step Response

The step is now applied on the input  $V_{inp}$ , with a  $V_{pulse}$  generator, setting the input voltage step to  $-200 \text{ mV}$  and  $200 \text{ mV}$ , rise time and fall time equal to  $500 \text{ ns}$ , pulse width=  $2.5 \mu\text{s}$  and delay=  $6 \mu\text{s}$ , in figure 18. Launch ADE-L, chose a tran simulation with a stop time=  $100 \mu\text{s}$  and select  $V_{out}$ . It is possible to notice that in this situation the system is unstable, due to the fast rise and fall time.

Therefore, to have a stable system rise and fall time were increased up to  $700 \text{ ns}$  and the simulation is also repeated in order to obtain the correct performance parameters.

Computing the value in the linear region is possible to obtain the rise time, in the  $10\% - 90\%$  of the transient response, so  $t_r = 578.4 \text{ ns}$ , in figure 19.

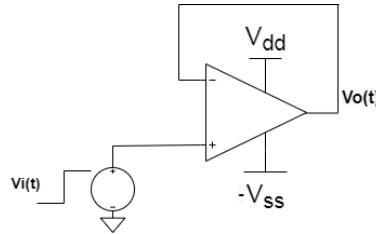
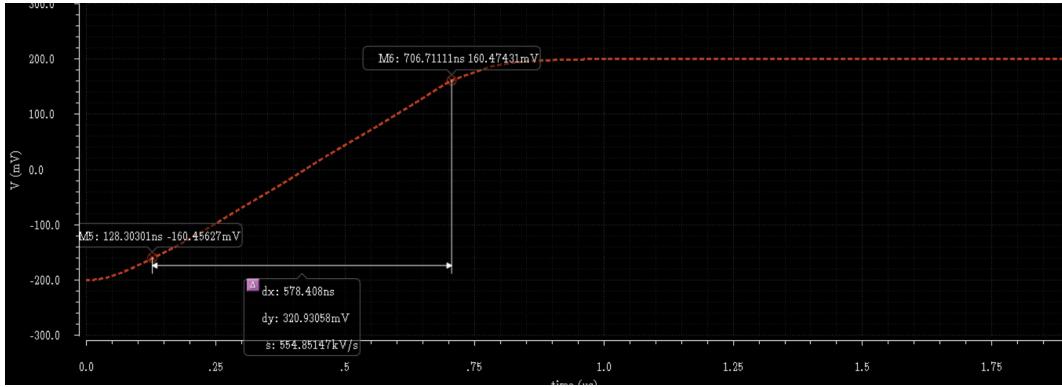


Figure 18: SR scheme

Figure 19: Rise Time  $t_r$ 

The settling time is the time required for the response curve to reach and stay within a range of certain percentage, 1% of the final value. In figure 20, it is possible to highlight that it is equal to  $931.1\text{ ns}$ .

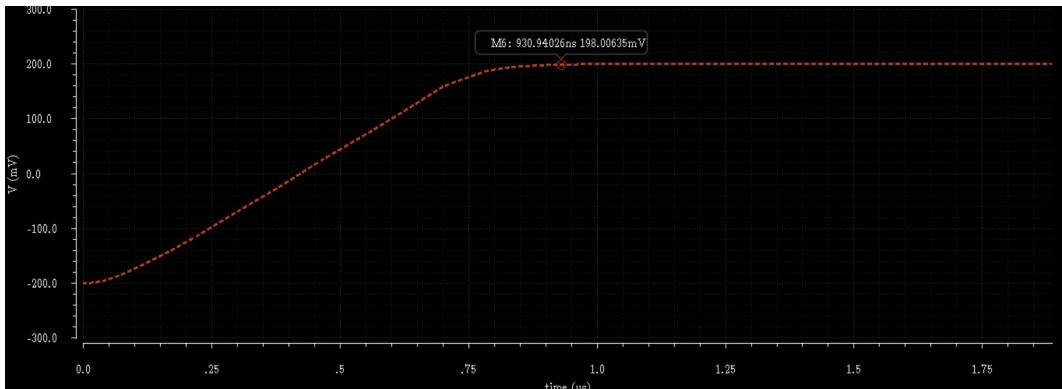


Figure 20: Positive Settling Time

At last the slew rate, defined as the rate of change of the voltage per unit time, is computed,  $SR_+ = 0.56\text{ V}/\mu\text{s}$ , in figure 21.

All these parameters are also computed for the falling edges, as fall time  $t_f = 569.2\text{ ns}$ , figure 22, negative settling time  $905.54\text{ ns}$  in figure 23, and negative slew rate  $SR_- = 0.57\text{ V}/\mu\text{s}$  in figure 24.

The positive and negative settling time obtained result higher than the paper ones,

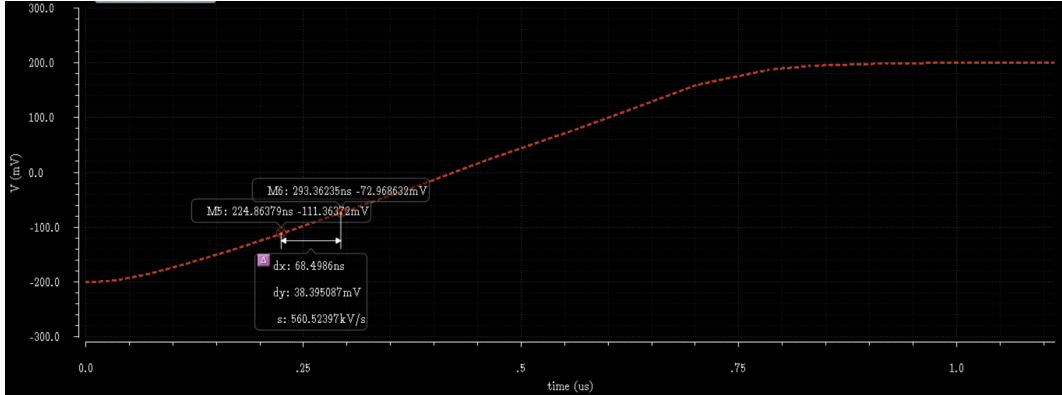


Figure 21: Positive Slew Rate

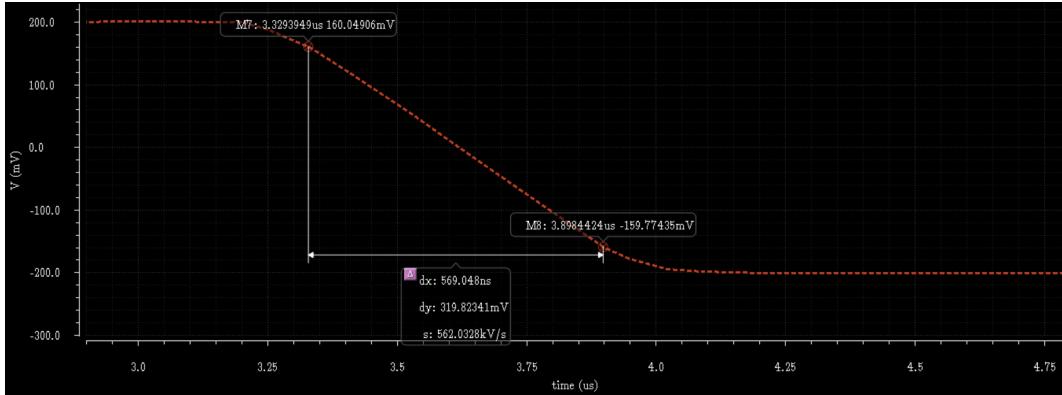
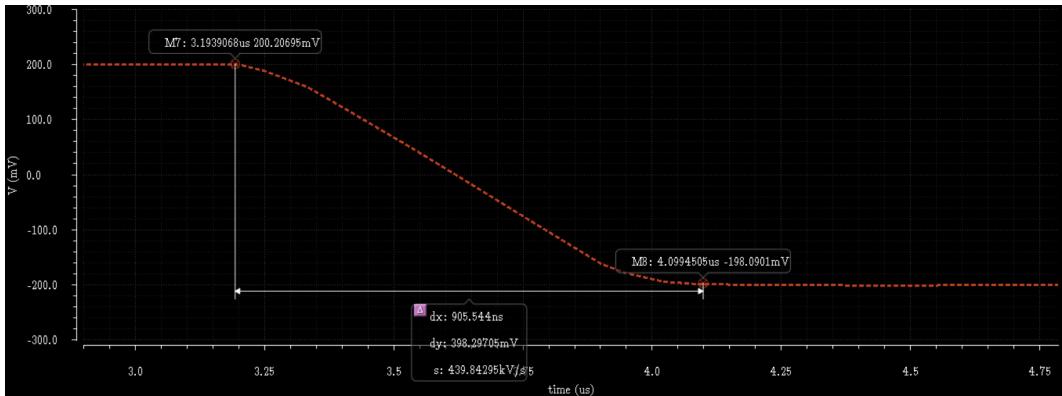
Figure 22: Fall Time  $t_f$ 

Figure 23: Negative Settling Time

because now have bad system performance to reach the 1% of final value.  
 Also for the Slew Rate, both positive and negative, the performance became worse, in fact now have a very deep reduction of about 4 times.

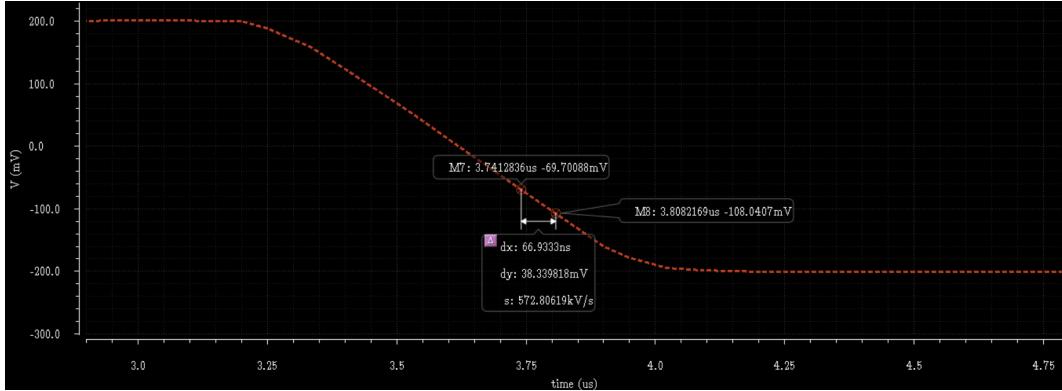


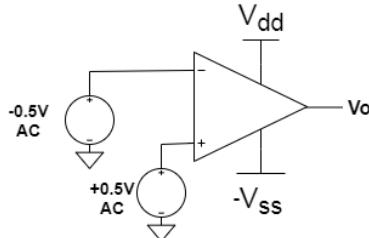
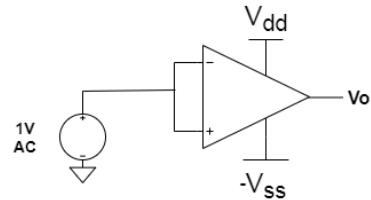
Figure 24: Negative Slew Rate

### Common Mode Rejection Ratio

The CMRR expresses the ability of a differential amplifier to not amplify the common mode signal respect to the differential mode signals.

$$CMRR = \frac{A_d}{A_c} = A_{d,dB} - A_{c,dB} \quad (42)$$

The differential gain was also computed before with previous simulations, figure 25, and it is  $A_d = 107.7 dB$ . Therefore, it is possible now to compute the common gain  $A_c$ , open the loop and consider for both the input generator an AC magnitude= 1 V, figure 26.

Figure 25: Scheme to determine  $A_d$ Figure 26: Scheme to determine  $A_c$ 

Repeat the AC simulation, with range from 1 Hz to 5 MHz, sweep type Logarithmic within 20 points per decade. Thus, proceed Results/Direct plot/AC Gain and Phase of  $V_{out}$  vs  $V_{inp}$  to obtain  $A_c = 59.35 dB$ .

The CMRR became:

$$CMRR = A_{d,dB} - A_{c,dB} = 107.7dB - 59.35dB = 48.35dB \quad (43)$$

The simulated one is lower respect the CMRR computed in the paper, probable due to the different technology used and other performance parameters.

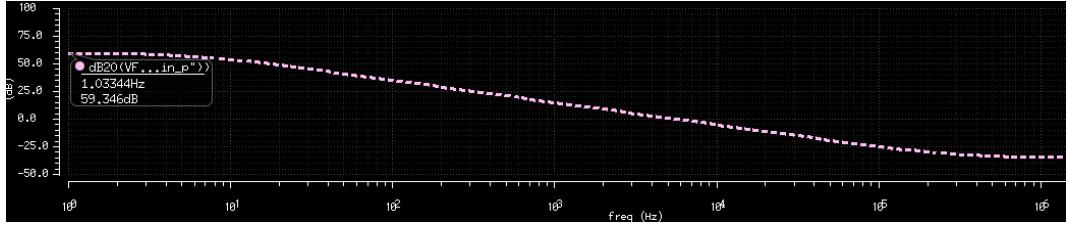


Figure 27: Common Mode Gain

### Common Mode Range

The CMR is the range of values of input voltage for which it is guaranteed that all transistors remains in saturation.

In closed loop configuration, figure 28, it is performed a DC sweep simulation of  $V_{inp}$ , in order to compute both the  $CMR^-$ , the lower limit of the range, and  $CMR^+$ , upper limit to guarantee that the transistors are in saturation range. In figure 29 is possible to see in evidence both these two values.

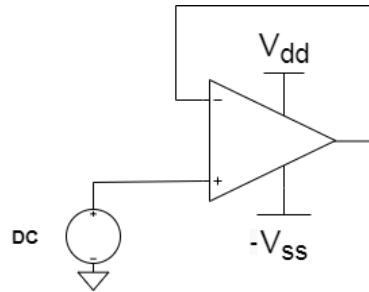


Figure 28: CMR scheme

$$CMR = CMR^+ - CMR^- = 1.214V - (-1.467)V = 2.68V \quad (44)$$

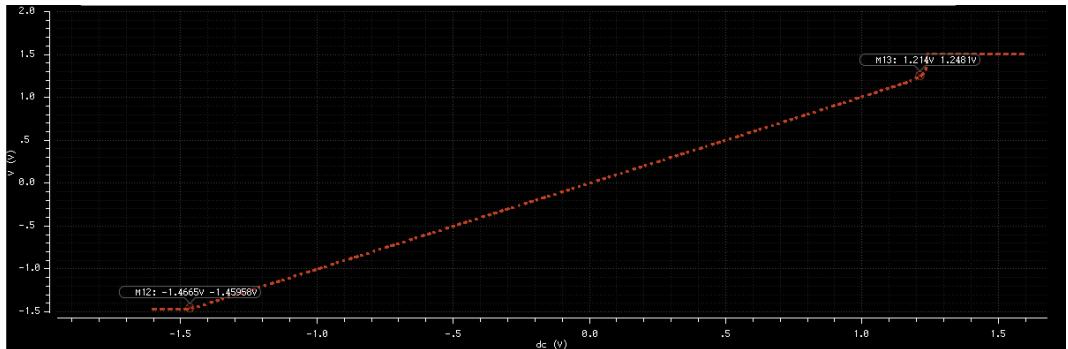


Figure 29: Common Mode Range

### Power Supply Rejection Ratio

The PSRR describe the capability of an electronic circuit to suppress any power supply variations to its output signal. It is defined as the ratio of the change in supply voltage to the equivalent output voltage it produces.

It is possible to analyze this parameter in open loop, imposing AC Magnitude= 1V on the positive power supply, figure 32.

$$PSRR_+ = \frac{A_d}{\frac{dV_o}{dV_{DD}}} \quad (45)$$

The AC simulation is done with always define the same parameters and so it is possible to compute the value of  $\frac{dV_o}{dV_{DD}}$ , like it is possible to see in figure 30.

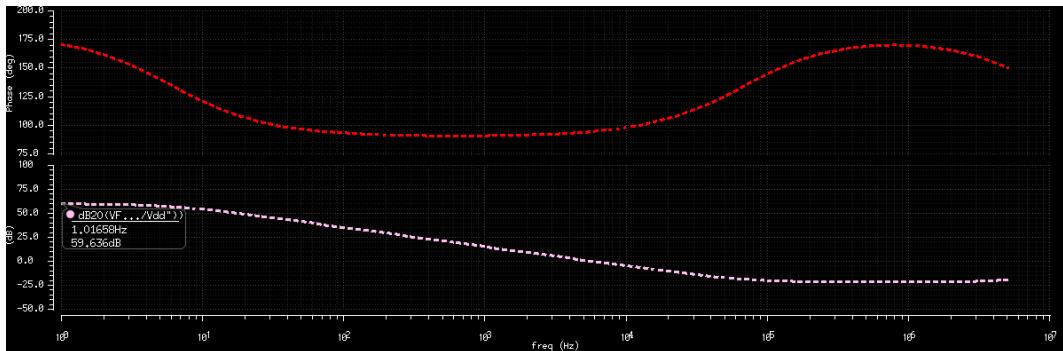


Figure 30: Positive Power Supply Rejection Ratio

Due to the fact that the differential gain is computed previously, so it is possible to have:

$$PSRR_+ = \frac{A_d}{\frac{dV_o}{dV_{DD}}} = 107.7dB - 59.6dB = 48.1dB \quad (46)$$

On the other hand is defined  $PSRR_-$  always in an open loop configuration, figure 33, but imposing AC Magnitude= 1V on the negative power supply.

$$PSRR_- = \frac{A_d}{\frac{dV_o}{d(-V_{SS})}} \quad (47)$$

The AC simulation is done to compute the value of  $\frac{dV_o}{d(-V_{SS})}$ , like it is possible to see in figure 31.

$$PSRR_- = \frac{A_d}{\frac{dV_o}{d(-V_{SS})}} = 107.7dB - 67.3dB = 40.4dB \quad (48)$$

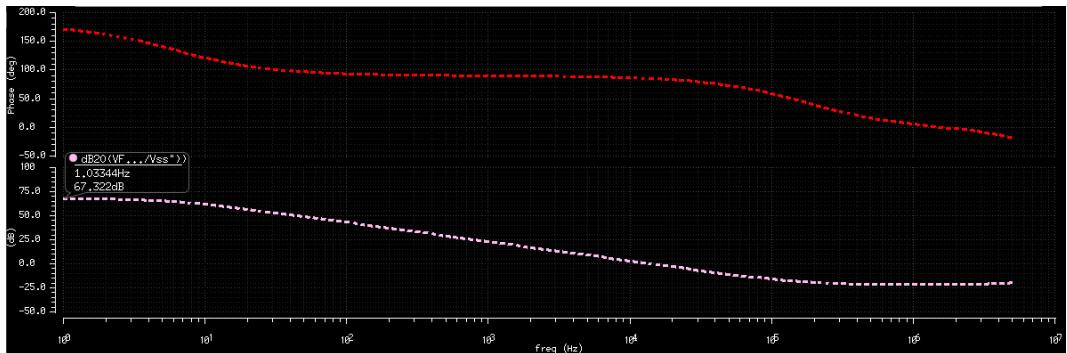
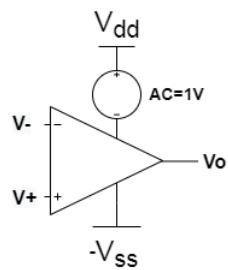
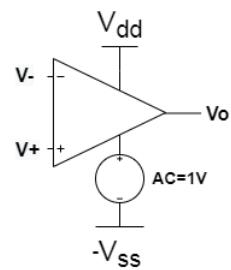


Figure 31: Negative Power Supply Rejection Ratio

Figure 32:  $PSRR_+$ Figure 33:  $PSRR_-$

## 5 Layout

The Layout project is splitted into the three different stages of the OTA, represented in figure 34; the stages were developed one per time by using a divide et impera approach. In order, the first stage, second stage and third stage's layout and simulation are going to be presented.

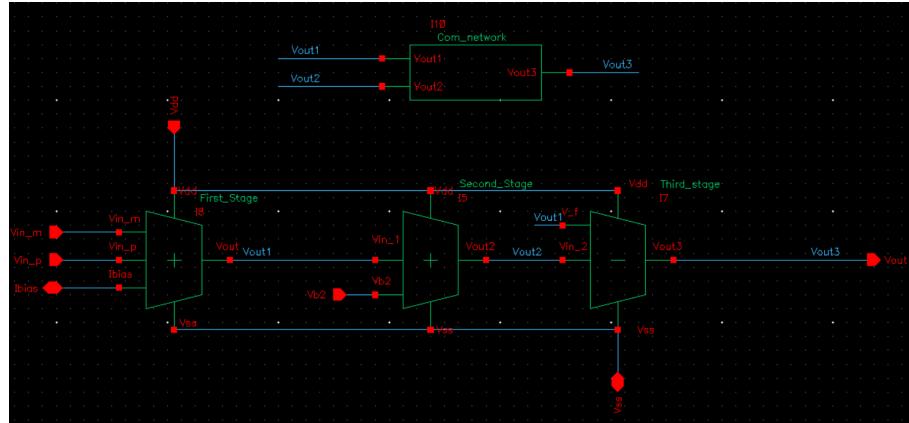


Figure 34: OTA Stages

### 5.1 First Stage

The first stage is composed by a current mirror biasing network and an unbalanced differential pair with active load, as already presented. The goal was the design of a compact and mismatch insensitive layout, to obtain a square structure and so to minimize the chip area.

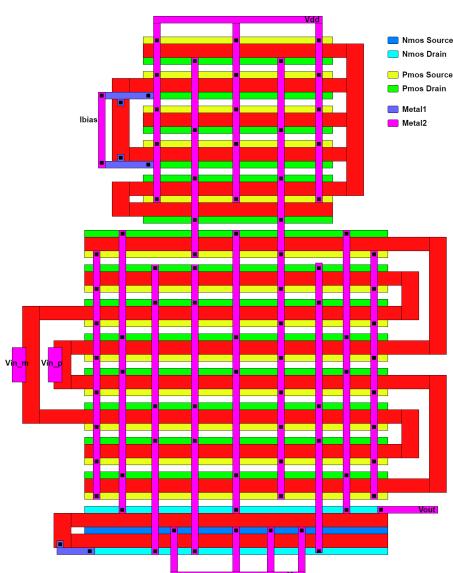


Figure 35: First Stage Stick Diagram.

In order to do that, the biasing network was developed by interdigitating the PMOS transistors belonging to the current mirror. In fact, these transistors have the same dimensions and therefore that structure is feasible. The differential pair was designed by implementing a different structure that is the common centroid, which is better respect to the previous one in terms of robustness to the mismatch effects.

Furthermore, whenever was possible, the transistors were placed in order to share the active areas; for example the two NMOS belonging to the active load share the same source, which it is done for example to reduce the parasitic capacitances referred to the contacts or the total area.

- *PMOS mirror*: it was decided to divide  $M_{01}$  and  $M_0$  respectively in 2 and 4 fingers in order to reduce the total width of the structure. Note that in this way the single finger width is half than the one defined in the schematic. Anyway, since  $M_0$  has a double aspect ratio than  $M_{01}$ , the structure has been interdigitated as ABABAA, where A is associated to  $M_0$  and B to  $M_{01}$ . This is evident also in the figure looking at the connection of  $I_{bias}$  to the  $M_{01}$  drain. Unfortunately, the different transistor dimensions don't allow to make a symmetric interdigitating. To realize it, it should be implemented an  $M_0$  finger with a double width in order to have a structure like ABAB or ABBA.
- *PMOS differential pair*: this time, since the  $M_1$  and  $M_2$  dimensions are the same, the common centroid approach can be perfectly used. In order to make a square structure as much as possible, only 4 fingers has been used for both transistor, using the dimensions as defined on schematic. In this way, the structure has been interdigitated as ABBAABBA, where A is  $M_2$  and B is  $M_1$ .
- *NMOS mirror - pair load*: since their dimensions are not so huge, only 1 finger has been used for both  $M_3$  and  $M_4$ , which share the same source has explained before.

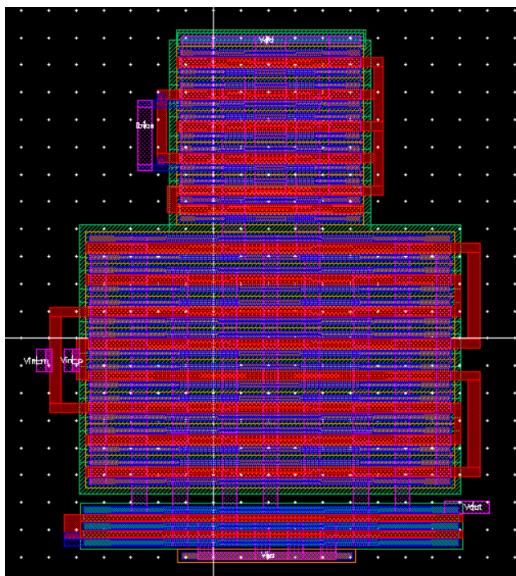


Figure 36: First Stage Layout

Once the transistors position and the routing were defined, the layout design started. The interconnections above the transistors were implemented with the second metal layer called *Metal2*, this due to the impossibility to use the first metal layer because all the active areas have already a *Metal1* contact. Therefore, the *Metal2* was used in order to minimize the interconnections lengths, by implementing them with a straight segment. By looking at the figure, the inputs were placed on left and the output was placed on right, in order to make easier the linking to the next stages. Furthermore, the power supply input was developed by using the ntap, which is useful even to bias the PMOS substrate. An analogue discussion is valid for the NMOS substrate, but the ptap was used to connect it and the circuit to the negative power supply.

Once the layout of the first stage was completed, it is obviously necessary to check if the layout rules are correct, so do the Design Rule Check, **DRC**, to verify it. In order to verify if the layout respects the schematic implementation, it is done the extracted of the structure and so check if it is correct, doing the Layout Versus

### Schematic, LVS.

A simulation environment was prepared to compare the layout vs schematic performances. The symbol is used to simulate the extracted view while the schematic for the circuit without the layout implementation. Due to the mismatches, both implementations didn't have the same bias point and therefore some DC sweep were performed in order to find the two optimum bias points. At the end, the two found values are the following:

- $V_{CM}^{LAYOUT} = 524.7mV$
- $V_{CM}^{SCHEMATIC} = 528mV$

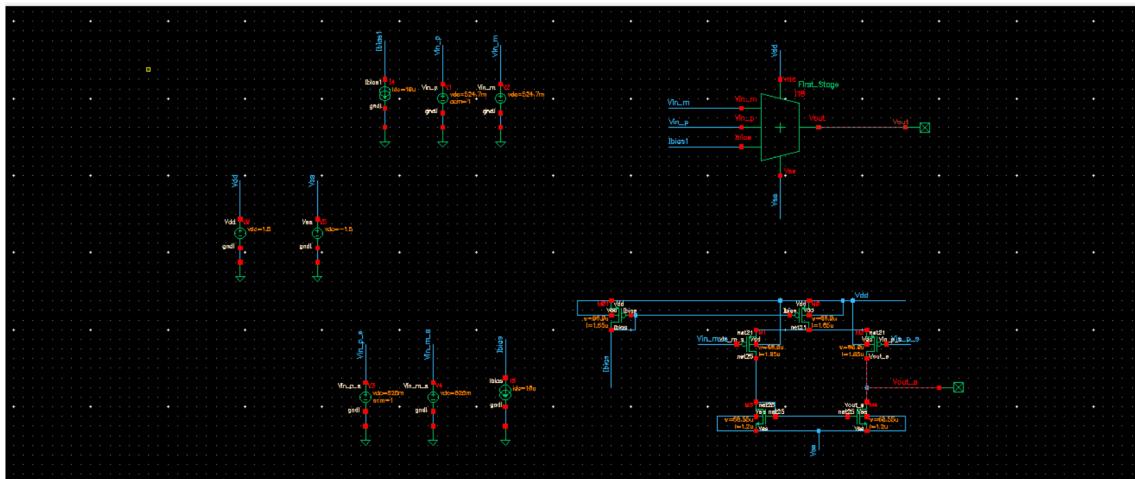


Figure 37: First stage simulation environment

An AC simulation was performed in order to evaluate the gain and bandwidth differences between the two circuits. This to understand how the layout could vary the performances.

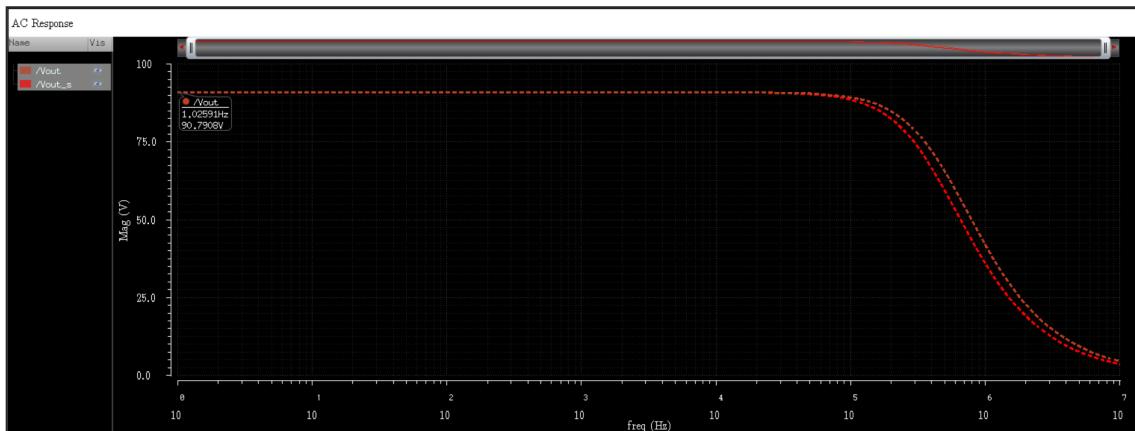


Figure 38: First Stage AC simulation

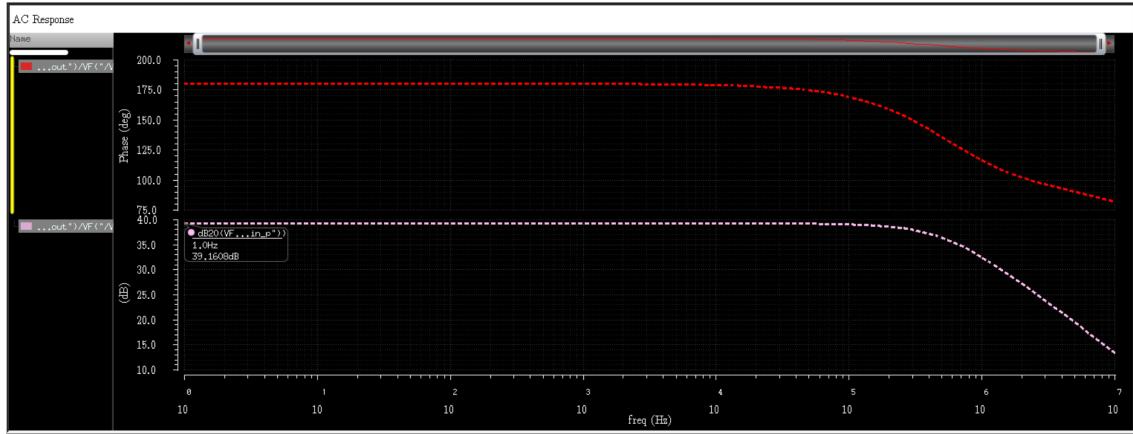


Figure 39: First stage Bode Plot

As the images above shows, the gain is more or less the same in both cases,  $Gain = 39dB$ , but the bandwidth is larger in the circuit with a layout implementation. Maybe it could be due to the pessimistic approach of the simulation environment, in which the parasitic values belonging to the circuit without a layout implementation refer to the worst case. Nevertheless, the bandwidths is almost the same at the value  $525.4kHz$ .

## 5.2 Second Stage

The second stage is composed by a cascade of two common source but connected together by using a PMOS current mirror network: in total there are four transistors.

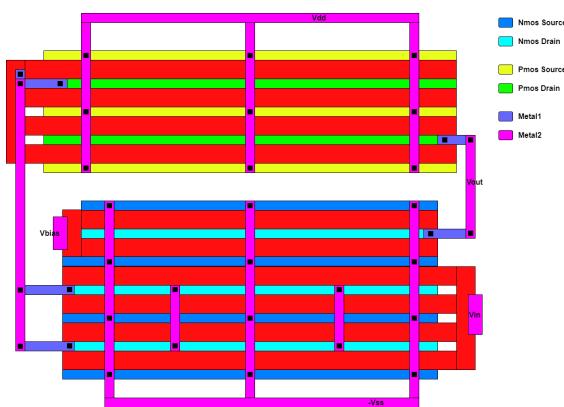


Figure 40: Second Stage Stick Diagram

Both PMOS and NMOS are placed in an active area-sharing way. The four fingers represented at the top in figure 40, compose the PMOS current mirror, while the bottom NMOS transistors are placed by following the same approach.

Nevertheless, the PMOS mirror isn't implemented in an interdigitated way in order to have the possibility to share the drain and source terminals of  $M_6$  and  $M_7$ , in fact the connection is **AABB**, where **A** is  $M_6$  and **B** is  $M_7$ . On the other side, interdigitating  $M_5$  and  $M_8$  it would have been superfluous due to their functionality, since they are two transistors completely separated.

$M_5$  and  $M_8$  were instantiated separately but they were placed in order to share their source. Originally the  $M_5$  and  $M_8$  NMOS transistors should be composed respectively by two and one fingers, but in order to improve the compactness of the

circuit, they were split respectively in to four and two fingers, by reducing their aspect ratio proportionally. It is the main reason why the *Metal2* don't pass on the transistors structure but it gets around the transistors.

The same process has been done also for  $M_6$  and  $M_7$ , using two fingers each.

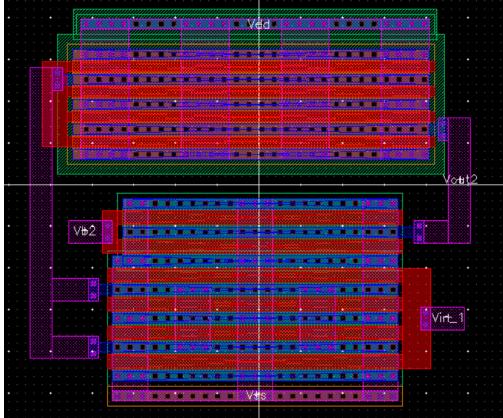


Figure 41: Second Stage Layout

Regarding the pins, due to the routing and in contrast to the first stage, the input pin and the output pin were placed both on right, while the M8 bias pin was placed on left.

As in the first stage, a simulation environment was prepared in order to compare the layout performances with the schematic ones. That environment is represented by the figure 42.

Even for the second stage, some DC sweep were performed in order to evaluate the optimum bias point. In this case even the bias voltage was swept; that due to the mismatches between the schematic and the layout. The found values are reported in table 8:

	$V_{IN,B}$	$V_{BIAS}$
Schematic	$-835.8mV$	$-748mV$
Layout	$-835mV$	$-785.7mV$

Table 8: Second stage bias points.

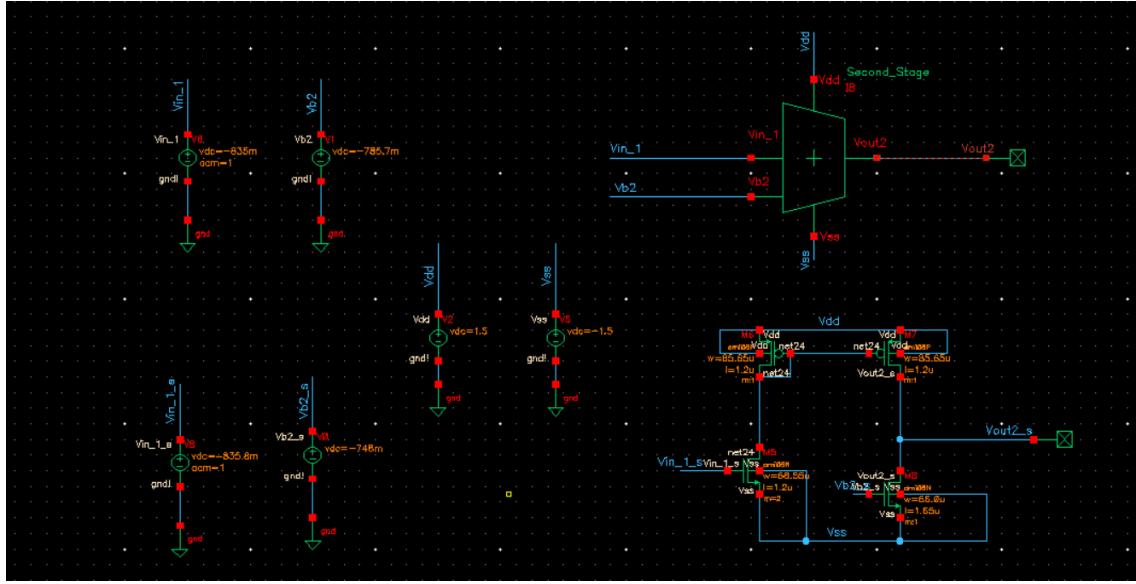


Figure 42: Second stage simulation environment

Even for the second stage, an AC analysis was performed to evaluate the differences of performances of the two implementations. The results are represented in figure 43, in which can be observed that the performances are worse in the layout implementation than in the schematic in terms of gain, but the bandwidth is a little bit larger in the layout case:

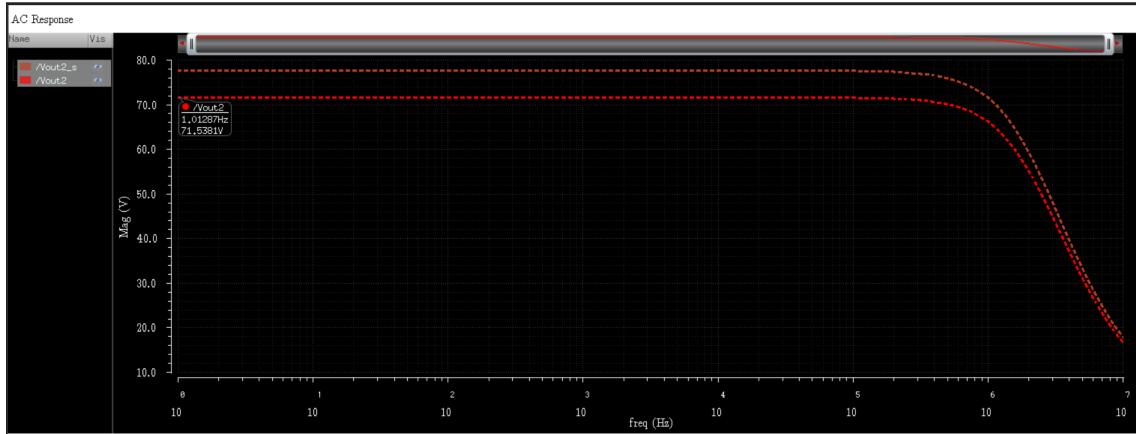


Figure 43: Second Stage AC simulation

By observing the figure 44, the gain and the dominant pole can be extracted:

- $G = 37dB$
- $B_{-3dB} = 2.45MHz$

Both the first and the second stage are the responsible of the high gain of the OTA, in fact the they yield the major gain contribute. Below the second stage Bode plot is showed:

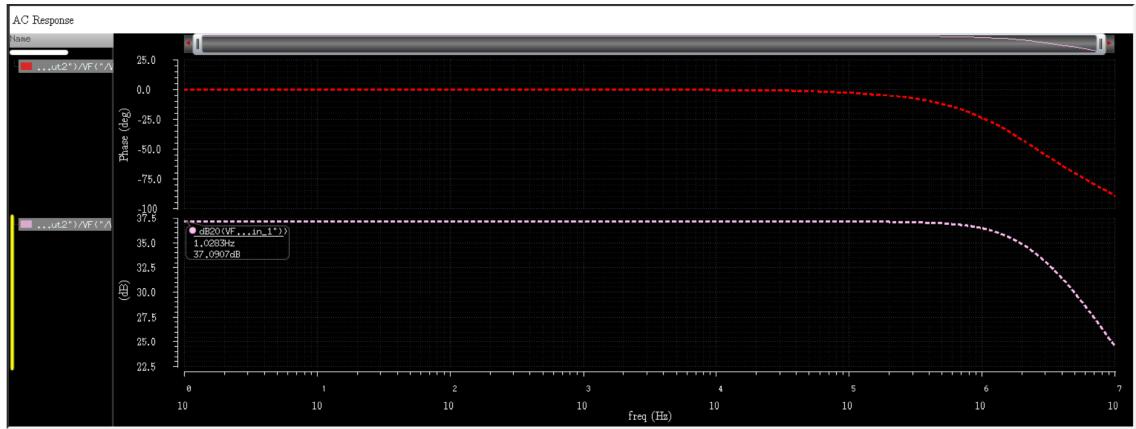


Figure 44: Second stage Bode Plot

### 5.3 Third Stage

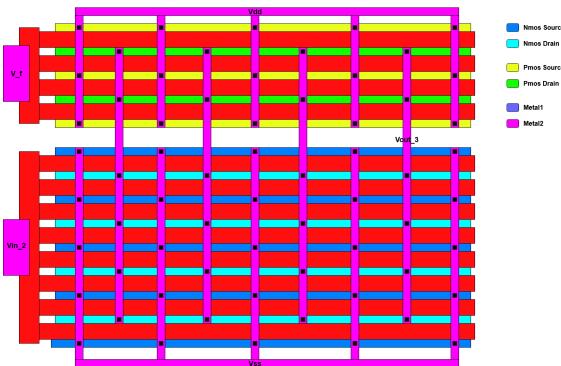


Figure 45: Third Stage Stick Diagram

- *PMOS*: as already mentioned, it is the feed-forward responsible and it is made by four fingers that have the second high aspect ratio 40/0.7
- *NMOS*: it is composed by eight fingers and due to that it has the higher transconductance and the aspect ratios are the same of the previous PMOS.

Even in this case an interdigitated or a common centroid structure were not possible due to the fact that all the fingers of the same transistor should be connected together

by the polysilicon, even on both cases. In this case the routing was developed in a very compact way, the structure is very similar to a square shape and the power supply is equally distributed to the active areas. In fact, by looking to the  $M_9$  transistor, there are five *Metal2* lines that deliver the positive power supply to the finger sources. Also the linking between the two transistors and the routing between the NMOS source and the negative power supply, were designed with the same technique.

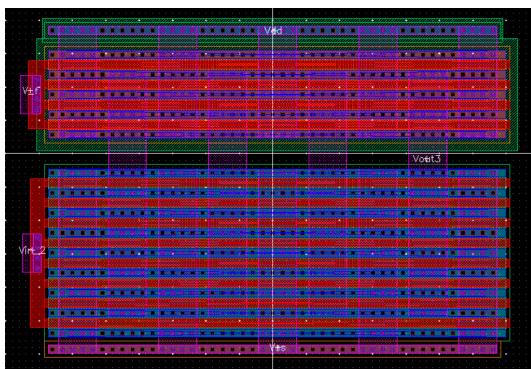


Figure 46: Third Stage Layout

The image in figure 46 shows the third stage final implementation of the layout. As previously said, all the metal lines pass on the transistor structure and the inputs and output pins are in line with the previous stages. In fact the feed-forward input and the transconductor input were placed on the left side, while the third stage output pin was placed on the right, even in this case to make easier the further union of the three stages.

Once the layout was defined and implemented, a simulation environment was created in order to evaluate the differences between the layout and the schematic. Even in this case a DC sweep was performed to bias both the circuit to the optimum point and, the matching is very well, in fact both circuit was biased to the same input voltage:

- $V_{IN,B} = -282mV$

Below, the simulation environment is showed in the figure 47:

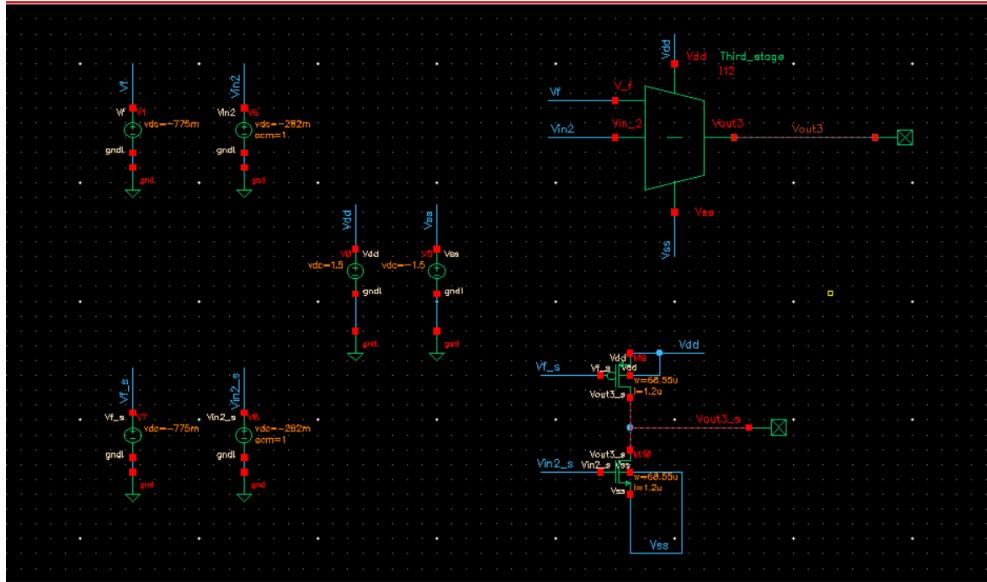


Figure 47: Third stage simulation environment

Next to the optimum bias point finding, an AC analysis was performed to evaluate the gain and bandwidth differences, and even for the third stage, the frequency behavior is better than the schematic, in fact the figure 48 illustrates that the layout implementation has an higher bandwidth respect to the schematic one, as happens for the first stage.

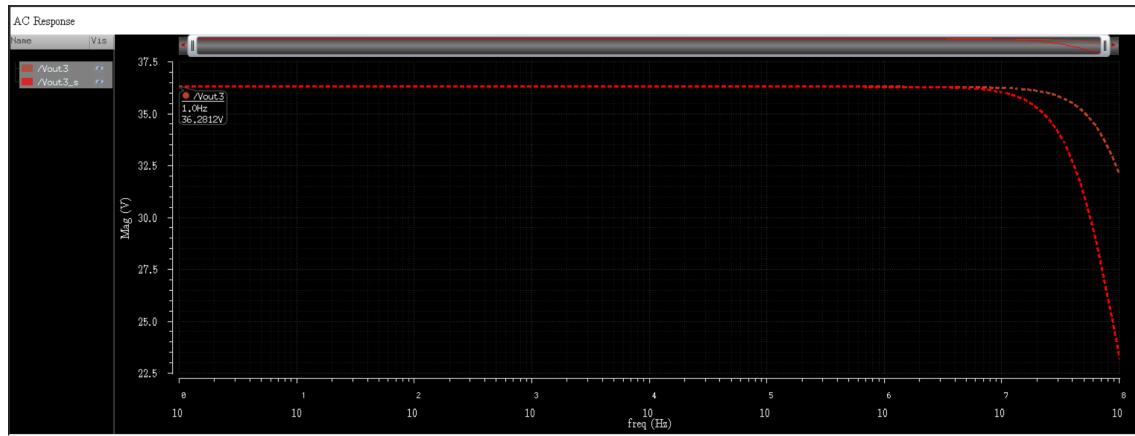


Figure 48: Third Stage AC simulation

In conclusion, the frequency response of the third stage was isolated and the Bode plot evaluated in order to compute the gain and the dominant pole of the circuit:

- $G = 31.19dB$
- $B_{-3dB} = 187.9MHz$

Below, the figure 49 shows the Bode plot of the third stage and, although the third stage is the one with the lowest gain considering all stages, it exhibits the highest bandwidth. Maybe, it is caused by the Miller effect, in fact lower the gain and lower the amplification of the parasitic capacitance referred between the gate and the output of the M10 transistor.

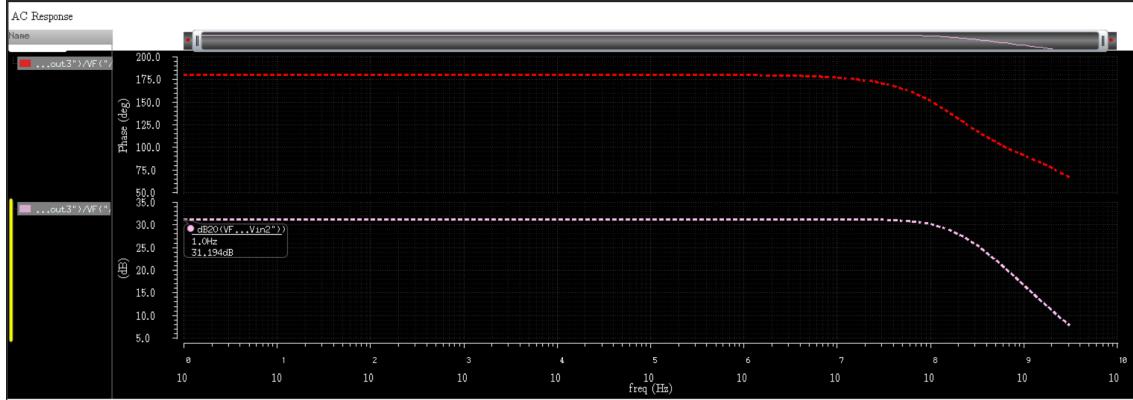


Figure 49: Third stage Bode Plot

## 5.4 Compensation Net

The compensation network was designed in order to obtain the desired gain-bandwidth product of  $F_{GBW} = 1.5MHz$ , and the obtained values are represented in table 7. In order to implement those components, a paper and pencil analysis was fundamental. The first component designed was the  $R_{C2} = 156.2k\Omega$  resistance, by looking to the technological file V37P, the more suitable material was the *Poly2\_HR* which the square resistance is  $R_{\square} = 1076\frac{\Omega}{\square}$ , that is highly adapted to build high value resistances. By using the desired value and the square resistance, the aspect ratio can be evaluated in the following way:

$$\frac{L}{W} = \frac{156.2k\Omega}{1076\frac{\Omega}{\square}} = 145.17 \quad (49)$$

But, by implementing a width  $W = 1.2\mu m$ , the length become  $L = 174.2\mu m$ . That value was quite high and therefore the resistance was divided in ten smaller resistance with a length of  $L = 17.42\mu m$ . After the *Poly2\_HR* with the previous dimensions was instantiated, the obtained resistance value was too high respect to the target and, after some adjustment, the final aspect ratio value per single resistance is  $\frac{L}{W} = 13$ . The basic resistance component is represented in the figure 52 which its the value is  $R_{C2} = 15.5k\Omega$ , and the final result is showed in figure 51 which its value is  $R_{C2} = 155k\Omega$ :

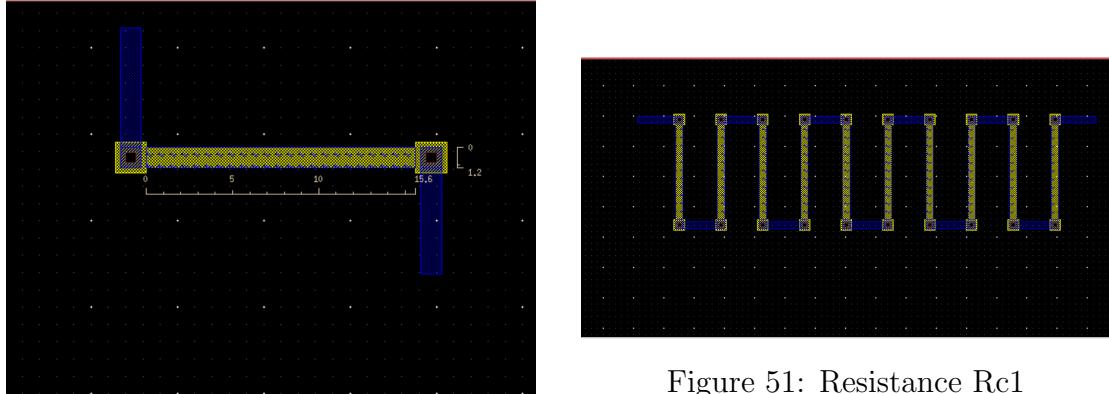


Figure 51: Resistance Rc1

Figure 50: Basic Resistance component

The second component was the resistance  $R_{C1} = 45.8\Omega$ , but in this case the *Poly2\_HR* could not be used due to its too high square resistance, the *Poly1* seemed more suitable with its square resistance of  $R_{\square} = 23.2\frac{\Omega}{\square}$ .

By repeating the same procedure done before, the paper and pencil steps are represented below:

$$\frac{L}{W} = \frac{45.8k\Omega}{23.2\frac{\Omega}{\square}} = 1.97 \quad (50)$$

But, by implementing a width  $W = 4.5\mu m$ , the length become  $L = 8.88\mu m$ .

Even in this case the length should be adjusted in order to reach the optimum available value, that is  $L = 7.35\mu m$ . The aspect ratio was changed and its value now is  $\frac{L}{W} = 1.63$ . The final result is represented in figure 52 and the final resistance result is  $R_{C1} = 45.54\Omega$ :

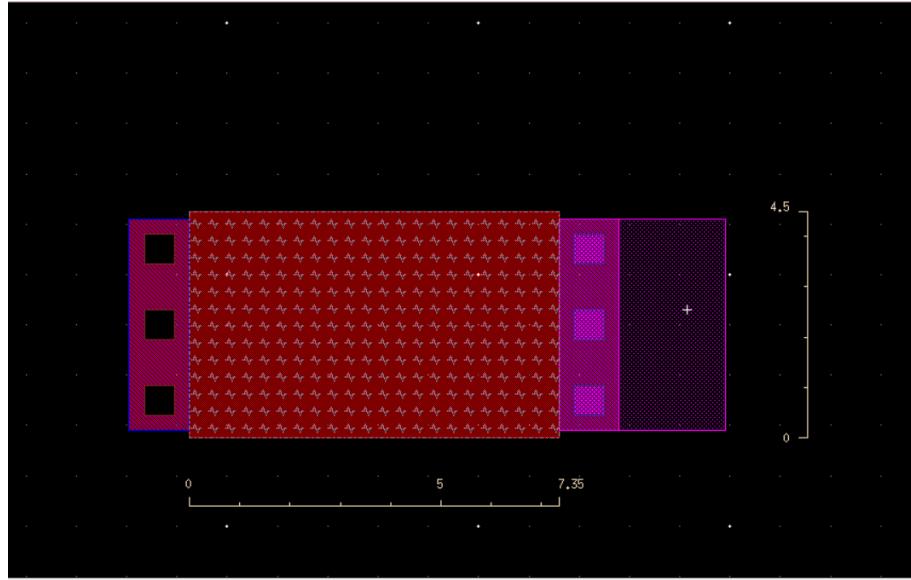


Figure 52: Resistance Rc1

The third component to be designed was the capacitor  $C_{C2} = 145.5fF$  referred to the second stage output. The chosen materials are *Poly1* and *Poly2*, due to their large capacitance per unit area of  $C_{PUA} = 922aF/\mu m^2$ . The procedure to evaluate the edge length of the capacitor is the following:

$$Area = \frac{C_{C2}}{C_{PUA}} = \frac{145500aF}{922aF/\mu m^2} = 157.809\mu m^2 \quad (51)$$

but, in order to obtain the edge value, the square root must be done:

$$Edge = \sqrt{157\mu m^2} = 12.56\mu m \quad (52)$$

When a capacitor with these dimensions was instantiated, the value was not the wanted one, therefore the edges were modified in order to obtain the desired values and, at the end the capacitor dimensions are

- $L = 13.65\mu m$
- $W = 13.35\mu m$

The total area is now  $A = 186.32\mu m^2$ , that is almost 20% higher than the expected one, this means that the capacitors must be modified a lot in order to reach the wanted value. This is less evident in the resistors cases. At the end, the capacitor value is  $C_{C2} = 145.4 fF$ , the final structure can be observed in figure 53

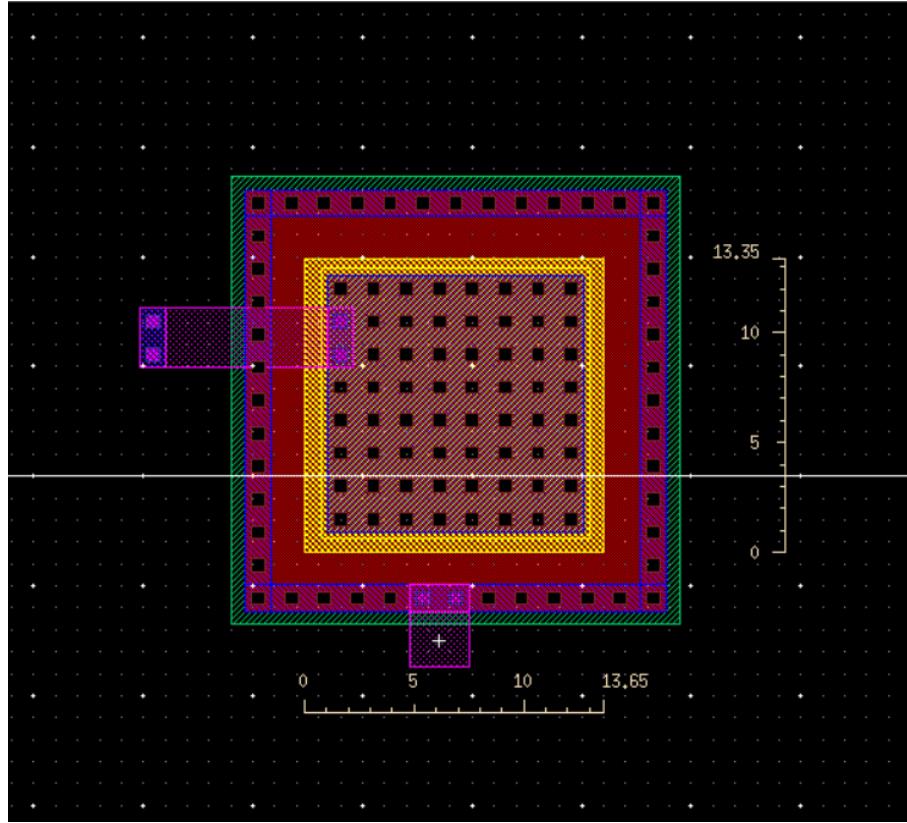


Figure 53: Capacitor Cc2

The fourth component to be designed was the capacitor  $C_{C1} = 12.46 \text{ pF}$  referred between the output and the first stage output. The chosen materials are even in this case, *Poly1* and *Poly2* for the same reasons presented before. The procedure to evaluate the edge length of the capacitor is the following:

$$\text{Area} = \frac{C_{C2}}{C_{PUA}} = \frac{12.46 \cdot 10^6 \text{ aF}}{922 \text{ aF}/\mu\text{m}^2} = 13514.1 \mu\text{m}^2 \quad (53)$$

but, in order to obtain the edge value, the square root must be done:

$$\text{Edge} = \sqrt{13514.1 \mu\text{m}^2} = 116.25 \mu\text{m} \quad (54)$$

When a capacitor with these dimensions was instantiated, the value was not the wanted one, therefore the edges were modified in order to obtain the desired values and, at the end the capacitor dimensions are:

- $L = 125.5 \mu\text{m}$
- $W = 125.4 \mu\text{m}$

The total area is now  $A = 15487.8\mu m^2$ , that is 14.6% higher than the expected one. At the end, the capacitor value is  $C_{C2} = 12.46pF$ , the final structure can be observed in figure 54

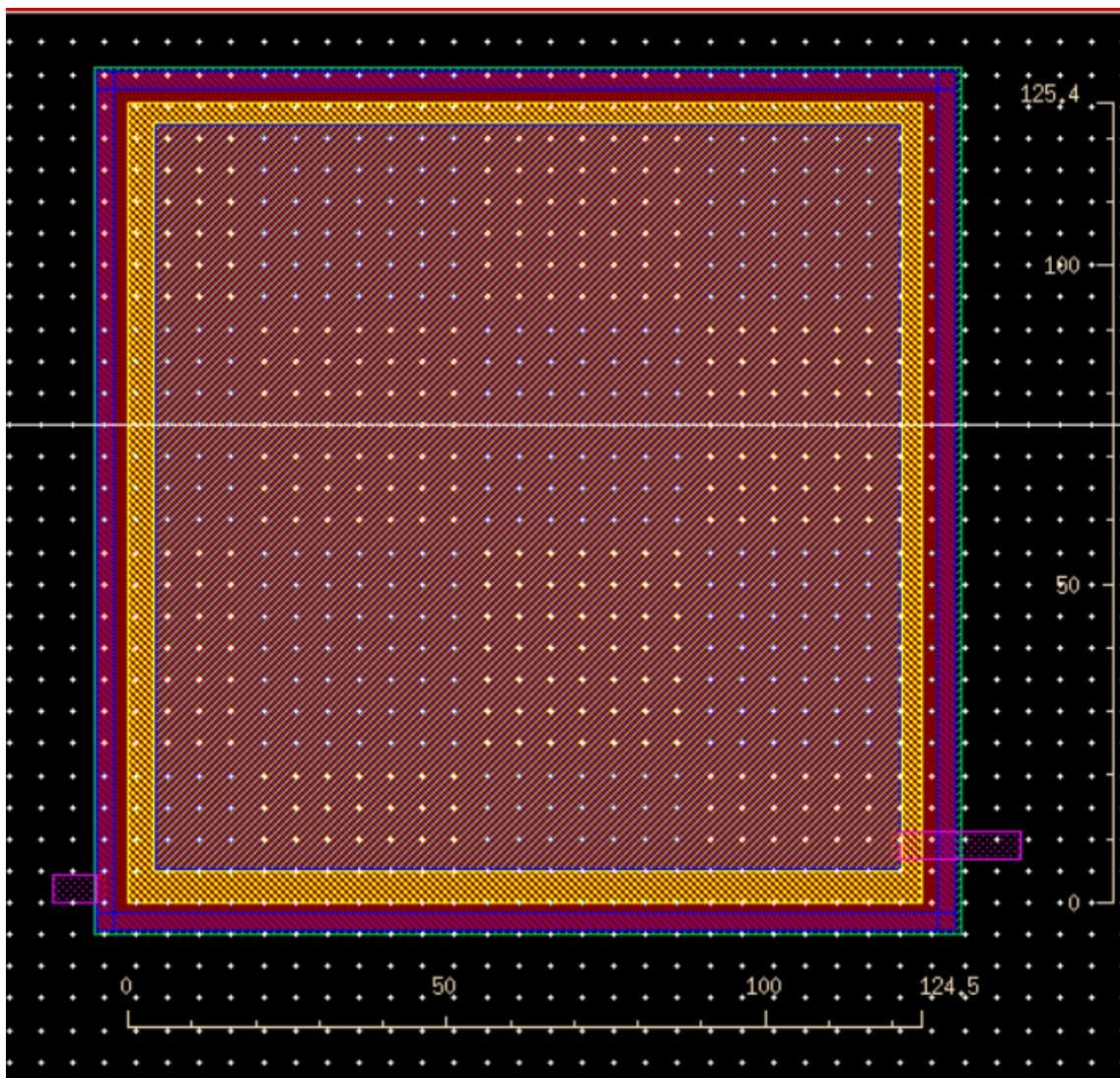


Figure 54: Capacitor Cc1

In the image 55 can be observed the complete scheme of the compensation network, in which all the component are connected together:

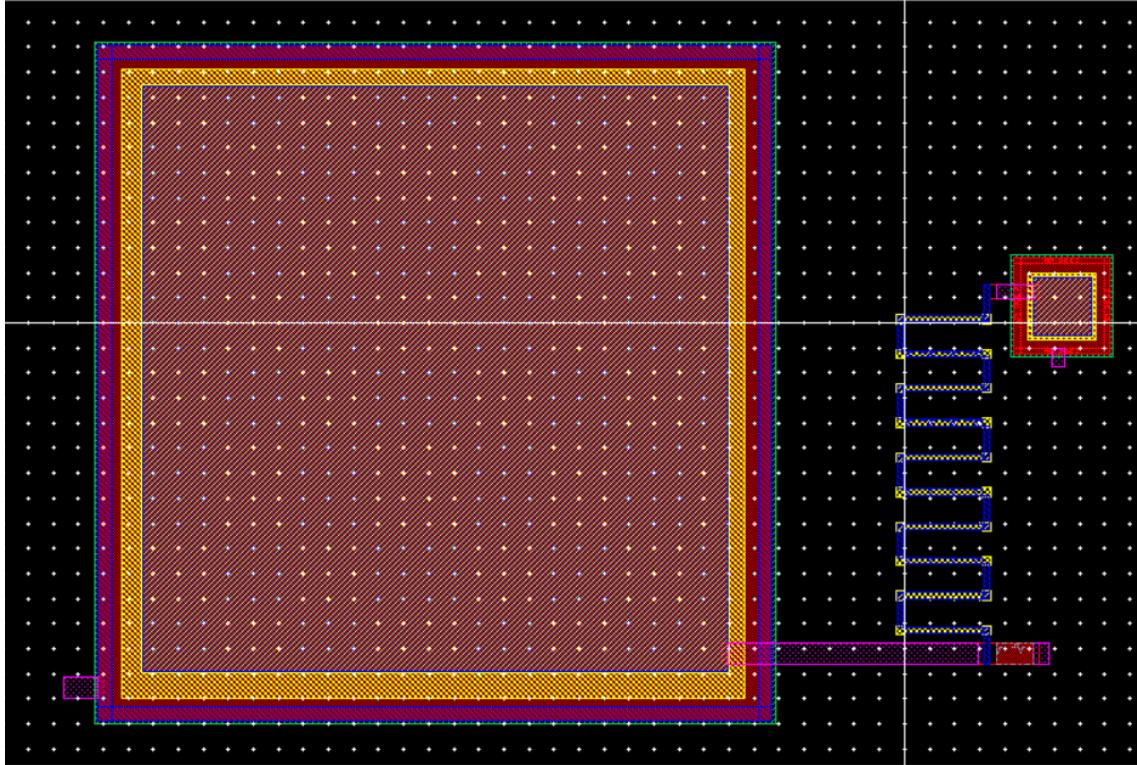


Figure 55: Compensation Network LAYOUT

## 5.5 Final Layout

All the different stages and the compensation net are connected together in order to reduce much as possible the connections length, the total area and the parasitic parameters. It is also tried to have a square structure so as better occupy the possible area of the chip, in figure 56.

The *Metal2* is used to connect together the positive power supply of every stage,  $V_{DD}$ , and also for the negative one  $V_{SS}$ , and all the other connections where it was possible to use. But, it was necessary to exploit also *Metal3* to connect each other all the three stages and the two compensation capacitance, because it was the only way to connect all without exploiting any long or complex routing.

At last the Layout area is estimated using the ruler to obtain the total dimension of the chip.

It is possible to notice, in figure 58, that the base=  $241.95 \mu m$  while the height=  $(477.6 - 241.95) \mu m = 235.65 \mu m$ , to obtain a total area=  $0.057 mm^2$ , less than the nominal one of the paper, because the compensation capacitance used are smaller respect the ones of the paper, that it has been said equal to about the 80% of the total Layout area. Therefore the area is almost 24% less than the paper one, and

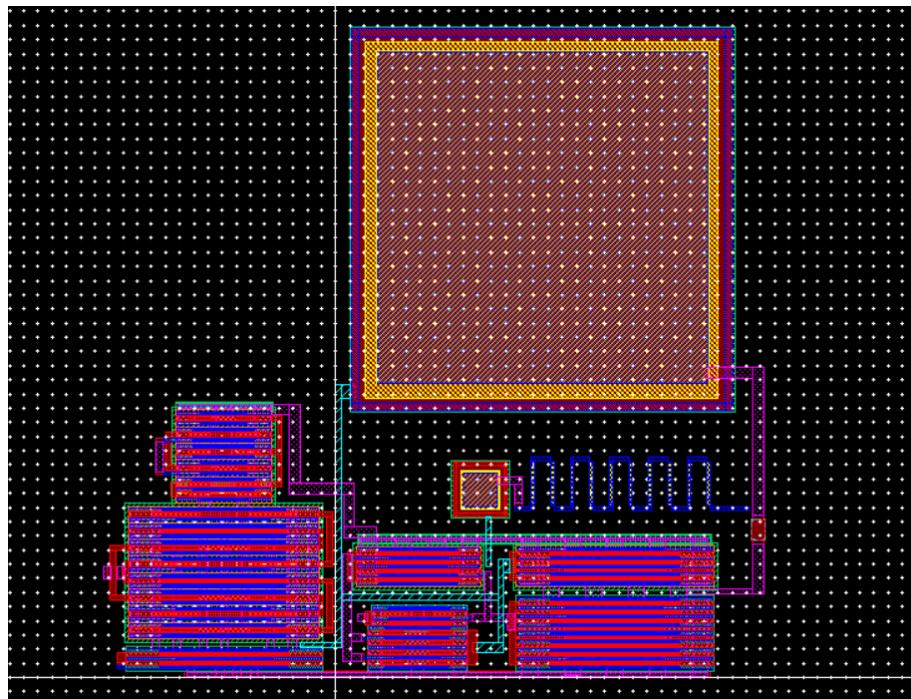


Figure 56: OTA LAYOUT

the compensation network now, occupies a total amount of area  $A_{CNET} = 144.6\mu m \cdot 176.4\mu m = 0.0255mm^2$  which correspond to the 44.7% of the total OTA's area, as showed in figure 57:

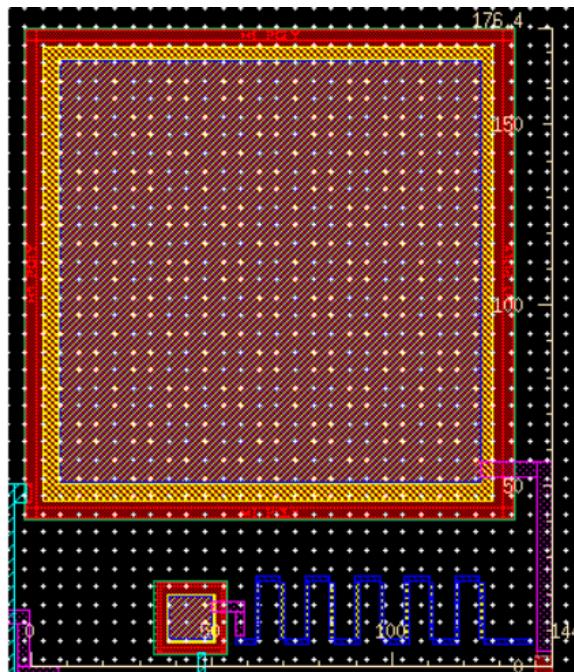


Figure 57: Compensation Network measuring

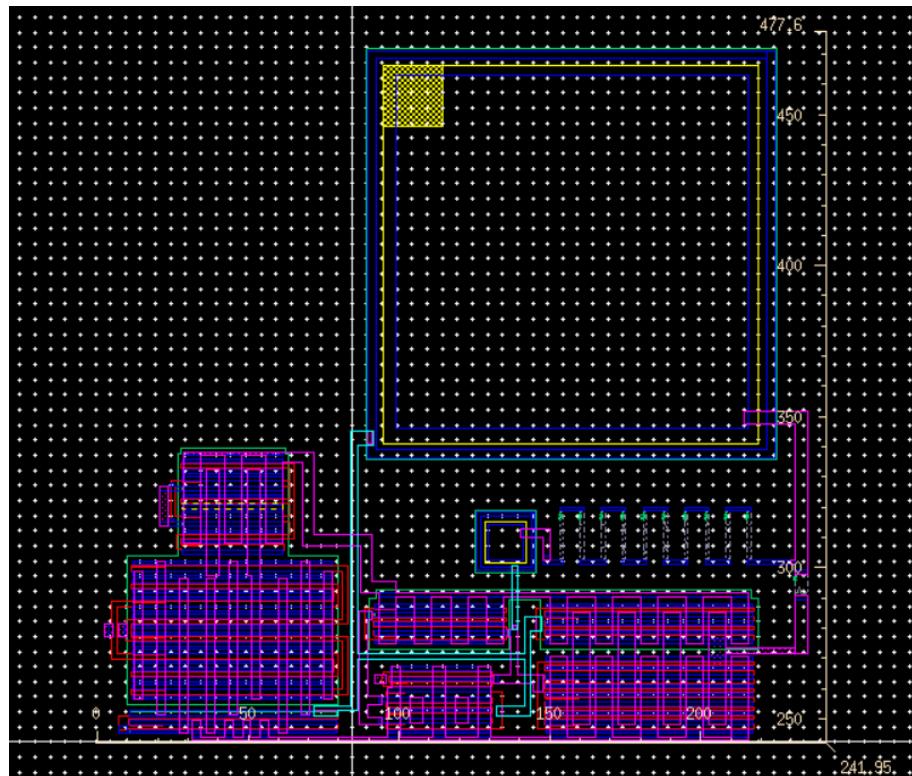


Figure 58: LAYOUT Dimension

The extracted view is obtained in order to do the simulations of the layout, figure 59.

Also the symbol view is made, obviously to connect all the generators and proceed with the simulations, figure 60.

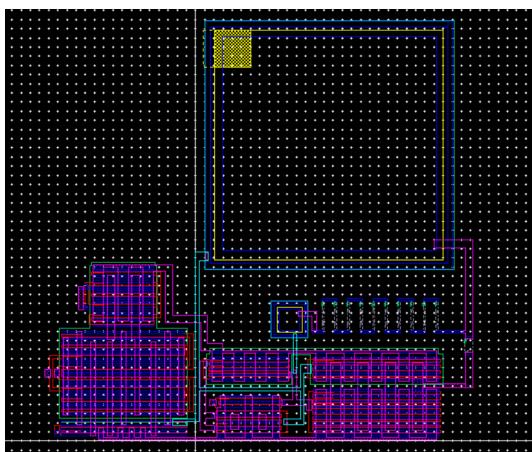


Figure 59: Extracted OTA

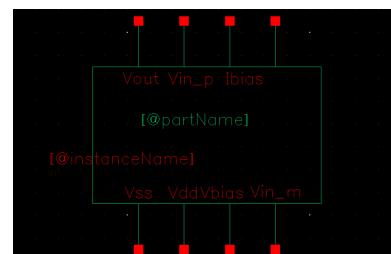


Figure 60: OTA Symbol View

## 5.6 Simulations

Layout is simulated to understand the behaviour under different conditions, to analyze the performance parameters, all at the temperature of  $T = 27^\circ$  and therefore compare it with the ones described in the 4.1 and after with the results of the paper. All the simulations are done on the extracted file that it is possible to create from the Layout and add into the simulations environment.

### DC Sweep

At first it is performed a DC sweep analysis in order to understand the correct working point for the  $V_{b2}$  and  $V_{inp}$  generators.

The two input generators are imposed to be equal,  $V_{inp} = V_{inm}$ , so the two pins are connected together, and at last proceed with the simulation.

Launch simulation following the same step as the schematic one. Therefore, choose Analysis/DC/Component parameter and select at first  $V_{b2}$  generator to sweep, with start-stop of  $-1.6V$  and  $+1.6V$ , step size of  $0.5 m$  and linear sweep type. At last select the output  $V_{out}$  and from the behaviour in figure 61, the optimum bias point found is  $V_{b2} = -785.7 mV$ .

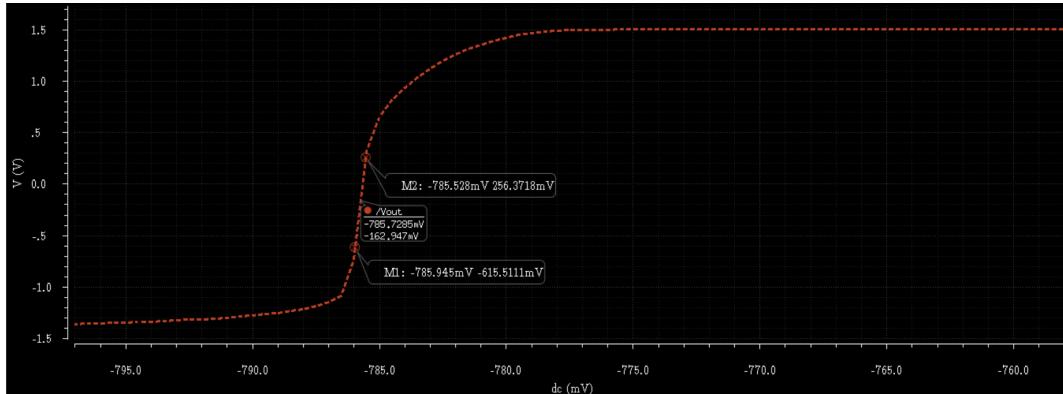


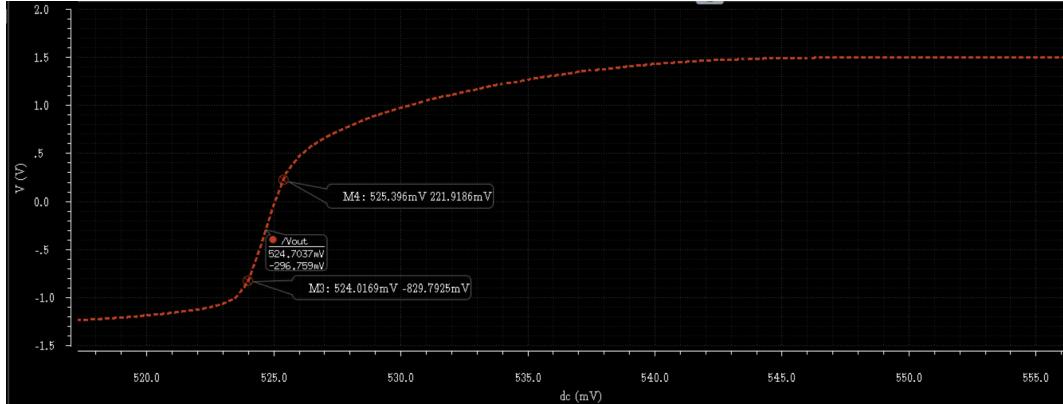
Figure 61: DC sweep of  $V_{b2}$

The sweep simulation is also repeated to obtain a  $V_{inp} = 524.7 mV$ , in figure 62.

These two results are obviously a little different respect the schematic ones, due to the possible parasitics effects introduced by the layout.

### Input Offset Voltage

To perform this simulation, set  $V_{out} = V_{inm}$  (closed loop configuration) and  $V_{inp}$  with DC Voltage= 0 and also AC Magnitude= 0. Launch the simulation in order to obtain the operating point, so when it is finished choose Results/Print/DC Node Voltage and select  $V_{out}$ . Therefore, the input offset voltage is equal to  $-275 \mu V$ , that it is generally a very small value for an OTA offset. This value results almost equal to the one obtained for the schematic.

Figure 62: DC sweep of  $V_{inp}$ 

### AC Open Loop

Simulation in open loop is done to obtain gain and phase. Therefore, Choose Analysis/AC, sweep variable is the frequency, with a range from  $1\text{ Hz}$  to  $5\text{ MHz}$ , sweep type Logarithmic within 20 points per decade. Thus, proceed Results/Direct plot/AC Gain and Phase of  $V_{out}$  vs  $V_{inp}$ , in figure 63.

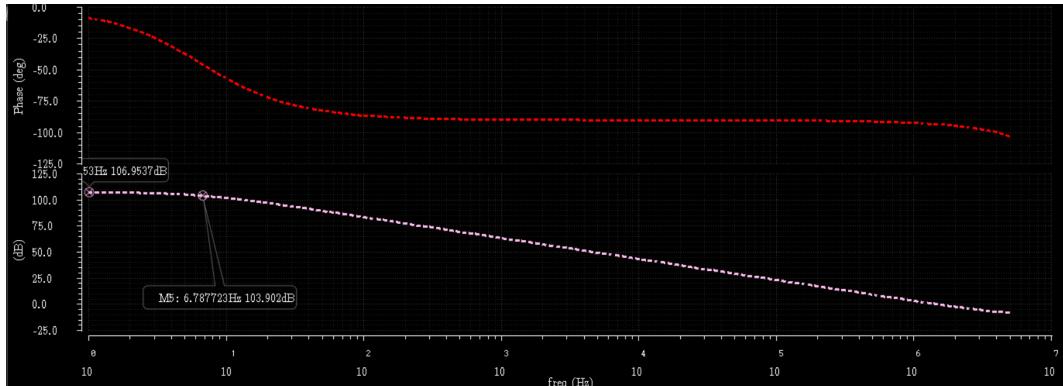


Figure 63: AC Gain in Open Loop

Notice that the DC open loop gain is  $107\text{ dB}$ , while the first pole has  $f = 6.6\text{ Hz}$  corresponding at gain  $104\text{ dB}$ . At last the transition frequency, the frequency when the gain equal to  $0\text{ dB}$ ,  $f_T = 1.54\text{ MHz}$  at the phase  $-93.4^\circ$ . In this situation is possible to understand that the phase margin,  $PM = (180 - 93.4)^\circ = 86.6^\circ$ , very large value so the system is in stability, in figure 64.

The compensation works again correctly, in fact 2 poles are canceled by two zeros, so is possible to notice first order behaviour of the system.

The DC gain and PM obtained are quite similar to the ones obtained during the schematic simulation.

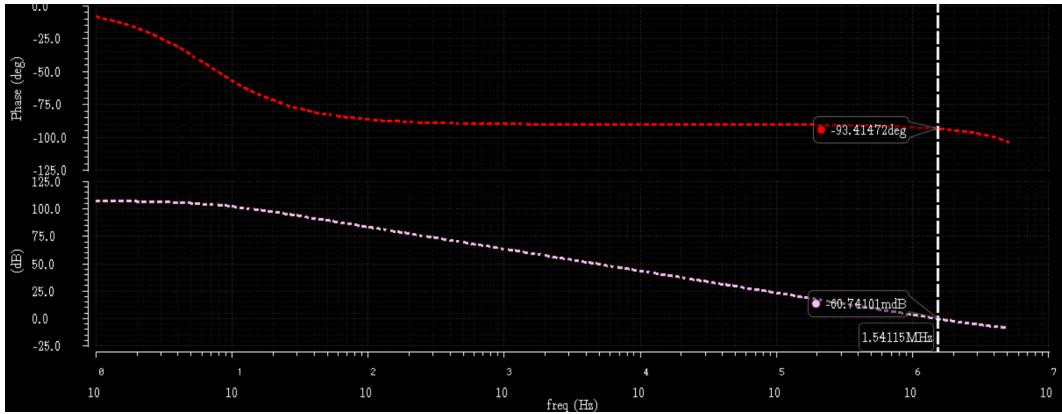


Figure 64: Phase in Open Loop

### Closed Loop

In order to obtain the GBW is used the closed loop configuration, and there are repeated the same simulations steps done before in open loop. On the other hand, the cut frequency,  $f_T(-3dB) = 1.71 MHz$  with a phase=50.2°,in figure 65.

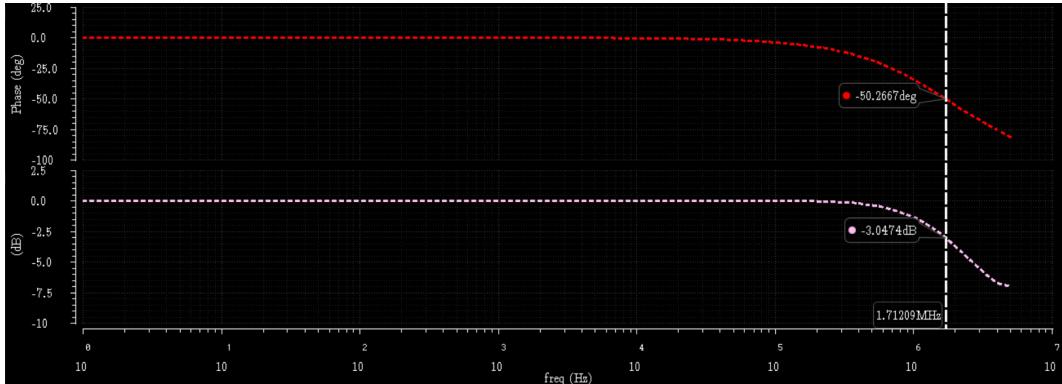


Figure 65: GBW

### Step Response

The step is now applied on the input  $V_{inp}$ , with a  $V_{pulse}$  generator, setting the input voltage step to  $-200 mV$  and  $200 mV$ , rise time and fall time equal to  $700 ns$ , pulse width=  $2.5 \mu s$  and delay=  $6 \mu s$ . Launch ADE-L, chose a tran simulation with a stop time=  $100 \mu s$  and select  $V_{out}$ .

Computing the value in the linear region is possible to obtain the rise time, in the  $10\% - 90\%$  of the transient response, so  $t_r = 583.56 ns$ , in figure 66.

The settling time, the time required for the response curve to reach and stay within a range of certain percentage,  $1\%$  of the final value. In figure 67, is possible to highlight that is equal to  $942.3 ns$ .

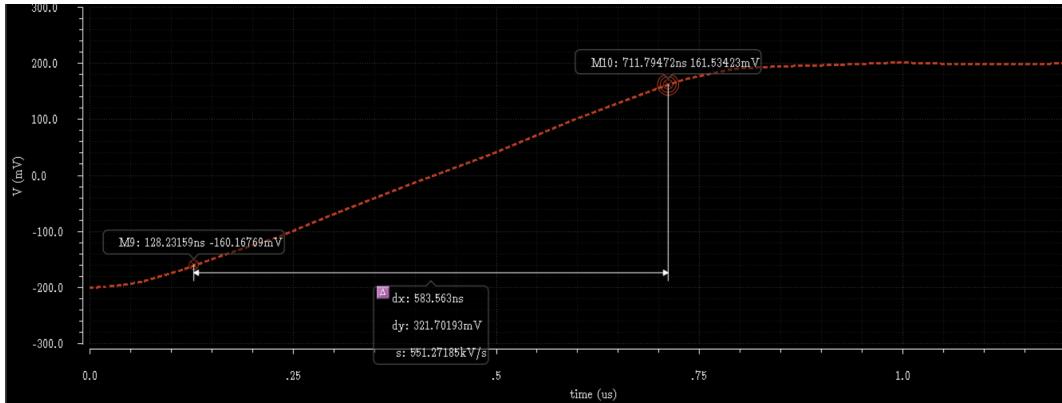
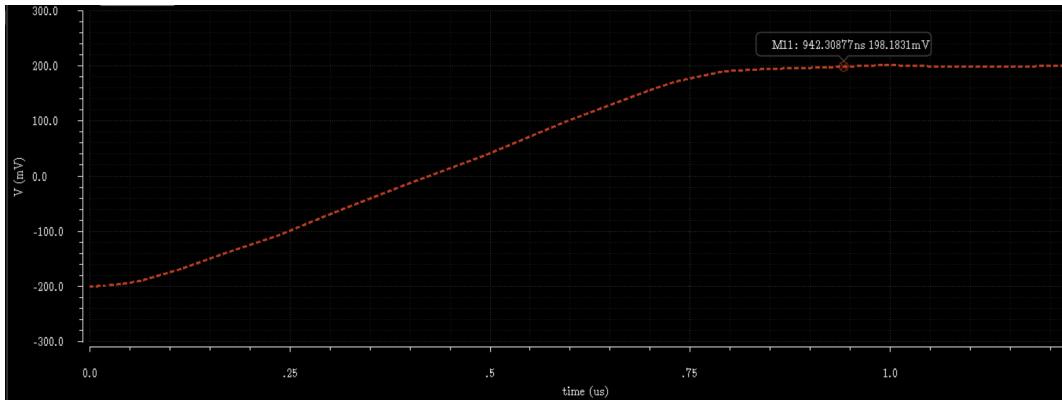
Figure 66: Rise Time  $t_r$ 

Figure 67: Positive Settling Time

At last the slew rate, defined as the rate of change of the voltage per unit time, is computed,  $SR_+ = 0.58 \text{ V}/\mu\text{s}$ , in figure 68.

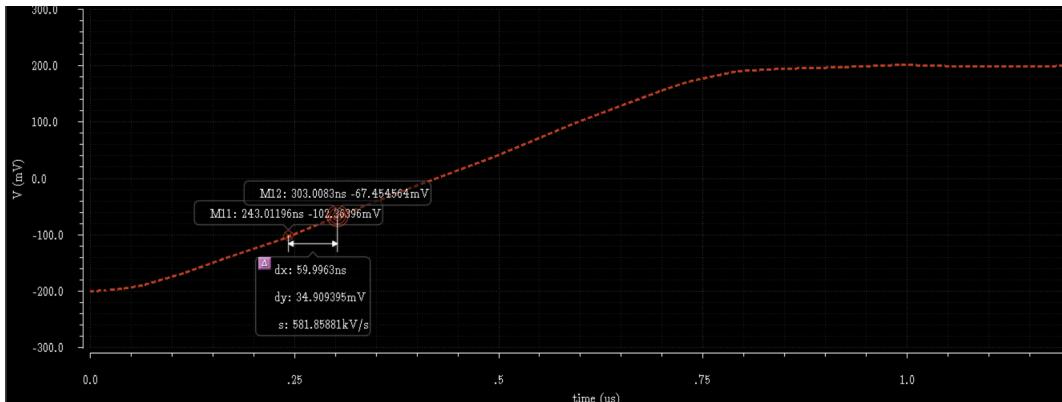


Figure 68: Positive Slew Rate

All these parameters are also computed for the falling edges, as fall time  $t_f = 575.21 \text{ ns}$ , figure 69, negative settling time  $972.3 \text{ ns}$  in figure 70, and negative slew rate  $SR_- = 0.61 \text{ V}/\mu\text{s}$  in figure 71.

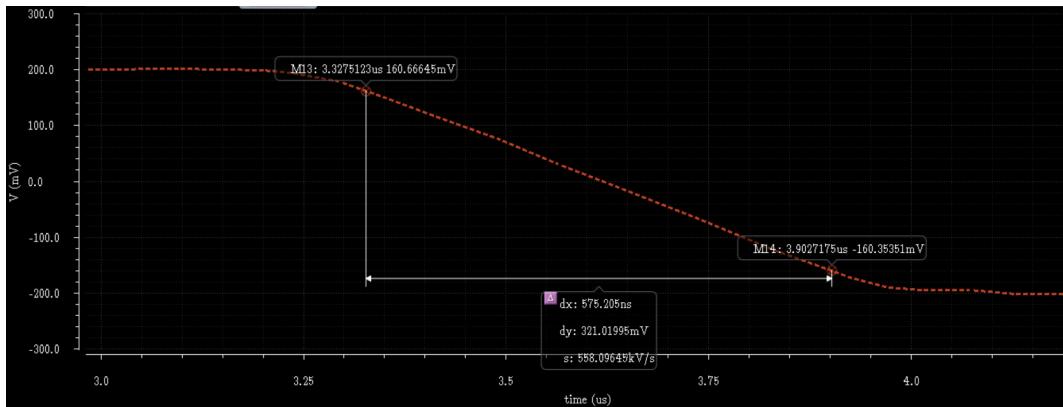
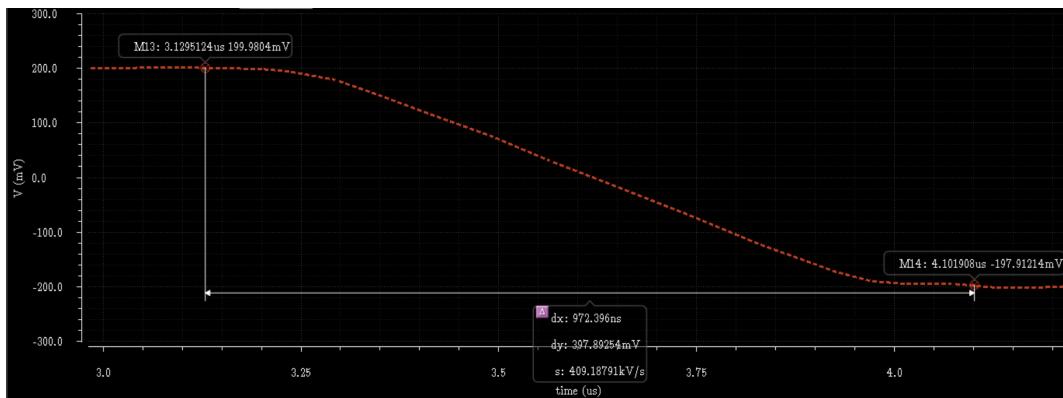
Figure 69: Fall Time  $t_f$ 

Figure 70: Negative Settling Time

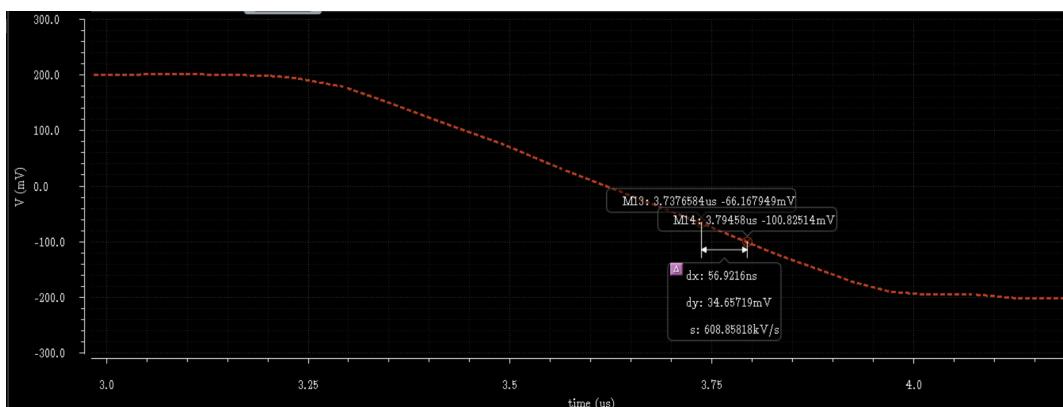


Figure 71: Negative Slew Rate

All the results obtained are quietly similar to the schematic ones.

### Common Mode Rejection Ratio

The CMRR expresses the ability of a differential amplifier to not amplify the common mode signal respect to the differential mode signals.

$$CMRR = \frac{A_d}{A_c} = A_{d,dB} - A_{c,dB} \quad (55)$$

The differential gain was also computed before with previous simulations, and it is  $A_d = 107 dB$ . Therefore, it is possible now to compute the common gain  $A_c$ , open the loop and consider for both the input generator an AC magnitude= 1 V. Repeat the AC simulation, with range from 1 Hz to 5 MHz, sweep type Logarithmic within 20 points per decade. Thus, proceed Results/Direct plot/AC Gain and Phase of  $V_{out}$  vs  $V_{inp}$  to obtain  $A_c = 58.6 dB$  , in figure 72.

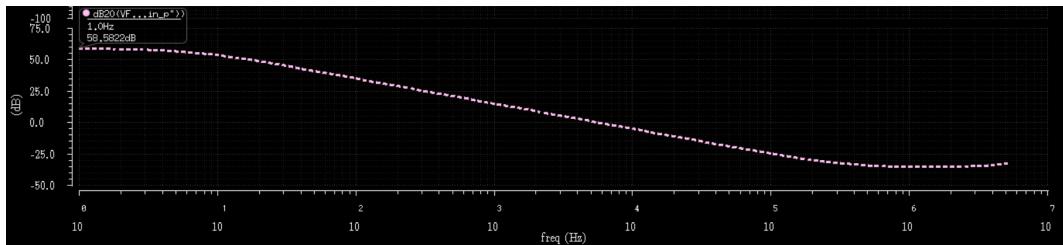


Figure 72: Common Mode Gain

The CMRR became:

$$CMRR = A_{d,dB} - A_{c,dB} = 107 dB - 58.6 dB = 48.4 dB \quad (56)$$

### Common Mode Range

The CMR is the range of values of input voltage for which it is guaranteed that all transistors remains in saturation.

In closed loop configuration it is performed a DC sweep simulation of  $V_{inp}$ , in order to compute both the  $CMR^-$ , the lower limit of the range, and  $CMR^+$ , upper limit to guarantee that the transistors are in saturation range. In figure 73 is possible to see in evidence both these two values.

$$CMR = CMR^+ - CMR^- = 1.209V - (-1.474)V = 2.683V \quad (57)$$

### Power Supply Rejection Ratio

The PSRR describe the capability of an electronic circuit to suppress any power supply variations to its output signal. It is defined as the ratio of the change in supply voltage to the equivalent output voltage it produces.

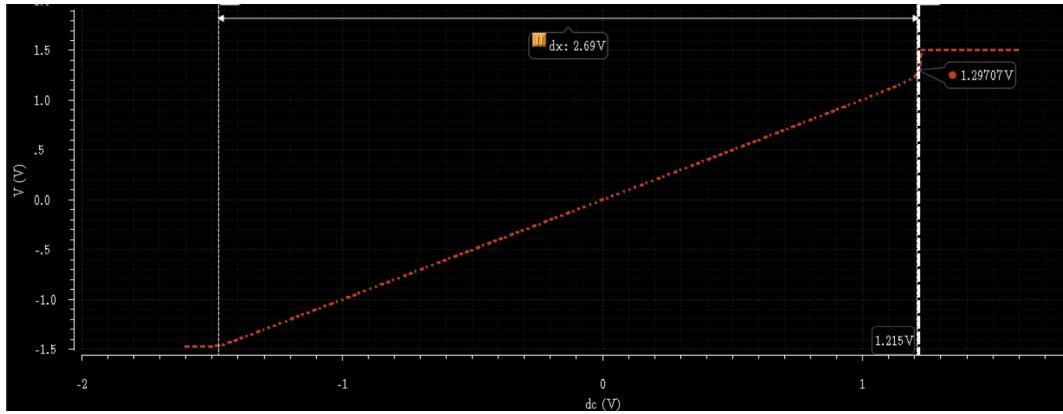


Figure 73: Common Mode Range

It is possible to analyze this parameter in open loop, imposing AC Magnitude= 1V on the positive power supply.

$$PSSR_+ = \frac{A_d}{\frac{dV_o}{dV_{DD}}} \quad (58)$$

The AC simulation is done with always define the same parameters and so it is possible to compute the value of  $\frac{dV_o}{dV_{DD}}$ , like it is possible to see in figure 74.  
Due to the fact that the differential gain is computed previously, so it is possible to have:

$$PSRR_+ = \frac{A_d}{\frac{dV_o}{dV_{DD}}} = 107 \text{ dB} - 58.8 \text{ dB} = 48.2 \text{ dB} \quad (59)$$

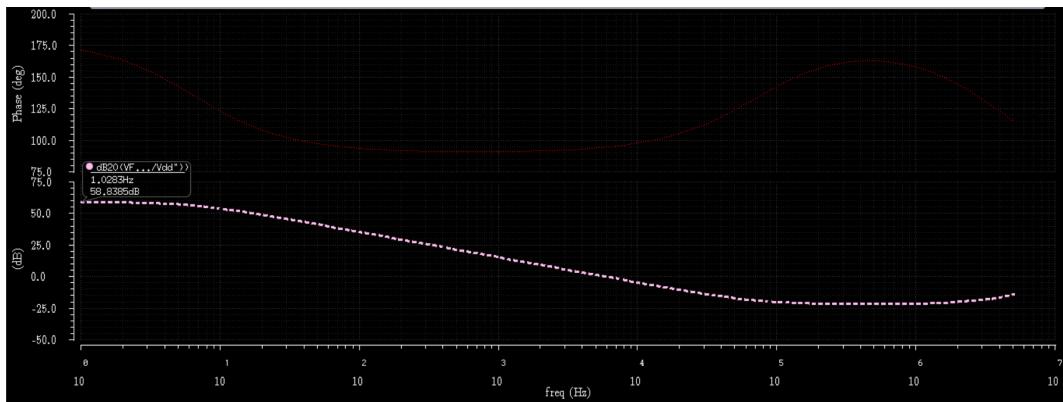


Figure 74: Positive Power Supply Rejection Ratio

On the other hand is defined  $PSRR_-$  always in an open loop configuration, but

imposing AC Magnitude= 1V on the negative power supply.

$$PSRR_- = \frac{A_d}{\frac{dV_o}{d(-V_{SS})}} \quad (60)$$

The AC simulation is done to compute the value of  $\frac{dV_o}{d(-V_{SS})}$ , like it is possible to see in figure 75.

$$PSRR_- = \frac{A_d}{\frac{dV_o}{d(-V_{SS})}} = 107 dB - 67.2 dB = 39.8 dB \quad (61)$$

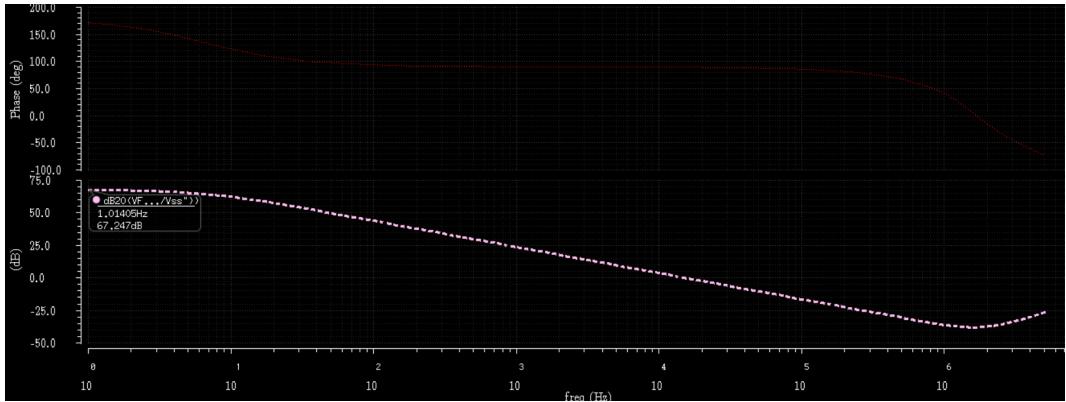


Figure 75: Negative Power Supply Rejection Ratio

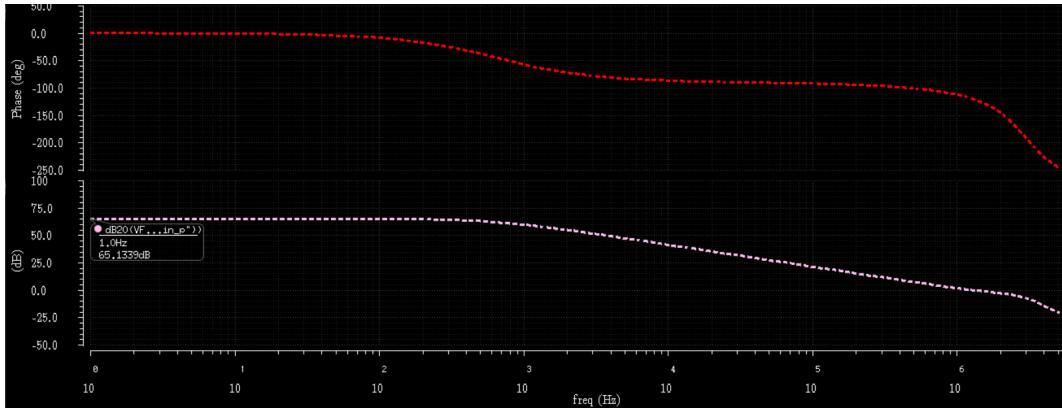
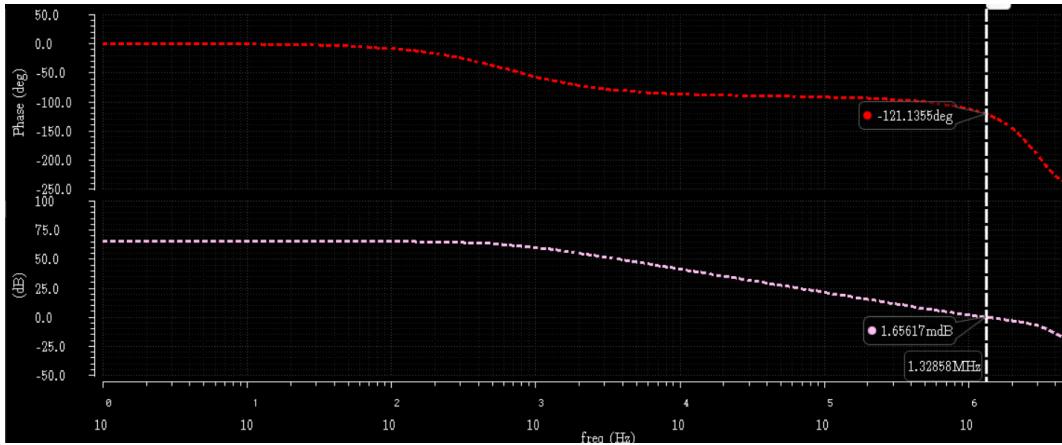
## Temperature

The dependency of the temperature is also exploited increasing it up to  $85^\circ$ , in order to see what happen to the important performance parameters.

Simulation in open loop is done again to obtain gain and phase, at the new temperature. Therefore, choose the same parameters as before and plot the AC Gain and Phase of  $V_{out}$  vs  $V_{inp}$ , in figure 76.

Notice that the DC open loop gain is now  $65.13 dB$ , while the first pole has  $f = 652 Hz$  corresponding at gain  $62 dB$ . The gain decrease a lot respect the case of  $@T = 27^\circ$ , probably because it is possible to have now a worst mismatch of the component and the compensation doesn't work correctly. In fact, the transconductances decrease due to the increase of temperature so also the gain decrease because is correlated to the transconductances.

At last the transition frequency is computed  $f_T = 1.33 MHz$  at the phase  $-121.1^\circ$ . In this situation is possible to understand that the phase margin,  $PM = (180 - 121.1)^\circ = 58.9^\circ$ , so the system is already in stability, figure 77. Also the PM strongly

Figure 76: AC Gain in Open Loop @ $T = 85^\circ$ Figure 77: Phase in Open Loop @ $T = 85^\circ$ 

decrease, because the resistance increase with the temperature,  $R(T \uparrow) \uparrow$ , so the compensation net change his behaviour and the  $PM \downarrow$  decrease a lot.

On the other hand, the GBW remain constant at  $T = 85^\circ$  because the DC gain decrease but the first pole is moving to higher frequency, thus the two parameters balance out the effects.

Finally on closed loop configuration is exploited the step response in order to see the effect of higher temperature. Apply the same parameters as before with rise time and fall time equal to  $700\text{ ns}$ , as it is done at  $T = 27^\circ$ , so it is possible to see in evidence that choosing a tran simulation with a stop time=  $60\text{ }\mu\text{s}$ , the system became unstable. Therefore, the increasing of the temperature, at the same conditions, cause the lose of stability.

## Harmonic Distortion

Finally, the linearity of the designed amplifier has been evaluated using the harmonics distortion parameter. It provides a measure of how much the amplifier is able to

reject the harmonics power and to amplify only the power at the fundamental. For this reason, the Harmonics Distortion value can be defined for each harmonic as the ratio between the power of n-esim harmonic and the power of the fundamental:

$$HD_n = \frac{A_n}{A_1} \quad (62)$$

Another figure of merit is the Total Harmonic Distortion, which take care of the contribution of all the harmonics component with respect to the fundamental one:

$$THD = \sqrt{\sum_{k=2}^n HD_k^2} \quad (63)$$

To make this simulation, a frequency domain analysis has to be performed. In order to understand how the linearity change with the amplitude of the input signal, it was used first  $400\text{ mV}$  and then  $500\text{ mV}$  peak to peak sinusoidal waveform at  $100\text{ kHz}$ . In both cases, an input and output port have been used; the first one was configured as shown in figure 78, while the second was simply a DC type port.

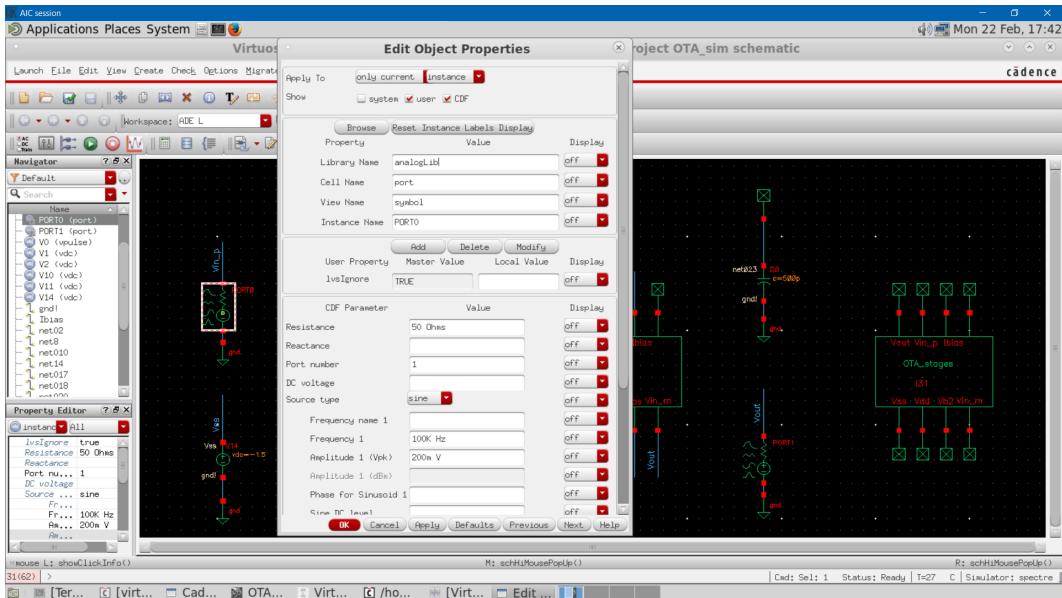


Figure 78: Input port configuration.

Closing the loop by connecting the negative input with the output node, the simulation environment is the one represented in figure 79.

- $400\text{ mV}_{pp}$  In order to perform a power spectrum simulation, it is used the *pss* simulation on ADE-L. The fundamental is set to  $100\text{ kHz}$  and the number of harmonics equal to 5. To plot the harmonics, it is used the tool *Result/Main*

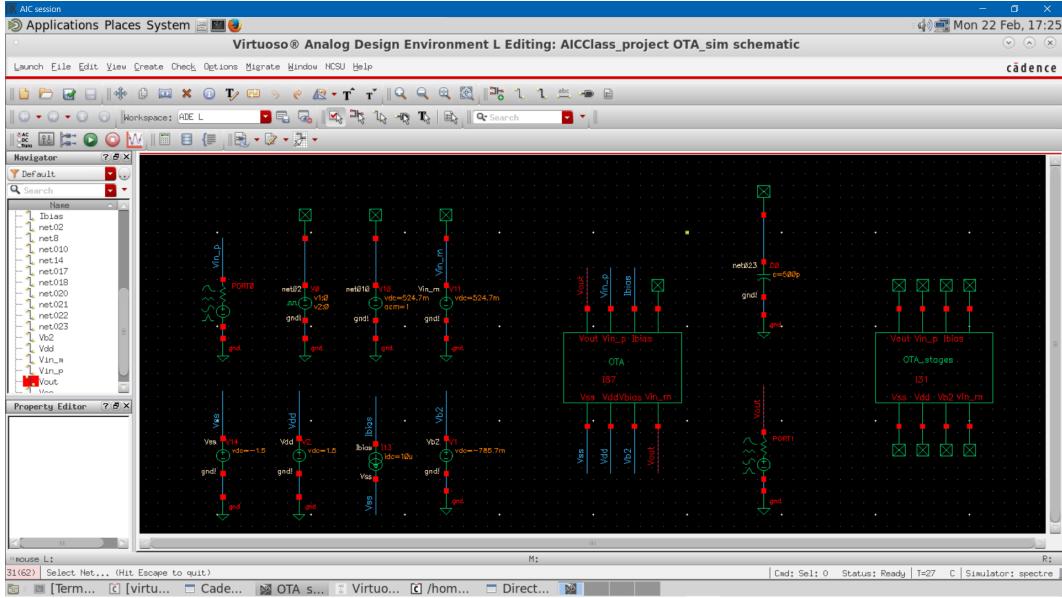
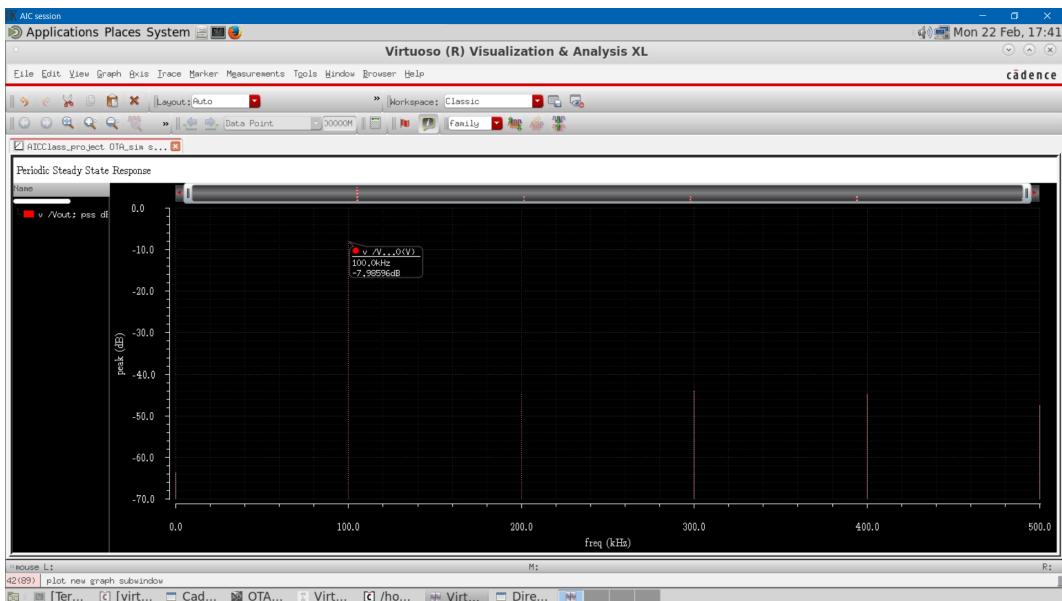


Figure 79: HD simulation schematic.

Figure 80: 400 mV<sub>pp</sub> harmonics.

form, deciding to plot the voltage peak in dB scale. The harmonics have a behavior as shown in figure 80.

The power spectrum of the fundamental, second and third harmonics are reported in table 9.

$P_1$	$P_2$	$P_3$
$-8 \text{ dB}$	$-44.8 \text{ dB}$	$-44 \text{ dB}$

Table 9: Power spectra with  $400 \text{ mV}_{pp}$ .

Using the Harmonics Distortion definition:

$$\begin{aligned} HD_2 &= P_2 - P_1 = -36.8 \text{ dB} \\ HD_3 &= P_3 - P_1 = -36 \text{ dB} \end{aligned} \quad (64)$$

These results are little worst than the paper ones but anyway they seems coherent and reasonable with this kind of circuit.

The Total Harmonic Distortion has been also evaluated using the available tool on Main Form window, finding:

$$THD = 2.79 \% \quad (65)$$

- $500 \text{ mV}_{pp}$  Exactly the same simulation as before has been performed, but this time using a bigger amplitude waveform at the input. In this case, it can be seen how the linearity of the circuit is worst, which is given by the fact that generally an amplifier have to find a trade-off between output power and linearity. The obtained value are reported in table 10.

$P_1$	$P_2$	$P_3$
$-6 \text{ dB}$	$-34.5 \text{ dB}$	$-35.3 \text{ dB}$

Table 10: Power spectra with  $500 \text{ mV}_{pp}$ .

The HD values are:

$$\begin{aligned} HD_2 &= P_2 - P_1 = -28.5 \text{ dB} \\ HD_3 &= P_3 - P_1 = -29.3 \text{ dB} \end{aligned} \quad (66)$$

Obviously, also the THD is worst, finding:

$$THD = 5.6 \% \quad (67)$$

This is a very huge value since a very good amplifier have to keep THD lowest than possible. For this reason, it is better to avoid to use this kind of amplifier with an amplitude of the input waveform bigger than the ones reported on these simulations.

## 6 Possible improvements

Until now voltage and current generator has been supposed to be ideal and external to the chip. In this section, a more realistic case is exploited and two possible implementations are proposed in order to integrate them within the circuit. The techniques to obtain voltage and current references are countless and it was decided to use two solutions which are considered suitable in terms of reliability and area consumption.

### 6.1 Voltage reference

The voltage reference can be designed starting from the ideal current generator with the configuration represented in figure 81.

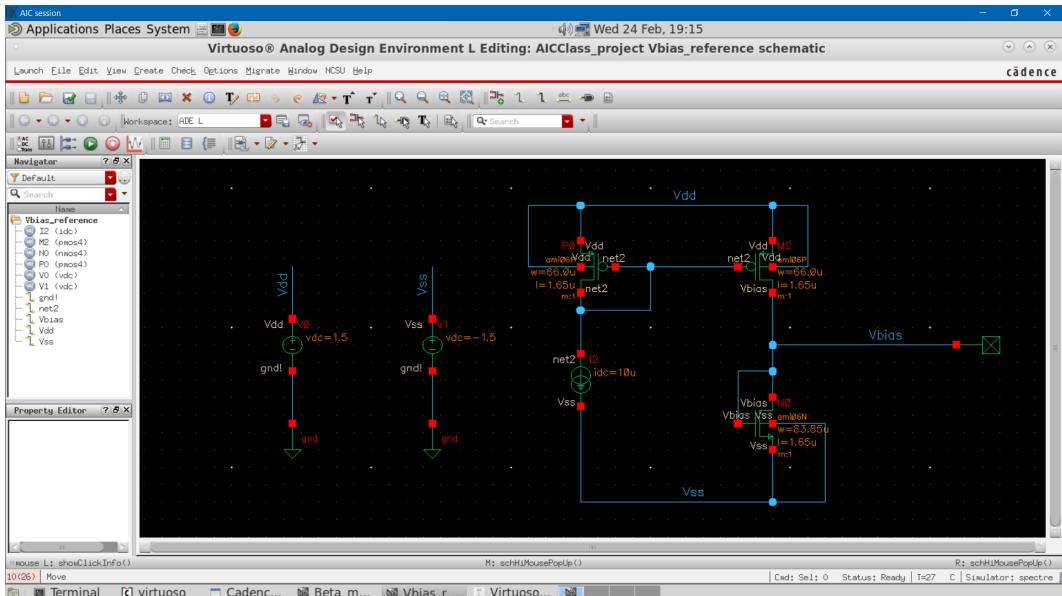


Figure 81: Vbias implementation.

Basically, the  $I_{bias}$  current is mirrored and delivered to  $M_0$ , which have to be designed in order to impose the desired  $V_{gs}$ , which is almost equal to the  $V_{bias}$  since it is on diode configuration. To this this analytically, let's consider that the drain current of  $M_0$  is basically equal to the bias current under the hypotheses of perfect mirroring. This current can be expressed as:

$$I_D = \frac{1}{2} \beta_n \left( \frac{W}{L} \right)_{M_0} (V_{GS} - V_{TH})^2 \quad (68)$$

Reversing the previous expression, the aspect ratio of  $M_0$  can be found.

However, the previous expression has a strong dependence on the transistor technology parameters. For this reason, a simulation approach has been used. In order to

design the M0 transistor aspect ratio, a DC sweep of W has been performed keeping constant the length at  $1.65 \mu m$  and looking at the  $V_{bias}$  value, founding the width for which the desired value is obtained. The simulated sweep is reported in figure 82.

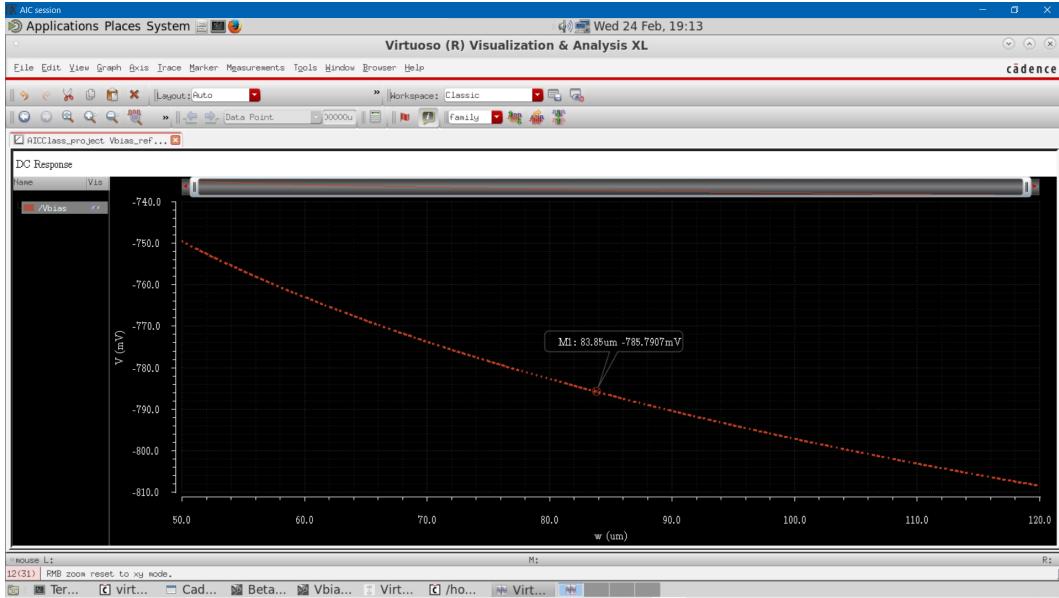


Figure 82:  $V_{bias}$  width sweep.

In this way:

$$\left(\frac{W}{L}\right)_{M0} = \frac{83.85}{1.65} \quad (69)$$

Just for confirmation, the previous result on aspect ratio has been used and a *DC voltage node* simulation has been performed, obtaining exactly the desired value.

## 6.2 Current reference - Beta multiplier

Also the bias current has been supposed to be external and ideal. If an internal reference current circuit is required, on literature a several number of solution are available. One of the most used is the beta multiplier circuit, which allows to provides a desired reference current using the mirroring principle and making the opportune transistor dimensions. In order to provides a very stable reference current, in this section it is presented its cascaded version. This solution, of course, is not suitable with very low voltage circuits since all transistors have to stay in saturation. The cascaded beta multiplier circuit implemented on Virtuoso has been reported in figure 83.

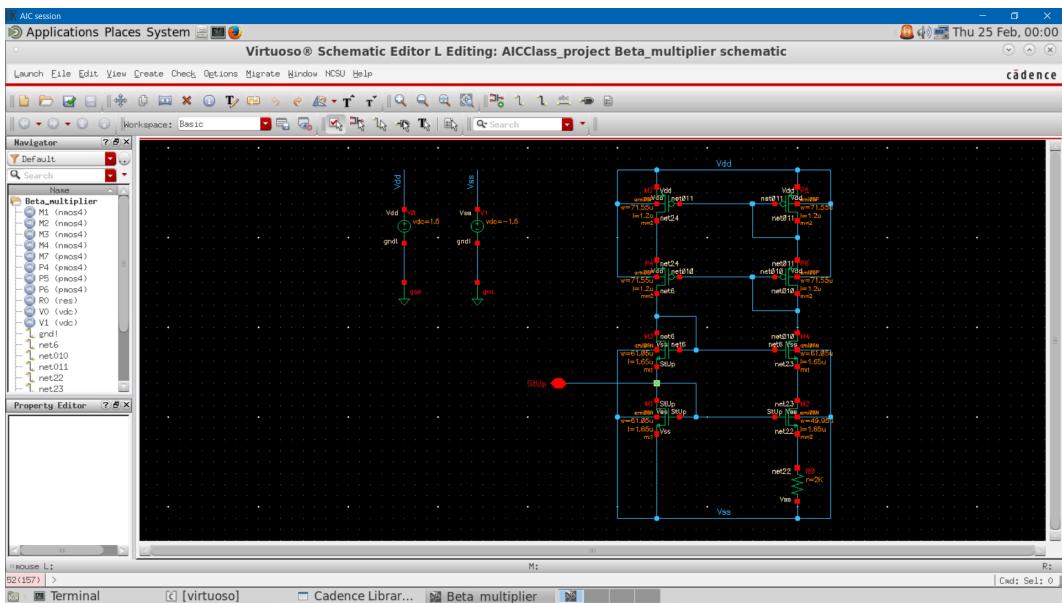


Figure 83: Beta multiplier.

The beta multiplier has been designed in order to provide a reference current of  $10 \mu A$ . The main design formula for this kind of circuit is:

$$I_{ref} = \frac{2}{R^2 \beta_1} \left( 1 - \frac{1}{\sqrt{k}} \right) \quad (70)$$

Where  $k$  has been set equal to 2 and the resistance  $R$  equal to  $2 k\Omega$ . Inverting this equation, the aspect ratio of  $M_1$  can be found:

$$\left( \frac{W}{L} \right)_{M1} = \frac{2}{R^2 k_n I_{ref}} \left( 1 - \frac{1}{\sqrt{k}} \right) = 37 \mu m \quad (71)$$

Since  $\beta_2 = k\beta_1$ , the aspect ratio of M2 is:

$$\left(\frac{W}{L}\right)_{M2} = k \left(\frac{W}{L}\right)_{M1} = 74 \mu m \quad (72)$$

Now, regarding the others NMOS,  $M_3$  and  $M_4$  are designed in order to have the same overdrive voltage of  $M_1$ .

$$\left(\frac{W}{L}\right)_{Mn} = 37 \mu m \quad (73)$$

At the same way, to achieve a 1:1 mirroring, the PMOS are designed with the same turn ratio. Under the assumption that all the overdrives are almost equal, it is found that for the PMOS:

$$\left(\frac{W}{L}\right)_{Mp} = \frac{k_n}{k_p} \left(\frac{W}{L}\right)_{Mn} \mu m \quad (74)$$

It is important to underline that in all these computations the body effect has been neglected.

Now, the transistor length has been fixed to:

$$\begin{aligned} L_n &= 1.65 \mu m \\ L_p &= 1.2 \mu m \end{aligned} \quad (75)$$

Finding these transistor widths:

$$\begin{aligned} W_2 &= 122 \mu m \\ W_n &= 61 \mu m \\ W_p &= 143 \mu m \end{aligned} \quad (76)$$

At this point, a DC sweep of  $W_2$  has been performed in order to find the exact value for which the reference current is  $10 \mu A$ , finding  $W_2 = 100 \mu m$ .

Finally, a DC sweep of supply voltage has been performed (figure 84), looking at the behaviour of the reference voltage and observing how its value is almost constant.

One fundamental constrain is that this kind of circuit must be used with a start-up circuit, which ensure the working on the desired equilibrium point.

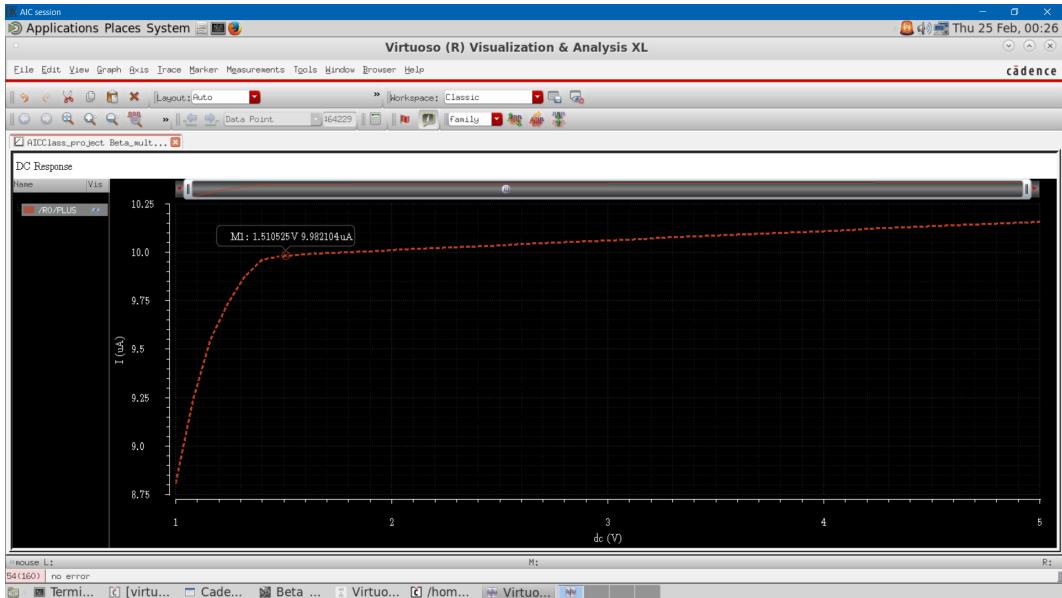


Figure 84:  $I_{ref}$  vs  $V_{DD}$ .

## 7 Conclusions

The topic points of the implemented projects are the high gain-bandwidth and phase margin of the OTA and the capability to drive a large capacitive load ( $500\text{ pF}$ ) thanks to the innovative proposed compensation strategy, so all the project choices was done in order to exploit as much as possible this characteristic.

There are many differences between the project proposed on the paper with respect to the one implemented on this report and these have been reported in table 11.

The main differences are due to the different technology used, because in the projected implemented is used the only one available that it is bigger and older than the one of the paper, which implicate many differences in the implementation of the layout. One of these is the necessity of redefine the compensation net and also the aspect ratios in order to maintain the same circuit characteristic.

Obviously, both projects have the same power supply and loading capacitance because these are some of the topic aspects that it is desired to maintain unchanged, in order to give fidelity to the comparisons.

The area in the new structure became lower even though the bigger technology used, due to the lower compensation capacitance designed for the project implemented, necessary to have the correct compensation behaviour. On the other hand, the area occupied by the compensation net for the paper implementation is about 80%, so obviously the reduction of capacitance means strongly reduction of area.

The layout obtained is simulated in order to obtain some performance parameters. For example, the obtained input offset voltage is very small, also lower respect the paper one.

The DC gain obtained is a little less respect the one obtained in the paper,  $113\text{ dB}$ ,

PARAMETER	PAPER	LAYOUT
Technology	$0.35 \mu m$ CMOS	$0.6 \mu m$ CMOS
Area	$0.075 mm^2$	$0.057 mm^2$
Power supply	$1.5 V$	$1.5 V$
Loading Capacitance	$500 pF$	$500 pF$
Input Offset Voltage	$2.3 mV$	$275 \mu V$
DC Gain	$113 dB$	$107 dB$
Gain-bandwidth Product	$1.4 MHz$	$1.71 MHz$
Phase Margin	$75^\circ$	$86.6^\circ$
CMRR @ DC	$78 dB$	$48.4 dB$
Positive(Negative) Slew Rate	$2.2(-1.8) V/\mu s$	$0.58(-0.61) V/\mu s$
Positive(Negative) Settling time at 1%	$810(740) ns$	$942.3(972.3) ns$
HD2/HD3 @ $100kHz, 400mVpp$	$-54.25 / -60.36 dB$	$-36.8 / -36 dB$
HD2/HD3 @ $100kHz, 500mVpp$	$-48.20 / -56.71 dB$	$-28.5 / -29.3 dB$

Table 11: COMPARISON OTA PERFORMANCE PARAMETERS.

maybe due to the fact that specific technology for the implementation in exam impose different transistor parameters.

However, the **Phase Margin** obtained is greater respect the one computed in the paper, that it is  $PM_{paper} = 75^\circ$ , so it is optimal because have a strongly stability condition.

One of the main topic aspect is also the **GBW**, so it is improved much as possible to obtain higher value respect the paper implementation.

On the other side, the **CMRR** of the designed OTA is reduced than the paper circuit, resulting on a worst capability to reject the common mode input voltage.

The positive and negative **settling times** obtained result higher than the paper ones, resulting on slowing behaviour to reach the 1% of final value.

Also for the **Slew Rate** (both positive and negative) the performance became worse, in fact now there is a very deep reduction of about 4 times compared to the paper project.

Finally, the **harmonic distortions** are computed like the difference in *dB* between the second and third harmonic and the fundamental one. The results are worst than the paper ones but anyway they seems coherent and reasonable for the circuit for both the considered amplitude of the input signal.

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