

Three-Stage CMOS OTA for Large Capacitive Loads With Efficient Frequency Compensation Scheme

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Introduction

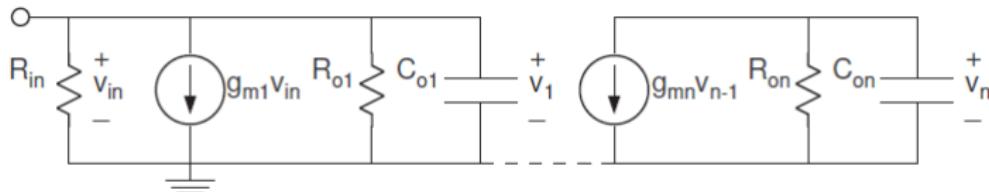
This project is based on the design and simulation of a real integrated analog circuit starting from the homonym paper published by Grasso, Palumbo and Pennisi in 2006. The work is divided in the following parts:

- Underlying theory;
- Paper and Pencil analysis and adaptation at the available technology;
- Schematic implementation with CMOS libraries and simulations;
- Layout realization and simulations;
- Conclusions and comparison with paper results.

Multistage OTAs

Theory

- One of the key parameters for a feedback amplifier is its **DC open loop gain**. Presently, amplifiers exhibiting DC gains over 100 dB can profitably be implemented with a cascade of three simple stages.
- Generally, the first stage, in addition to providing a gain, must also provide a high common mode rejection.
- The intermediate stages must provide most of the gain in voltage and sometimes convert signal from differential to single ended.
- The main task of the output stage is to supply the current required by the load efficiently.



Stability 1/2

Theory

- In design of a multistage OTAs with multiple high impedance node, special care must be taken to ensure **stability**.
- To ensure stability in a feedback amplifier, let's look at the loop gain:

$$T(j\omega) = |\beta(j\omega)a(j\omega)|e^{j\phi(\omega)} \quad (1)$$

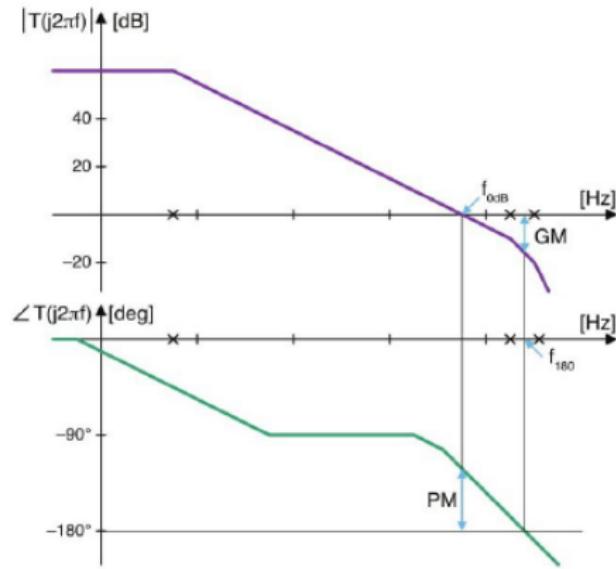
At frequency at which the phase angle $\phi(\omega)$ becomes 180° , the loop gain will be a negative real number, so at this frequency the feedback will become positive.

- On the other hand, at ω_{180} the magnitude of the loop gain is equal to unity, it follows that closed loop gain becomes infinite. The ω_{180} is defined oscillation frequency and **Barkhausen oscillation condition** occurs.

Stability 2/2

Theory

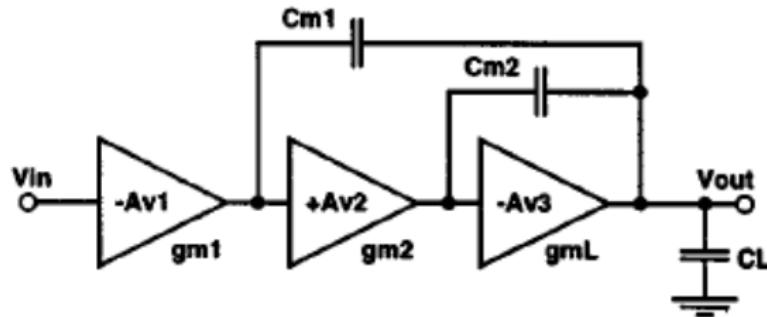
- The same concept can be expressed graphically by Bode plots and **phase margin** concept.
- $PM = 180 + \angle T(j\omega_T)$
- Amplifier defined stable if $PM > 0$. Typically $PM > 45^\circ$ required.
- By moving the second pole to the right the phase margin increases.



Classic Nested Miller Compensation

Theory

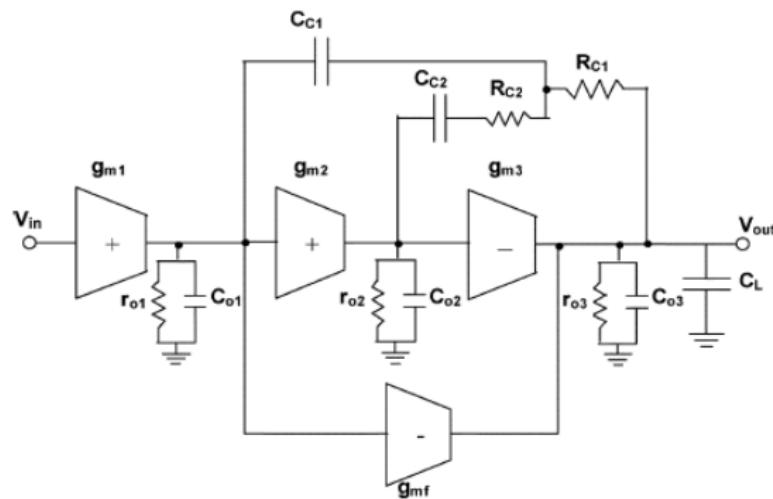
- Design of multistage amplifiers is challenging since the increased number of **high impedance nodes** (i.e. low-frequency poles) may result in instability.
- With three stage OTAs, one of the most employed possibility is to use the Nested Miller topology.
- However, this solution results in bandwidth reduction and high power consumption, especially in CMOS technology.



The adopted compensation technique

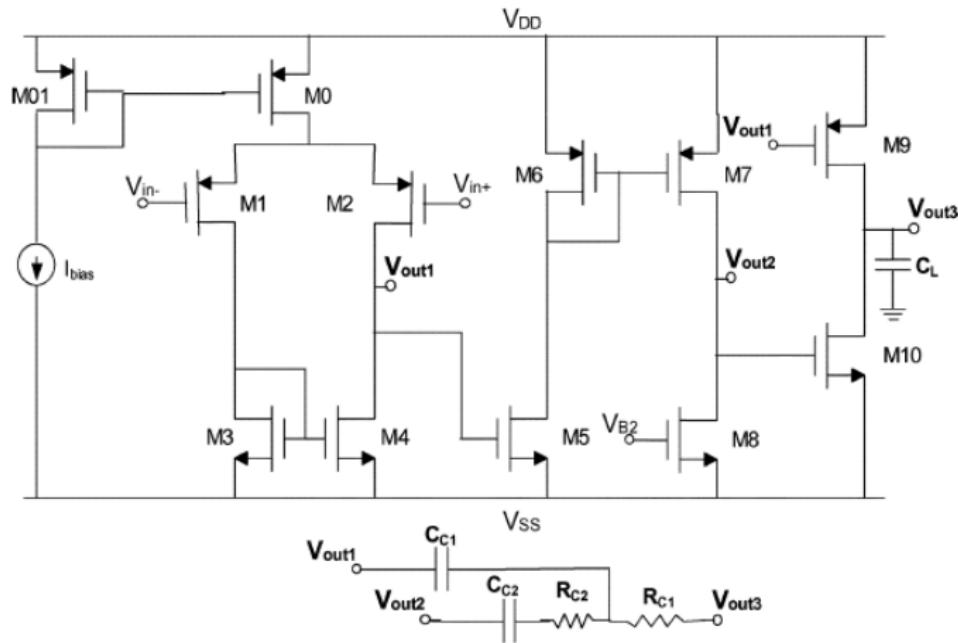
Theory

- In this work, a simple compensation strategy is exploited to design a three-stage OTA suitable for driving **high capacitive loads**.
- Basically, by choosing smartly the compensation net values, a double pole-zero compensation is achieved and the circuit behaves a simple **first-order system**.



The proposed three-stage OTA

Paper analysis



$$A_v(s) = A_0 \frac{a_2 s^2 + a_1 s + 1}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(b_2 s^2 + b_1 s + 1\right) \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (2)$$

OTA transfer function 1/2

Paper analysis

- A_0 is the DC gain and it is approximately equal to:

$$A_0 = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3} \quad (3)$$

- Regarding the numerator, the complete expression is given considering:

$$a_1 = R_{C1}C_{C1} + \left(R_{C2} - \frac{1}{g_{m3}} + \frac{g_{mf}}{g_{m2}g_{m3}} + R_{C1} \right) C_{C2} \quad (4)$$

$$a_2 = \frac{(1 + g_{m2}R_{C2})g_{m3}R_{C1} - 1 + g_{mf}R_{C1}}{g_{m2}g_{m3}} C_{C1}C_{C2} \quad (5)$$

These two terms provides two zeros on the compensated transfer function.

- The two zeros can be made both negative, ensuring the absence of RHP zeros.

OTA transfer function 2/2

Paper analysis

- The dominant pole is given by the Miller effect on C_{C1} and so it is around the frequency:

$$\omega_{p1} \approx \frac{1}{r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{C1}} \quad (6)$$

- Also, at the denominator it can be seen that there are two additional poles, which depends on C_{c2} and C_L and can be found considering:

$$b_1 = \left(R_{C2} + \frac{1}{g_{m2}} - \frac{1}{g_{m3}} + \frac{g_{mf}}{g_{m2}g_{m3}} \right) C_{C2} \quad (7)$$

$$b_2 = \frac{1 - g_{m2}R_{C1}}{g_{m2}g_{m3}} C_{C2} C_L \quad (8)$$

- In addition, there is a high-frequency pole given by the contribution of the C_{o2} , at the frequency:

$$\omega_{HF} = \frac{R_{C1}}{1 - g_{m2}R_{C1}} C_{o2} \quad (9)$$

Compensator design formulas

Paper analysis

- Properly choosing component values, the zeros can be adjusted to exactly cancel out the two higher poles by a double pole-zero superimposition.

$$R_{C1} = \frac{1}{g_{m3}} \quad (10)$$

$$R_{C2} = \frac{C_L}{g_{m3} C_{C2}} - \frac{g_{mf}}{g_{m3} g_{m2}} \quad (11)$$

$$C_{C1} = \frac{g_{m3} - g_{m2}}{g_{m2}} C_{C2} \quad (12)$$

- A degree of freedom allows to maximize one design parameter (**GBW** in our case, see later).
- Additional constraints to ensure practicability and performance will be verified.
- Unlike conventional compensation strategies, C_{C1} is not proportional to C_L but to C_{C2} and for this reason this is well suited for **high capacitive load**.

OTA Main performance parameters

Paper analysis

PARAMETER	VALUE
Technology	$0.35 \mu m$ CMOS
Area	$0.075 mm^2$
Power supply	$1.5 V$
Loading Capacitance	$500 pF$
Input Offset Voltage	$2.3 mV$
DC Gain	$113 dB$
Gain-bandwidth Product	$1.4 MHz$
Phase Margin	75°
CMRR @ DC	$78 dB$
Positive(Negative) Slew Rate	$2.2(-1.8) V/\mu s$
Positive(Negative) Settling time at 1%	$810(740) ns$
HD2/HD3 @ $100kHz, 400mVpp$	$-54.25 / -60.36 dB$
HD2/HD3 @ $100kHz, 500mVpp$	$-48.20 / -56.71 dB$

Table: OTA MAIN PERFORMANCE PARAMETER

Effect of mismatch 1/2

Paper analysis

- Imperfect double pole-zero cancellation can be caused by **process tolerances**.

$$A(s) = \frac{\omega_{GBW}}{s} \cdot \frac{1 + b_1 s + b_2 s^2}{1 + a_1 s + a_2 s^2} \quad (13)$$

- The effect of mismatch on coefficients b_i through parameters $\delta_{1,2}$ as:

$$b_1 = a_1(1 + \delta_1) = \frac{2\xi}{\omega_n}(1 + \delta_1) \quad (14)$$

$$b_2 = a_2(1 + \delta_2) = \frac{1}{\omega_n^2}(1 + \delta_2) \quad (15)$$

- The damping factor ξ is always greater than 1, so this ensures that the poles are real and are located approximately at the frequency $1/a_1 = \omega_n/2\xi$ and $a_1/a_2 = 2\xi\omega_n$.

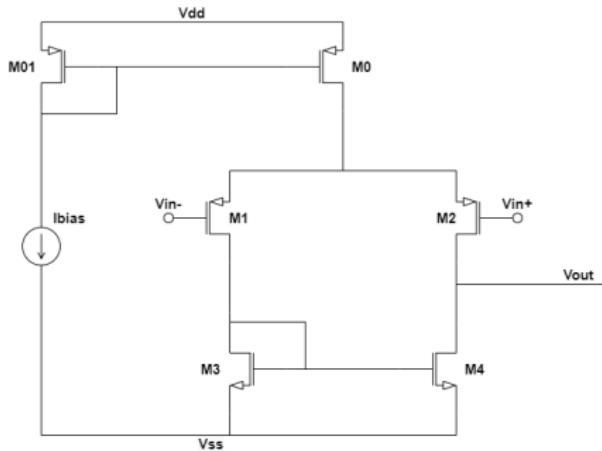
Effect of mismatch 2/2

Paper analysis

- The possible mismatch of parameters a_1 and b_1 could worsen the settling time and modify the actual unity-gain frequency.
- Pessimistic case in which the mismatches are all uncorrelated and assuming that the values of the circuit parameters are uniformly distributed within $\pm 20\%$ of their nominal value.
- δ_1 is almost insensitive to the parameter mismatches, due to the fact that its variation is very limited.
- δ_2 is more affected by mismatches since its value varies a lot. Responsible for the imperfect cancellation of the highest pole-zero doublet located well beyond the gain-bandwidth product.

First Stage

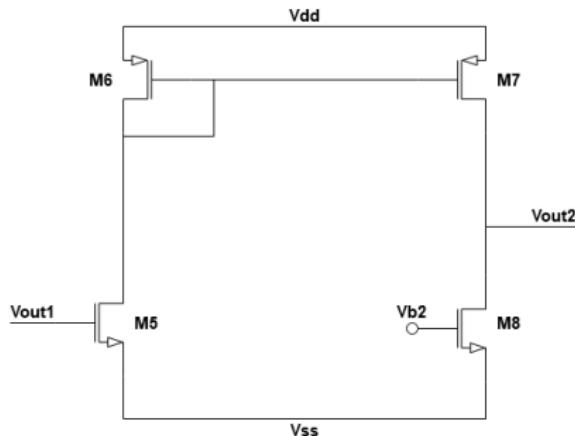
Single Stage Analysis



- It is composed by a PMOS differential pair polarized by current mirror M_0-M_{01} and having the mirror M_3-M_4 as load in order to obtain a large gain.
- Differential input and single output.
- To work properly, M_0 dimensions are double than M_{01} while M_3 and M_4 are equal. M_1 and M_2 must be identical to ensure symmetry.
- The gain is non-inverting as required on the compensation scheme: $A_1 = g_{m1,2}(r_{o4}/r_{o2})$

Second Stage

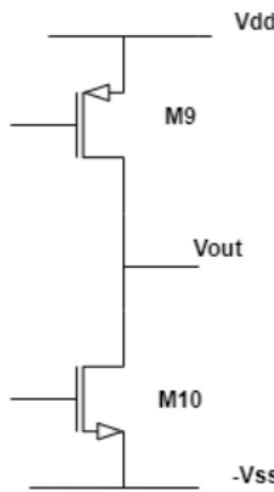
Single Stage Analysis



- Simple common source is not suitable with the proposed compensation technique since has inverting gain.
- Instead, analyzing this circuit, comes out that $A_2 = g_m5(r_{o7} // r_{o8})$.
- Same gain of the common source but with a plus sign.

Third Stage

Single Stage Analysis



- Third stage is a simple common source with active load.
- Easily, its gain is inverting and equal to $A_3 = g_{m10}(r_{o9} // r_{o10})$.
- Since M_9 is driven by V_{out1} , the stage behaves as AB output stage able to drive the capacitor C_L .
- M_9 also implements the **feedforward** transconductor required for the adopted compensation.

Poles evaluation

Non compensated circuit

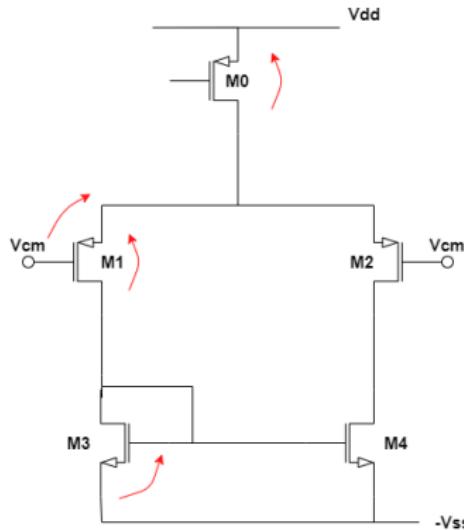
- Looking again at the single stages, the non-compensated circuit exhibits three poles:

	1st stage	2nd stage	3rd stage
ω_p	$\frac{1}{R_{o1}C_{o1}}$	$\frac{1}{R_{o2}C_{o2}}$	$\frac{1}{R_{o3}C_{o3}}$

- $C_{o1} = C_{gs5} + C_{gd5} \left[1 + g_{m5} \left(\frac{1}{g_{m6}} // r_{o5} \right) \right]$
- $C_{o2} = C_{gs10} + C_{gd10} (1 + A_3)$
- $C_{o3} \approx C_L$
- Using Miller RHP zeros are presents and located at high frequency and they can sometimes be cause of instability. In order to solve this issue, resistances on compensator network are used.

Input range

Analytic evaluation



Using KVL node equations and imposing transistors saturation:

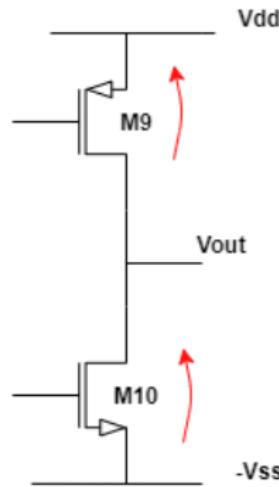
$$\begin{cases} V_{CM} + V_{SG,M1} - V_{GS,M3} - (-V_{SS}) \geq V_{OD,M1} \\ V_{DD} - (V_{SG,M1} - V_{CM}) \geq V_{OD,M0} \end{cases}$$

After some algebraic steps, the lower and upper limits of CMR are:

$$\begin{cases} V_{CM} \geq V_{THN} - |V_{THP}| + \sqrt{\frac{I_{BIAS}}{2 \cdot \beta_N \cdot \frac{W}{L} |_3}} - V_{SS} \\ V_{CM} \leq V_{DD} - \sqrt{\frac{2 \cdot I_{BIAS}}{\beta_P \cdot \frac{W}{L} |_1}} - |V_{THP}| \end{cases}$$

Output range

Analytic evaluation



Upper and lower limits are found to ensure M_9 and M_{10} saturation:

$$\begin{cases} V_{out,max} \leq V_{DD} - V_{OD,M9} \\ V_{out,min} \geq -V_{SS} + V_{OD,M10} \end{cases}$$

Adaptation at available technology.

- Transistors have been resized from $0.35\ \mu m$ to $0.6\ \mu m$ CMOS technology.
- $2L_{min}$ has been considered as lower limit.

Transistor	Aspect ratio
M0	$2 \times (40/1)$
M01	$40/1$
M1, M2	$4 \times (40/1)$
M3, M4	$40/0.7$
M5	$2 \times (40/0.7)$
M6, M7	$50/0.7$
M8	$40/1$
M9	$4 \times (40/0.7)$
M10	$8 \times (40/0.7)$

Table: Paper aspect ratios.

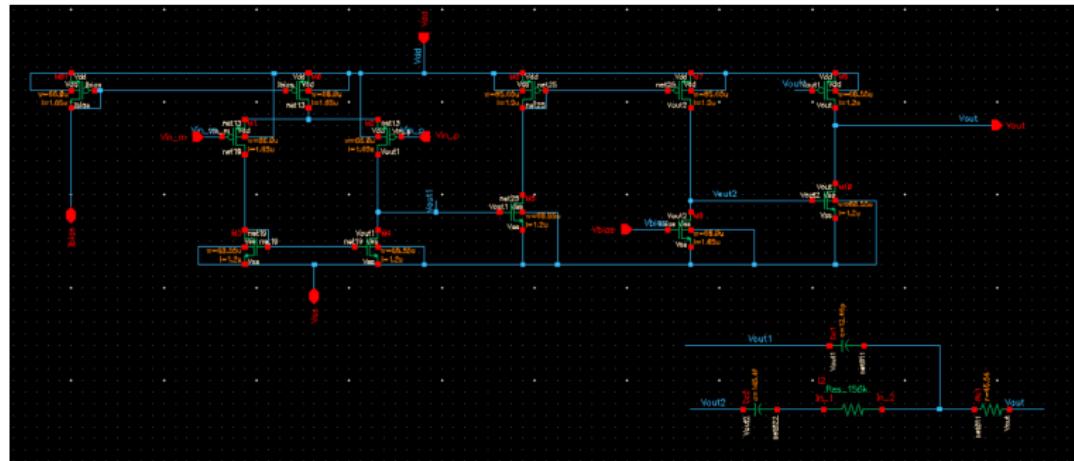
Transistor	Aspect ratio
M0	$2 \times (66/1.65)$
M01	$66/1.65$
M1, M2	$4 \times (66/1.65)$
M3, M4	$68.55/1.2$
M5	$2 \times (68.55/1.2)$
M6, M7	$85.65/1.2$
M8	$66/1.65$
M9	$4 \times (68.55/1.2)$
M10	$8 \times (68.55/1.2)$

Table: Project aspect ratios.

Schematic

Three stage OTA

- The design has been divided in two steps: the first regarding only the schematic and using the already available CMOS library while the second one with the complete layout realization.
- The projected aspect ratios have been used. Virtuoso environment allows to use the **multiplier**, which automatically takes "n" times the defined width of the transistors.



Schematic

- Since this is not specified on paper, it is supposed to have externally voltage and current biasing with ideal sources on the simulation cellview using additional pins.
- By performing a DC simulation and looking at single stages, the **transconductance values** have been found.

g_{m1}	$117.4 \mu A/V$
g_{m2}	$251.7 \mu A/V$
g_{m3}	$21.8 mA/V$
g_{mf}	$7.8 mA/V$

Table: Simulated transconductances.

- Using them, the compensation network has been designed thanks to the design formulas already reported in the theory section.

Compensation Network

Schematic

- With the Matlab auxiliary and using the simulated transconductances, the component values of **compensation network** have been found.

- Gain-Bandwidth Product** has been fixed: $\omega_{GBW} = \frac{g_{m1}}{C_{c1}} = 1.5 \text{ MHz}$

- Damping factor: $\xi = \frac{1}{2} \left(\frac{C_L}{C_{c2}} + \frac{g_{m3}}{g_{m2}} - 1 \right) \left[\frac{C_L}{C_{c2}} \left(\frac{g_{m3}}{g_{m2}} - 1 \right) \right]^{-\frac{1}{2}} = 3.2467$
- To obtain phase margin of at least 90 degree: $C_{c2} \gg \frac{g_{m1}g_{m2}}{(g_{m3}-g_{m2})^2} C_{o2}$, where $C_{o2} = C_{gs10} // C_{ds8}$
Let's verify: $C_{c2} - \frac{g_{m1}g_{m2}}{(g_{m3}-g_{m2})^2} C_{o2} = 1.97 \times 10^3$

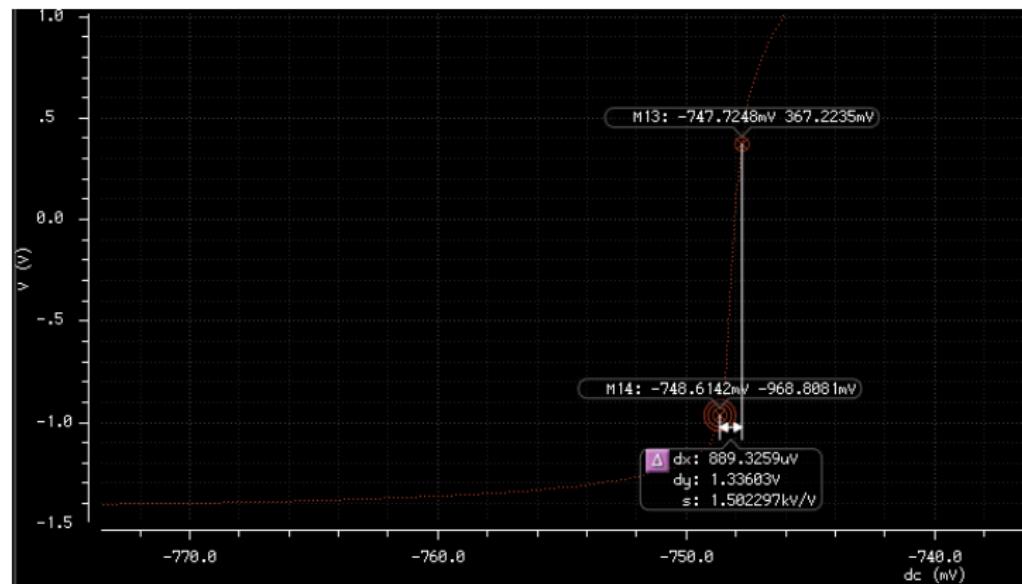
C_{c1}	12.46 pF
C_{c2}	145.5 fF
R_{c1}	45.8Ω
R_{c2}	$156.2 \text{ k}\Omega$

Table: Compensation network design.

DC Sweep 1/2

Schematic Simulation

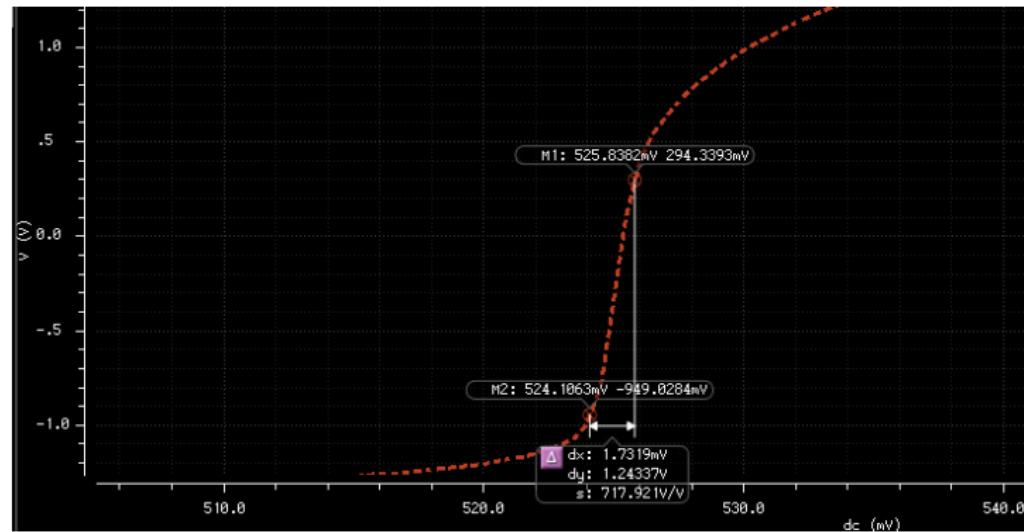
- Let's work in open loop, imposing $V_{inm} = V_{inp}$.
- Select at first V_{b2} generator to sweep between $-1.6V$ and $+1.6V$, linear sweep with step size of $0.5 mV$.
- The optimum **bias point** found is $V_{b2} = -748 mV$.



DC Sweep 2/2

Schematic Simulations

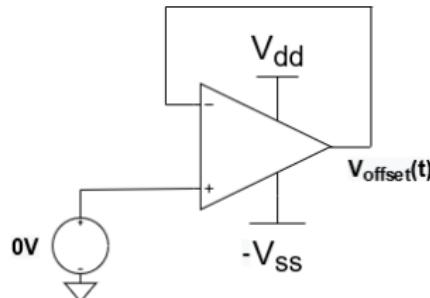
- Again, the same simulation as before has been performed, this time selecting V_{inp} generator to sweep.
- The optimum bias point found for $V_{inp} = 525 \text{ mV}$.



Input Offset Voltage

Schematic Simulations

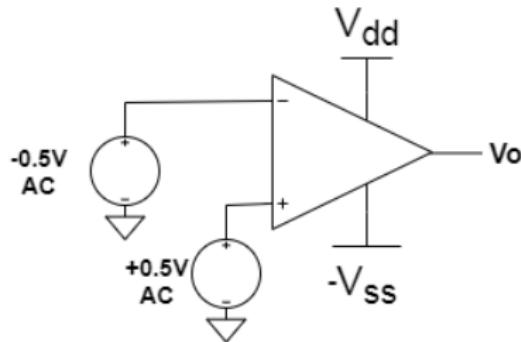
- To perform this simulation, a closed loop configuration has been set using $V_{out} = V_{inm}$.
- V_{inp} has been set to a DC Voltage= 0 and also AC Magnitude= 0.
- Looking at the output value, it is different from zero. The input offset voltage is equal to $-277 \mu V$, that it is generally a very small value for an OTA offset.



AC Open Loop 1/2

Schematic simulations

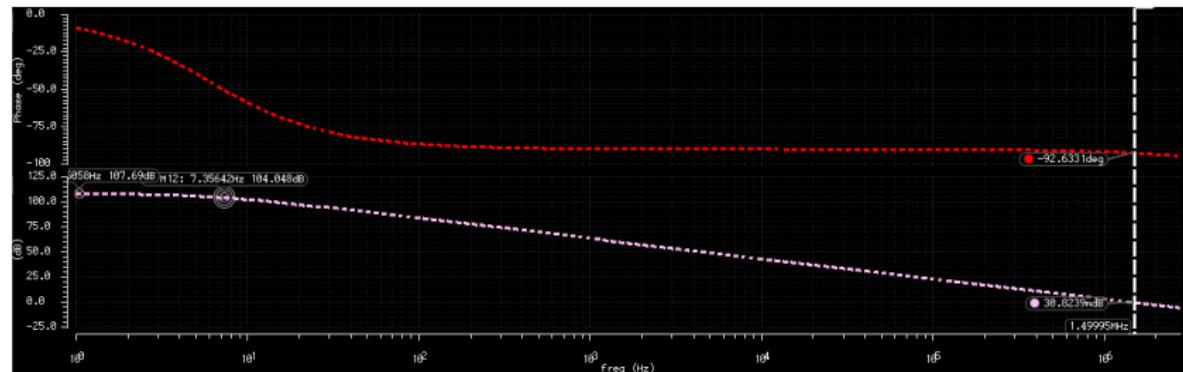
- Simulation in open loop is done to see at gain and phase Bode plots.
- Therefore, Choose Analysis/AC, sweep variable is the frequency, with a range from 1 Hz to 5 MHz , sweep type Logarithmic within 20 points per decade.
- Notice that the DC open loop gain is 107.7 dB , while the first pole has $f = 7.3\text{ Hz}$ corresponding at gain 104.7 dB .



AC Open Loop 2/2

Schematic Simulations

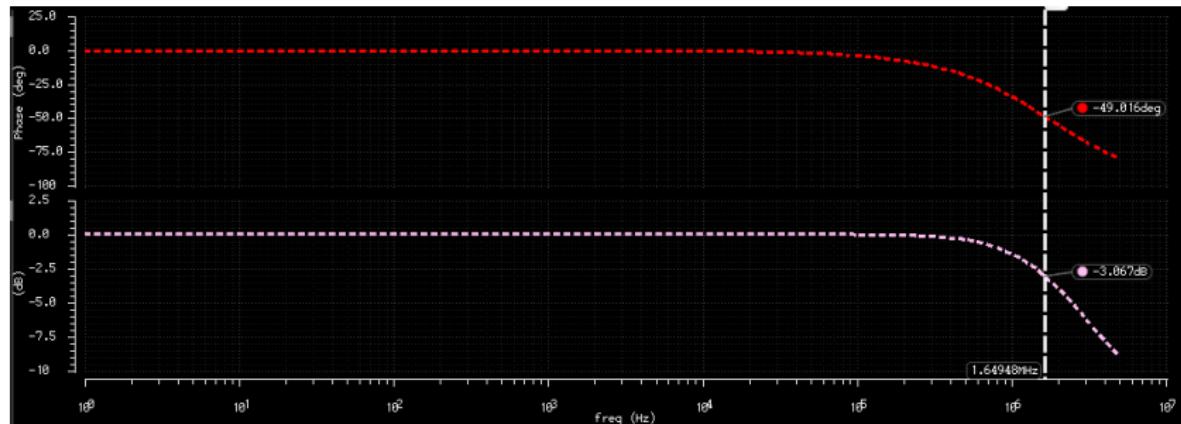
- At the transition frequency, when the gain equal to 0 dB, $f_T = 1.499 \text{ MHz}$ at the phase -92.6° .
- In this position the phase margin is evaluated, finding $PM = (180 - 92.6)^\circ = 87.4^\circ$.
- This is a very large value, so the system is in deep stability.



Closed Loop

Schematic Simulations

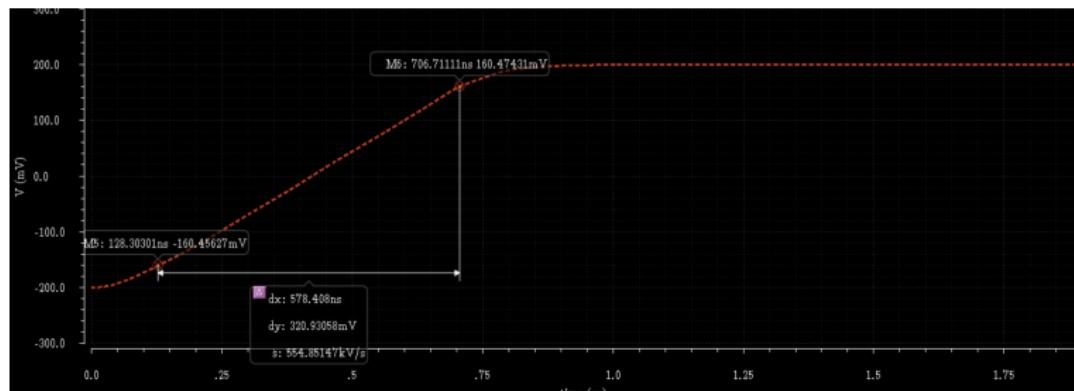
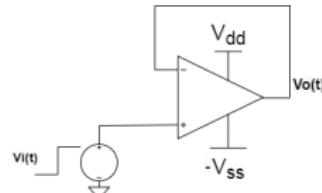
- Gain-BandWidth product is defined in closed loop configuration and applying AC signal at input.
- Looking at -3 dB , $GBW = 1.65\text{ MHz}$ at phase= -49°



Step response 1/4

Schematic Simulations

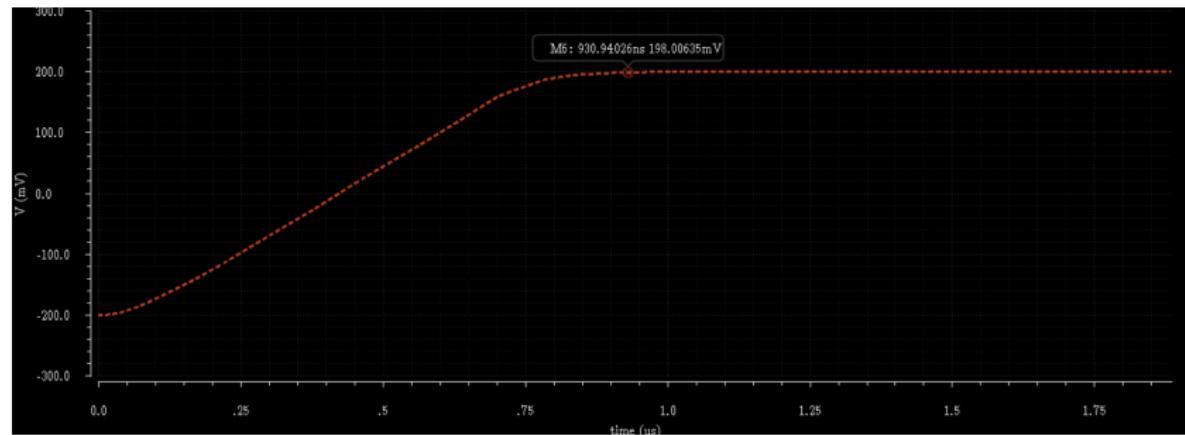
- An input step is applied on V_{inp} , with an amplitude between -200 mV and 200 mV , rise time and fall time equal to 700 ns , pulse width = $2.5 \mu\text{s}$ and period = $6 \mu\text{s}$.
- Choose a .tran simulation with a stop time of $100 \mu\text{s}$.
- The rise time between 10% and 90% is $t_r = 578.4 \text{ ns}$.



Step Response 2/4

Schematic Simulations

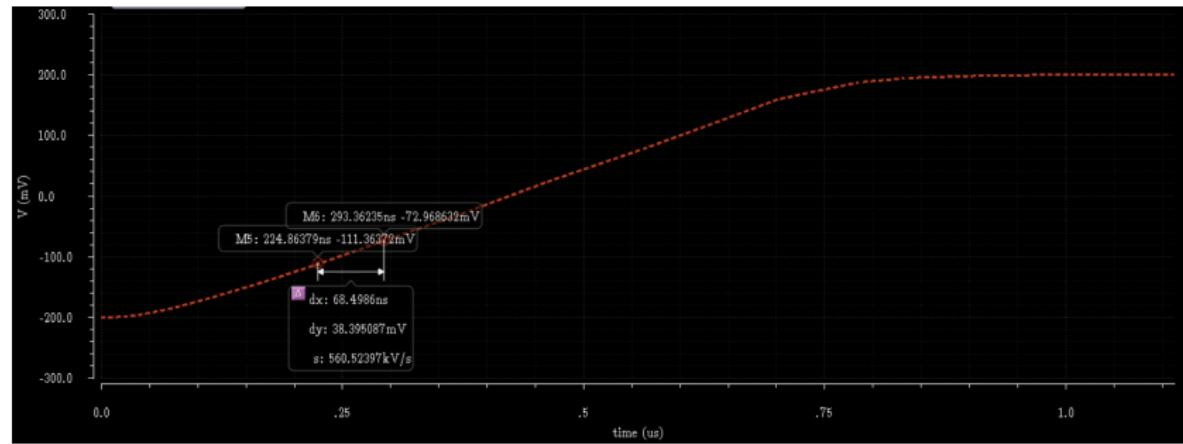
- The settling time is the time required for the response curve to reach and stay within a range of 1% of the final value (i.e. 198mV).
- $\text{settling_time}^+ = 931.1 \text{ ns}$.



Step Response 3/4

Schematic Simulations

- The Slew rate is defined as the rate of change of the output voltage per unit time.
- It defines how fast is the circuit to response at the input.
- Looking at the maximum slope points, it is found $SR^+ = 0.56 \text{ V}/\mu\text{s}$



Step Response 4/4

Schematic Simulations

- All the previous parameters have been also computed exactly in the same way for the falling edges.
- $t_f = 569.2 \text{ ns}$
- $\text{settling_time}^- = 905.54 \text{ ns}$
- $SR^- = 0.57 \text{ V}/\mu\text{s}$
- The result are generally worst than rising edge but anyway comparable.

Common Mode Rejection Range 1/2

Schematic Simulations

- The CMRR defines the ability of a differential amplifier to reject the common mode voltage at the input.
- To find it, the common mode gain has to be found.
- Let's put an AC signal both on positive and negative inputs and look at the DC gain value.

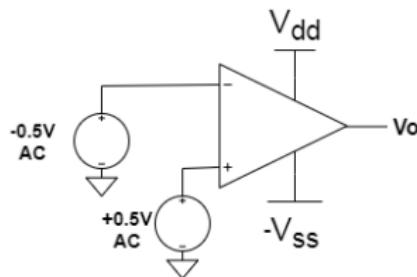


Figure: Scheme to determine A_d

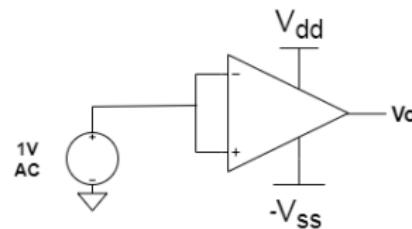
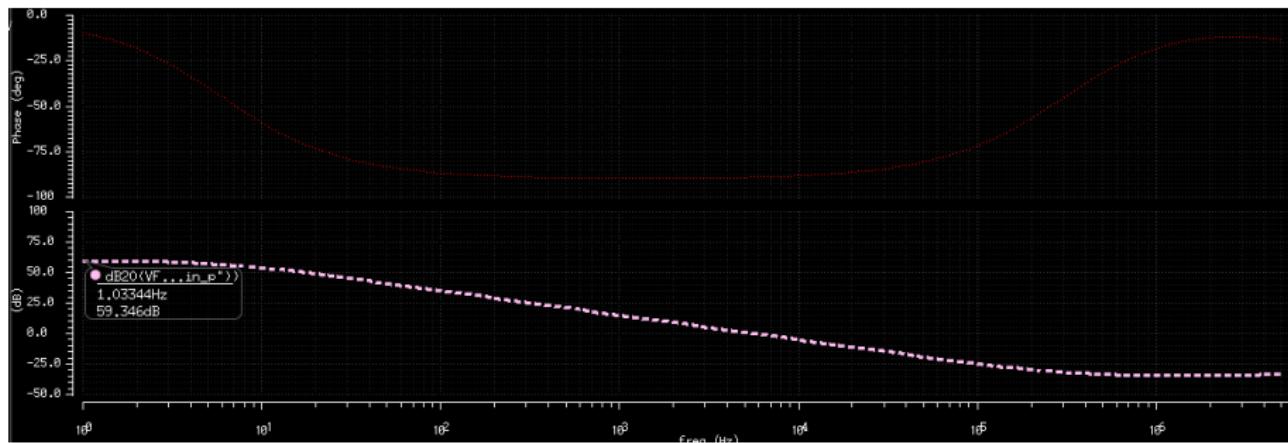


Figure: Scheme to determine A_c

Common Mode Rejection Range 2/2

Schematic Simulations

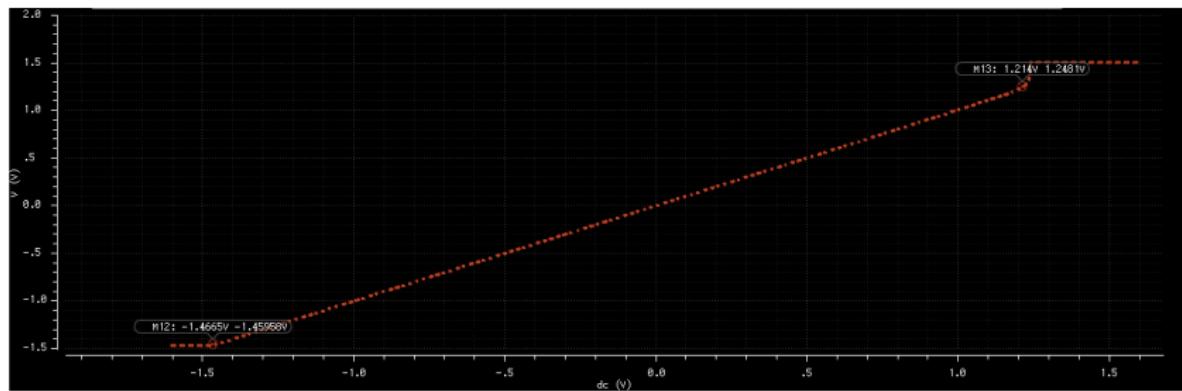
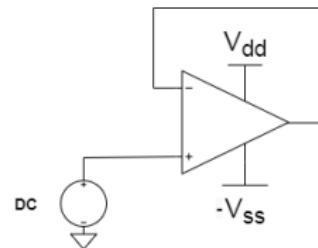
- $A_{d,dB} = 107.7 \text{ dB}$
- $A_{c,dB} = 59.35 \text{ dB}$
- $CMRR = A_{d,dB} - A_{c,dB} = 48.35 \text{ dB}$



Common Mode Range

Schematic Simulations

- The CMR is the range of input voltage values for which it is guaranteed that all transistors remains in saturation.
- Let's make an input DC sweep in closed loop configuration.
- $CMR = CMR^+ - CMR^- = 1.214V - (-1.467)V = 2.68V$



Power Supply Rejection Range 1/2

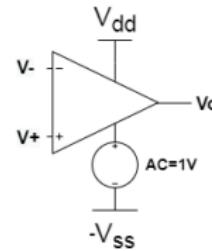
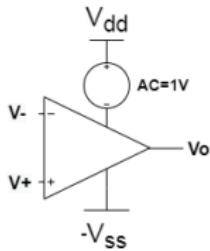
Schematic Simulations

- The PSRR defines the capability of rejecting the power supply AC component amplification.
- Let's put an AC signal at V_{DD} and see at the DC gain:

$$PSRR^+ = \frac{A_d}{\frac{dV_o}{dV_{DD}}} = 107.7 dB - 59.6 dB = 48.1 dB \quad (16)$$

- Similarly putting an AC component on V_{SS} :

$$PSRR^- = \frac{A_d}{\frac{dV_o}{d(-V_{SS})}} = 107.7 dB - 67.3 dB = 40.4 dB \quad (17)$$



Power Supply Rejection Range 2/2

Schematic Simulations

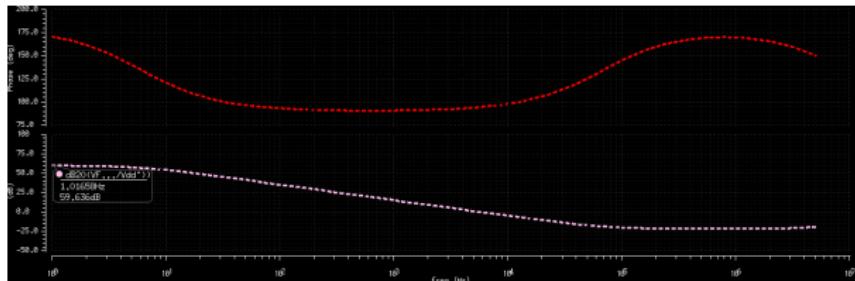


Figure: Positive Power Supply Rejection Range

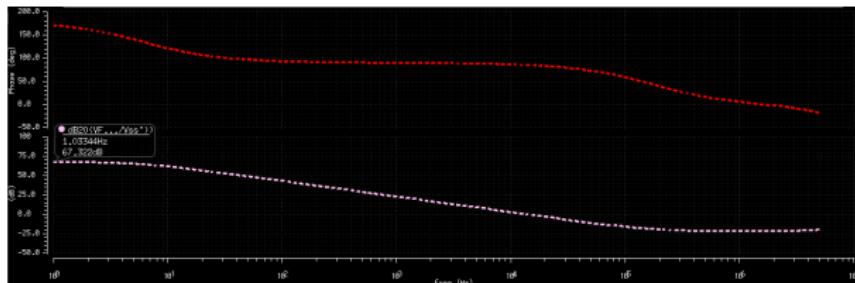
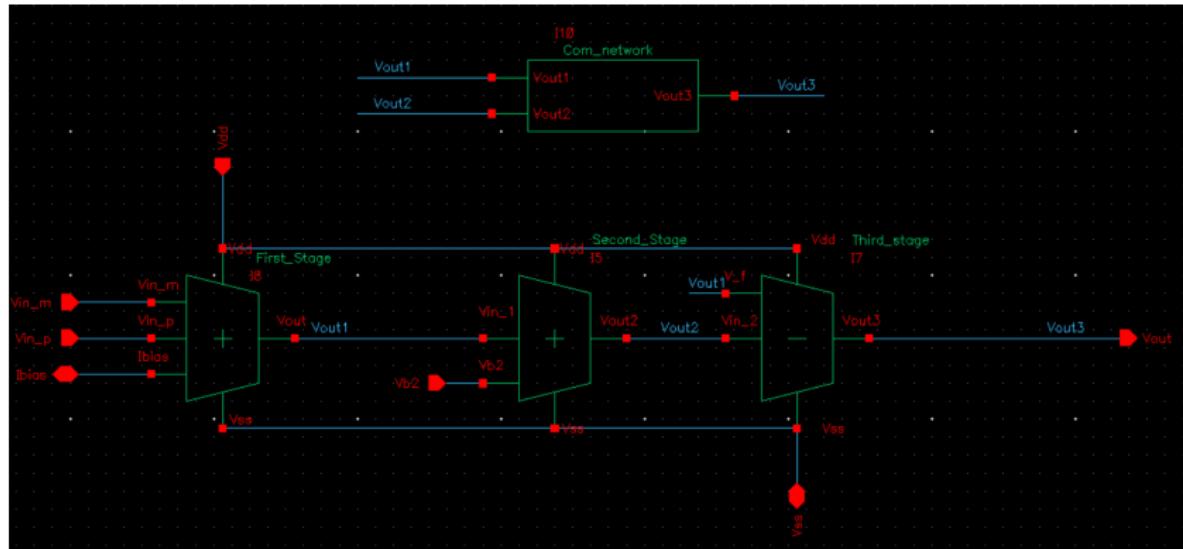


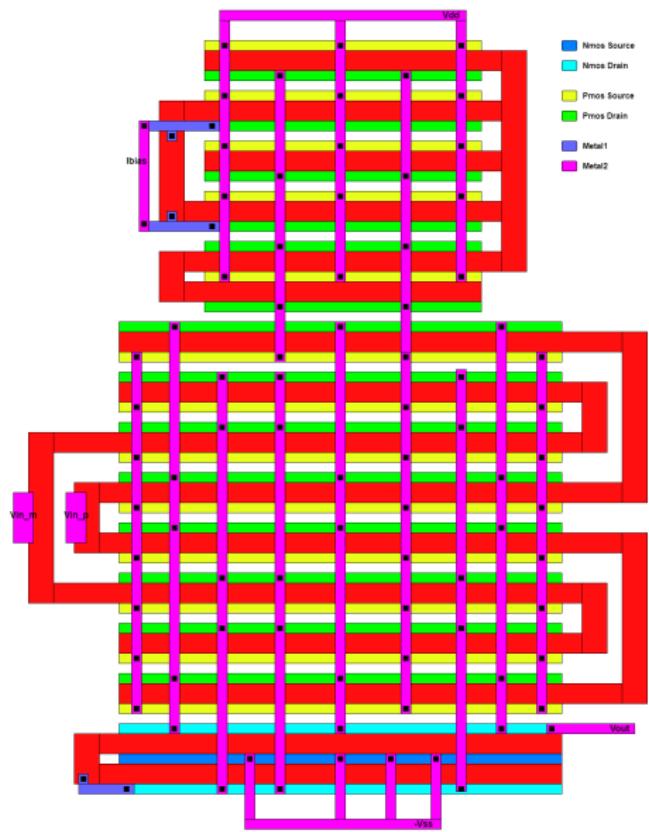
Figure: Negative Power Supply Rejection Range

Layout Implementation

- After schematic simulations, now let's design the OTA layout.
- It has been designed for each stage singularly.
- At the end all the layout views has been putted together.

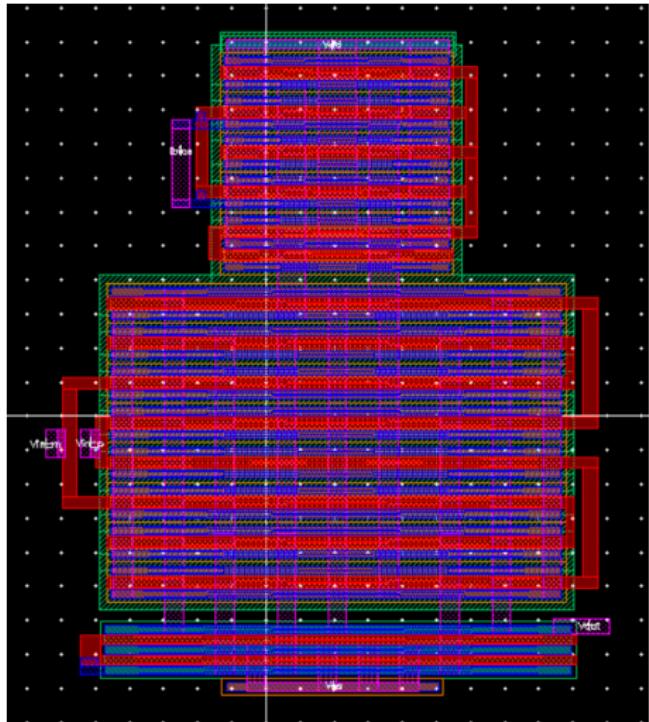


First Stage Stick Diagram



- *PMOS mirror:* M_{01} and M_0 respectively in 2 and 4 fingers in order to reduce the total width of the structure. Structure has been interdigitated as ABABAA, where A is associated to M_0 and B to M_{01} .
- *PMOS differential pair:* M_1 and M_2 dimensions are the same, the common centroid approach can be perfectly used. The structure has been interdigitated as ABBAABBA, where A is M_2 and B is M_1 .
- *NMOS mirror - pair load:* only 1 finger has been used for both M_3 and M_4 , which share the same source terminal.

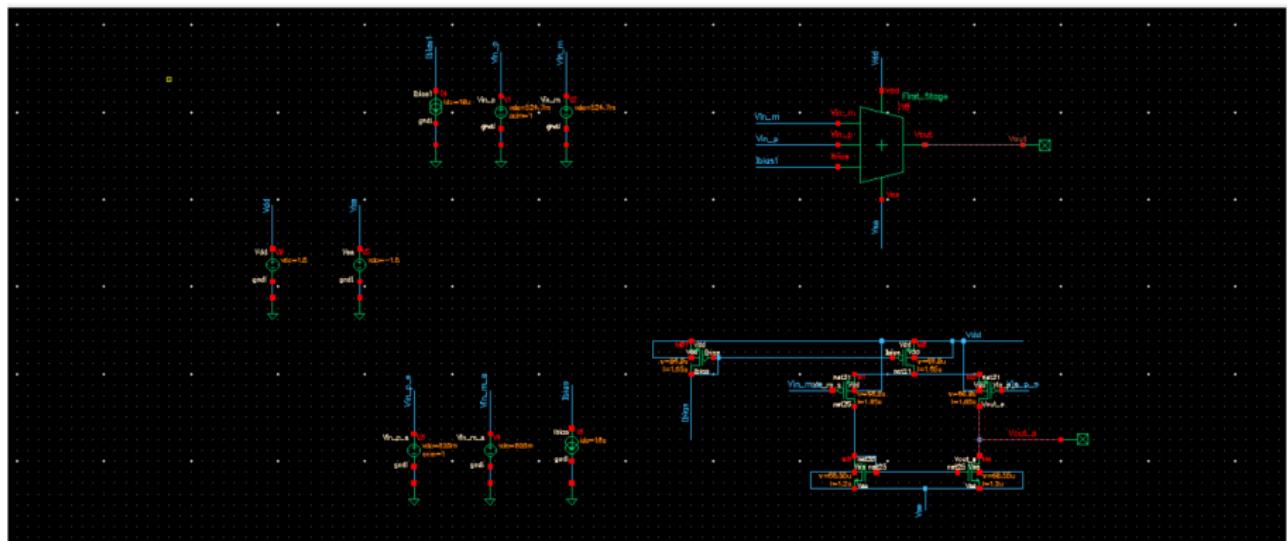
First Stage Layout



- The interconnections were implemented using the *Metal2*, because all the active areas have already a *Metal1* contact. Therefore, the *Metal2* was used with straight segments in order to minimize the interconnections lengths.
- Furthermore, the power supply input was developed by using the ntap to bias the PMOS substrate. An analogue discussion is valid for the NMOS substrate, but the ptap was used to connect it and the circuit to the negative power supply.

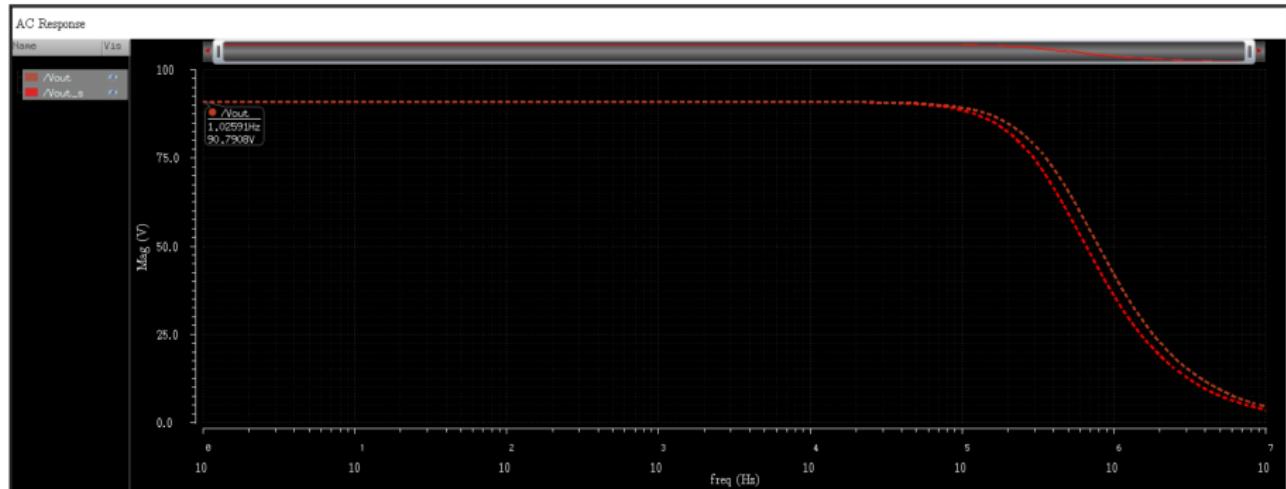
First Stage Layout Simulation 1/3

- The layout and schematic first stages have been simulated together in order to make a comparison between them.
- The symbol is used to simulate the extracted view and compare it with the schematic below.



First Stage Layout Simulation 2/3

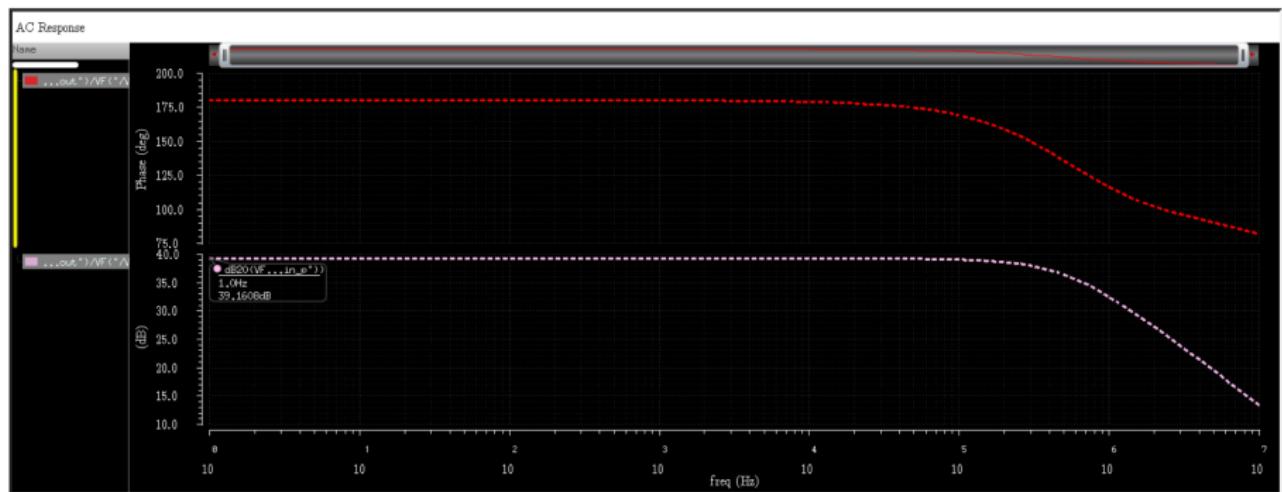
The AC simulation shows a coherent behavior of layout implementation since it is very similar to the schematic one.



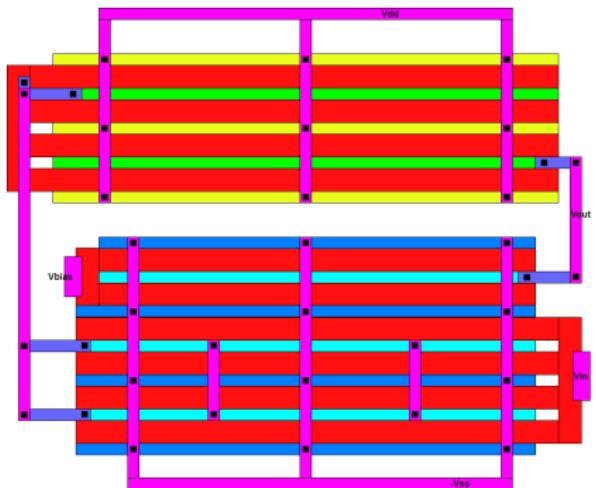
First Stage Layout Simulation 3/3

The AC simulation of extracted view provides:

- $G = 39dB$
- $B_{-3dB} = 300kHz$.

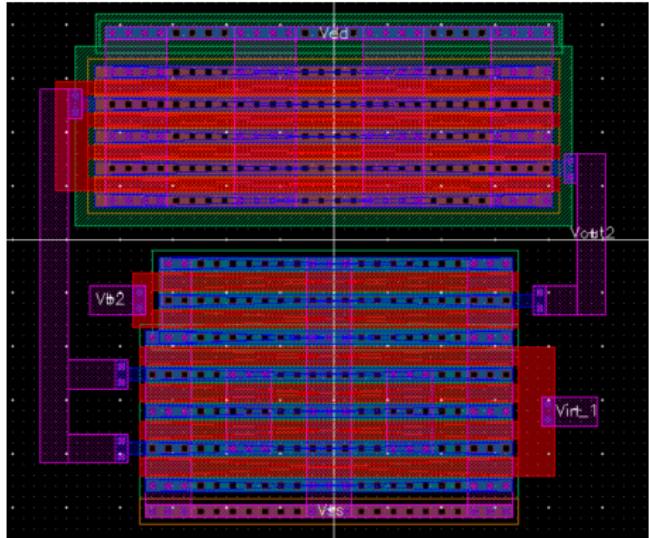


Second Stage Stick Diagram



- The second stage is composed by a cascade of two common source, connected together by using a PMOS current mirror network.
- PMOS mirror:* M_6 and M_7 , split in 2 fingers but not interdigitated in order to share the drain and source terminals, in fact the connection is AABB, where A is M_6 and B is M_7 .
- NMOS:* M_8 and M_5 split respectively in 2 and 4 fingers, and not interdigitated because the two transistors are completely separated.

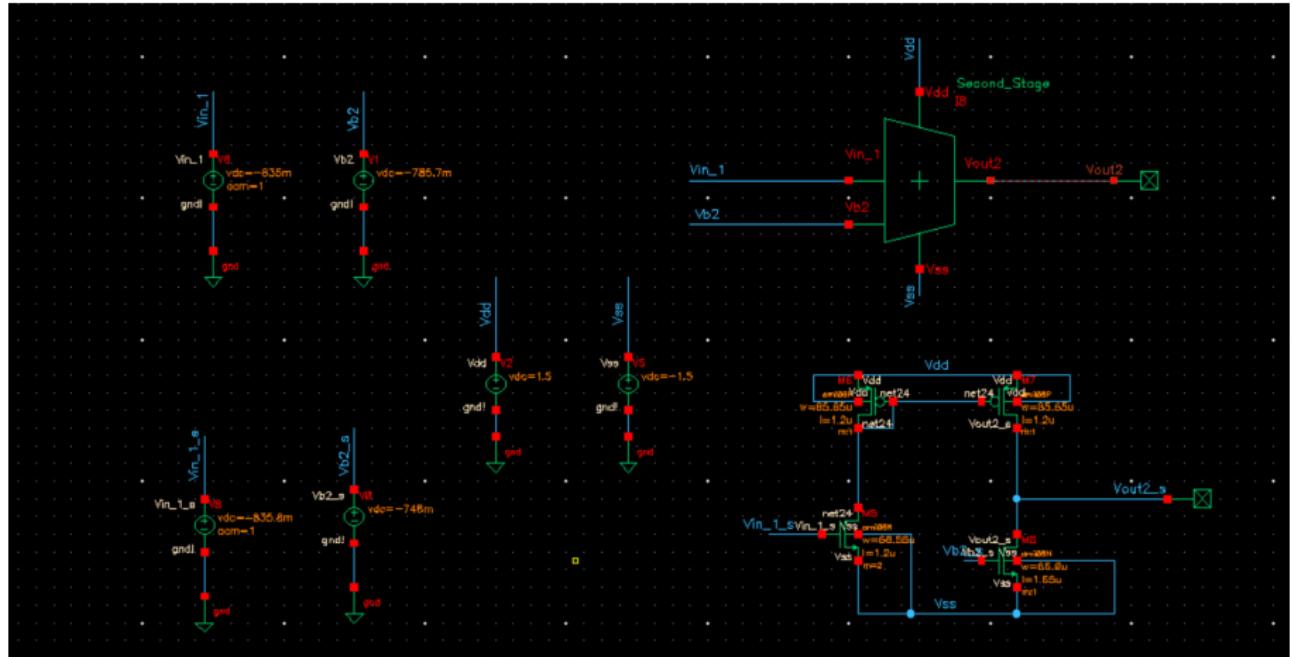
Second Stage Layout



- The interconnections were implemented using the *Metal2*, because all the active areas have already a *Metal1* contact. Therefore, not all the *Metal2* lines don't pass over the transistors but out, that due to the larger width of PMOS than NMOS.
- Furthermore, the power supply input was developed as the previous stage.
- The input pin and the output pin were placed both on right, the M_8 bias pin was placed on left.

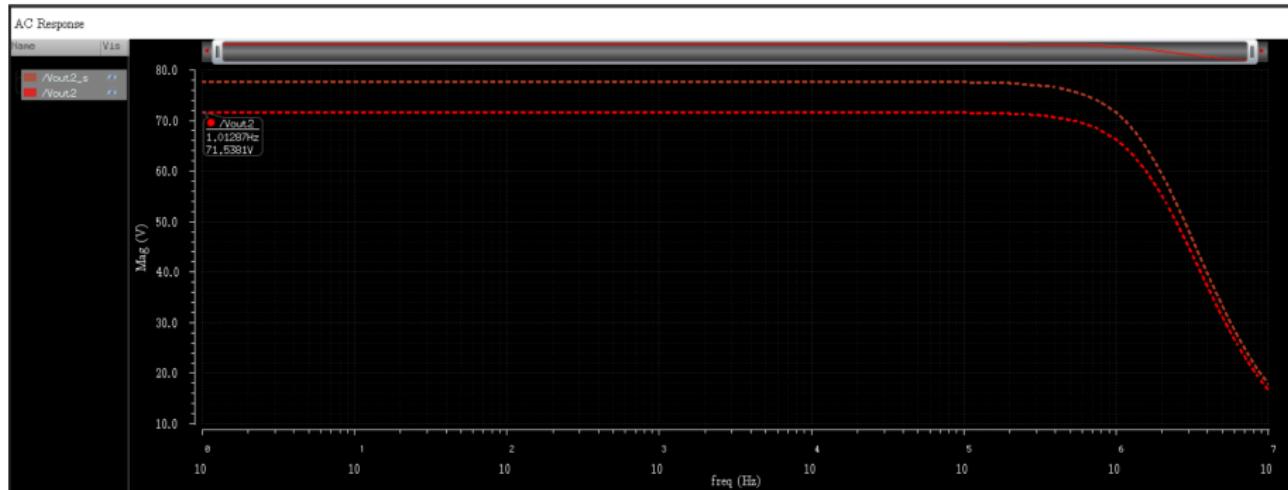
Second Stage Layout Simulation 1/3

Again, a comparison between schematic and extracted view has been performed.



Second Stage Layout Simulation 2/3

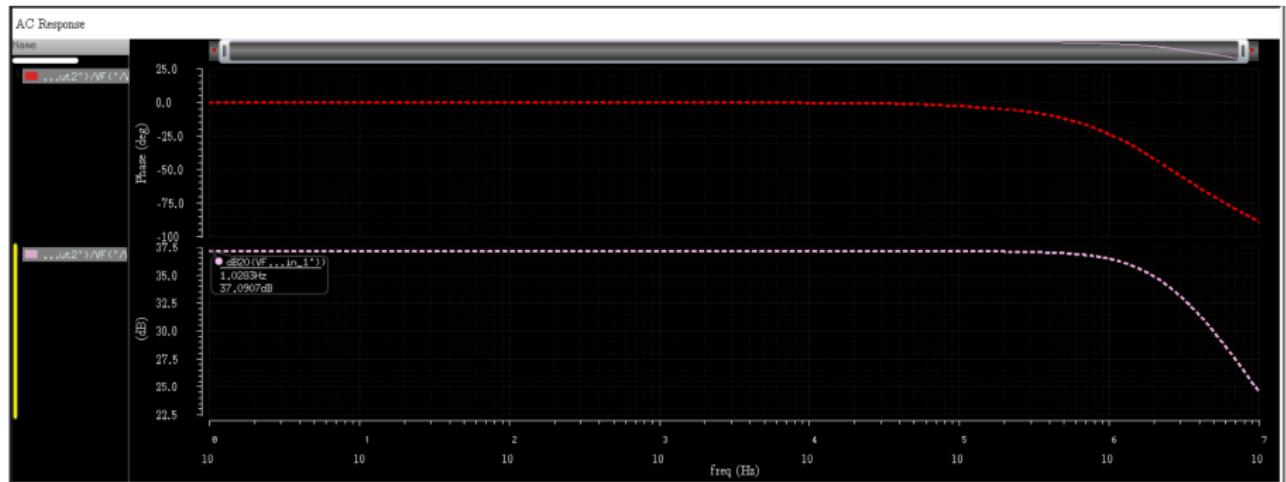
Making an AC simulation, notice that gain is low in the layout implementation than in the schematic one, while the bandwidth is a little bit larger:



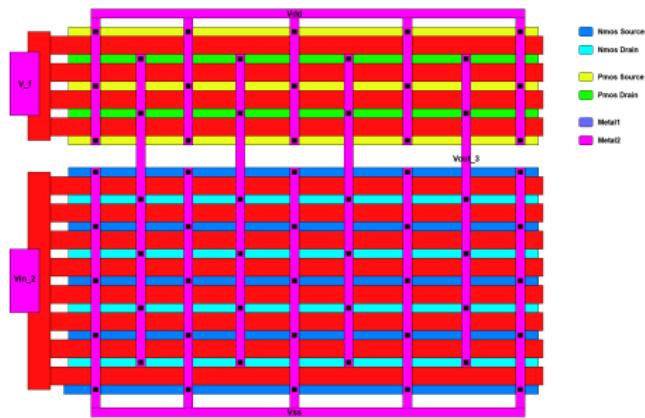
Second Stage Layout Simulation 3/3

Gain and the GBW frequency can be extracted by Bode plots:

- $G = 37dB$
- $B_{-3dB} = 2.45MHz$



Third Stage Stick Diagram



- *PMOS:* M_9 is the feedforward responsible and it is made by 4 fingers.
- *NMOS:* M_{10} is composed by 8 fingers and due to that it has the higher transconductance and the aspect ratios are the same of the previous PMOS.
- In this case an interdigitated or common centroid structure were not possible due to the presence of only one NMOS and one PMOS.

Third Stage Layout

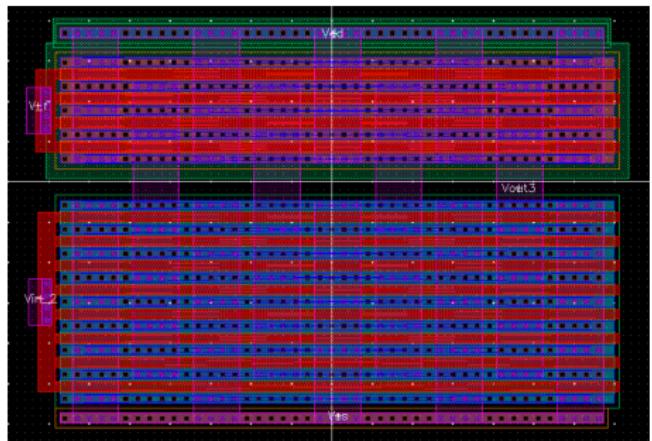
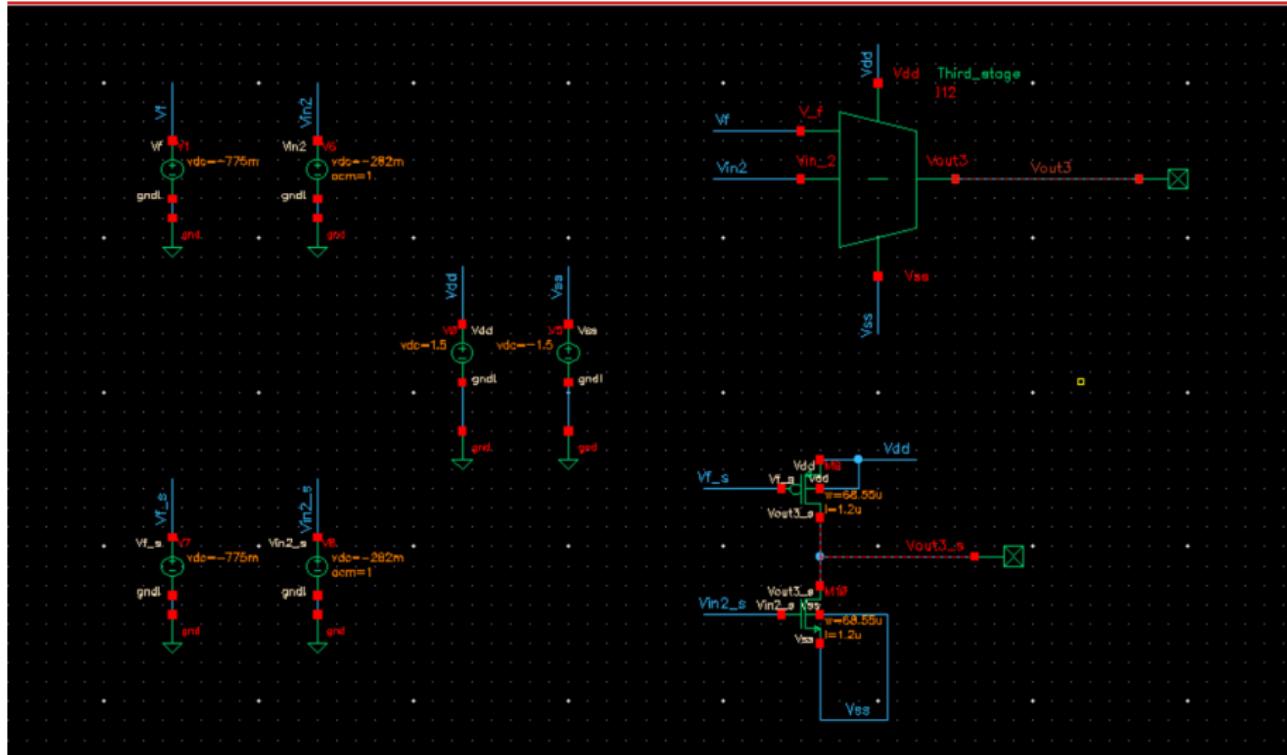


Figure: Third Stage Layout

- The routing is developed in a compact way with the power supply equally distributed to the active areas.
- On M_9 transistor there are five Metal2 lines that deliver the positive power supply to the finger sources. Also the linking between the two transistors and the routing between NMOS source and the negative power supply were designed with the same technique
- All the metal lines pass on the transistor structure and the inputs and output pins are in line with the previous stages.

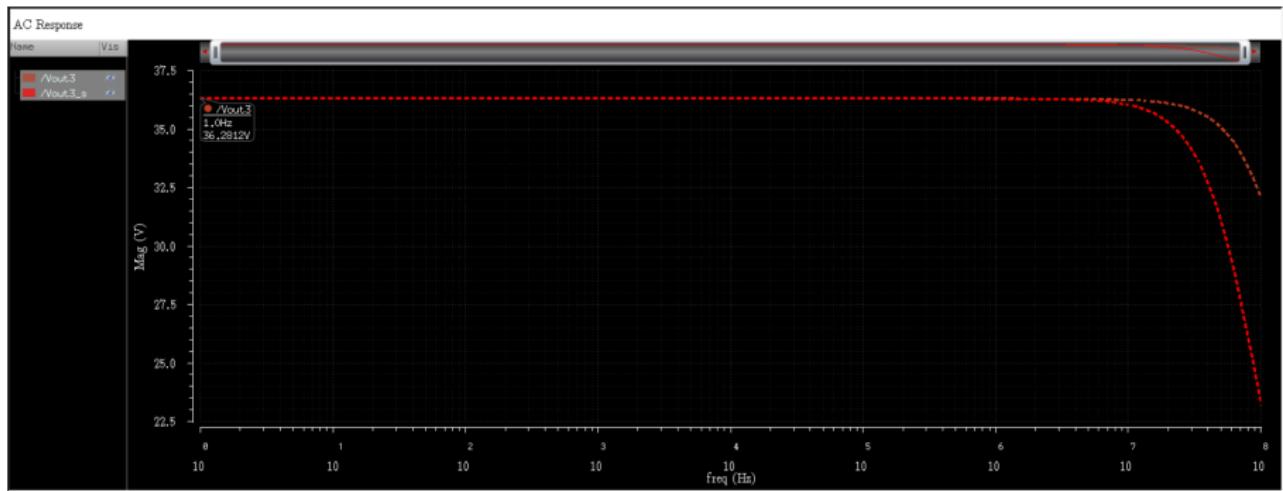
Third Stage Layout Simulation 1/3

Also for the third stage a layout vs schematic simulation has been made.



Third Stage Layout Simulation 2/3

Even for the third stage, the frequency behavior is little better than the schematic in terms of bandwidth.

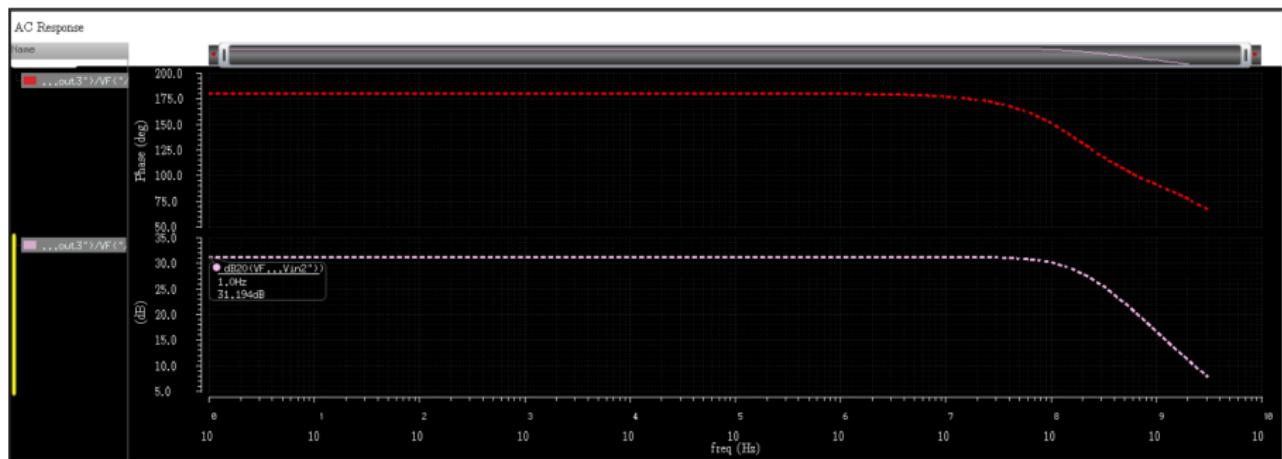


Third Stage Layout Simulation 3/3

The Bode plots are represented in order to compute:

- $G = 31.19dB$
- $B_{-3dB} = 187.9MHz$

Although the third stage is the one with the lowest gain considering all stages, it exhibits the highest bandwidth (coherent with Miller effect theory).

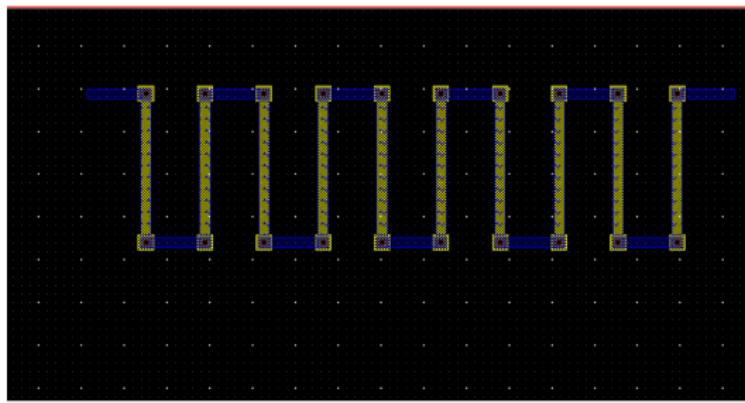


Compensation Network 1/5

- The first component designed was the $R_{C2} = 156.2 \text{ k}\Omega$ resistance.
- The more suitable material was the *Poly2_HR*, which square resistance is $R_{\square} = 1076 \Omega/\square$.

$$\frac{L}{W} = \frac{156.2 \text{ k}\Omega}{1076 \frac{\Omega}{\square}} = 145.17 = \frac{17.42 \mu\text{m}}{1.2 \mu\text{m}} \quad (18)$$

- The resistance was divided in ten smaller resistance with a length of $L = 17.42 \mu\text{m}$, obtaining finally $R_{C2} = 155 \text{ k}\Omega$.

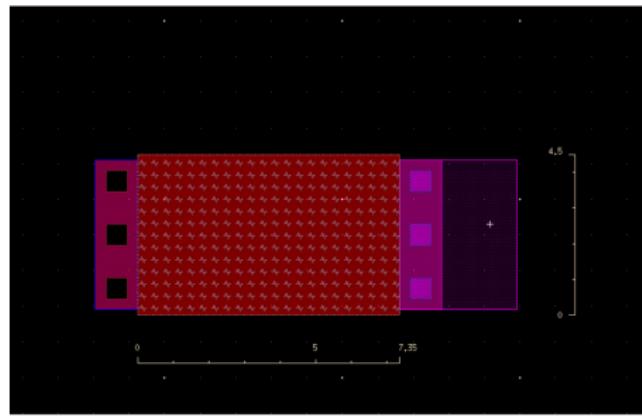


Compensation Network 2/5

- Resistance $R_{C1} = 45.8 \Omega$ is not designed in *Poly2_HR* since the *Poly1* seemed more suitable with its square resistance of $R_{\square} = 23.2 \frac{\Omega}{\square}$.
- Computing the dimensions:

$$\frac{L}{W} = \frac{45.8 k\Omega}{23.2 \frac{\Omega}{\square}} = 1.97 \quad (19)$$

- By implementing a width $W = 4.5 \mu m$, the length become $L = 8.88 \mu m$. Looking at extracted view, it was adjusted to $L = 7.35 \mu m$, obtaining $R_{C1} = 45.54 \Omega$.



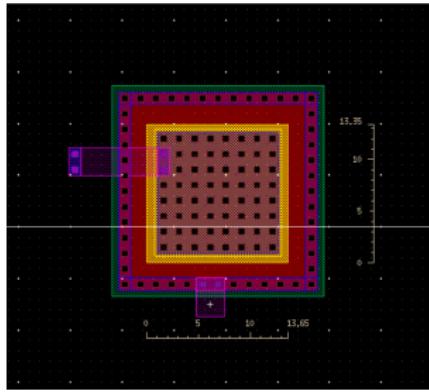
Compensation Network 3/5

- For $C_{C2} = 145.5fF$, the chosen materials are *Poly1* and *Poly2*, due to their large capacitance per unit area of $C_{PUL} = 922aF/\mu m^2$.

$$Area = \frac{C_{C2}}{C_{PUL}} = \frac{145500aF}{922aF/\mu m^2} = 157.809 \mu m^2 \quad (20)$$

$$Edge = \sqrt{157 \mu m^2} = 12.56 \mu m \quad (21)$$

- Looking at extracted view, $L = 13.65 \mu m$ and $W = 13.35 \mu m$ provides $C_{C2} = 145.4 fF$.



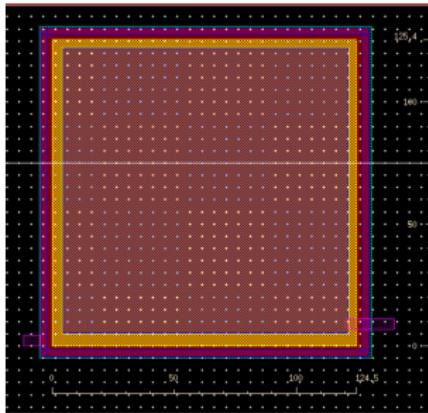
Compensation Network 4/5

- Also $C_{C1} = 12.46 \text{ pF}$ has been designed with *Poly1* and *Poly2*.

$$Area = \frac{C_{C2}}{C_{PUL}} = \frac{12.46 \cdot 10^6 \text{ aF}}{922 \text{ aF}/\mu\text{m}^2} = 13514.1 \mu\text{m}^2 \quad (22)$$

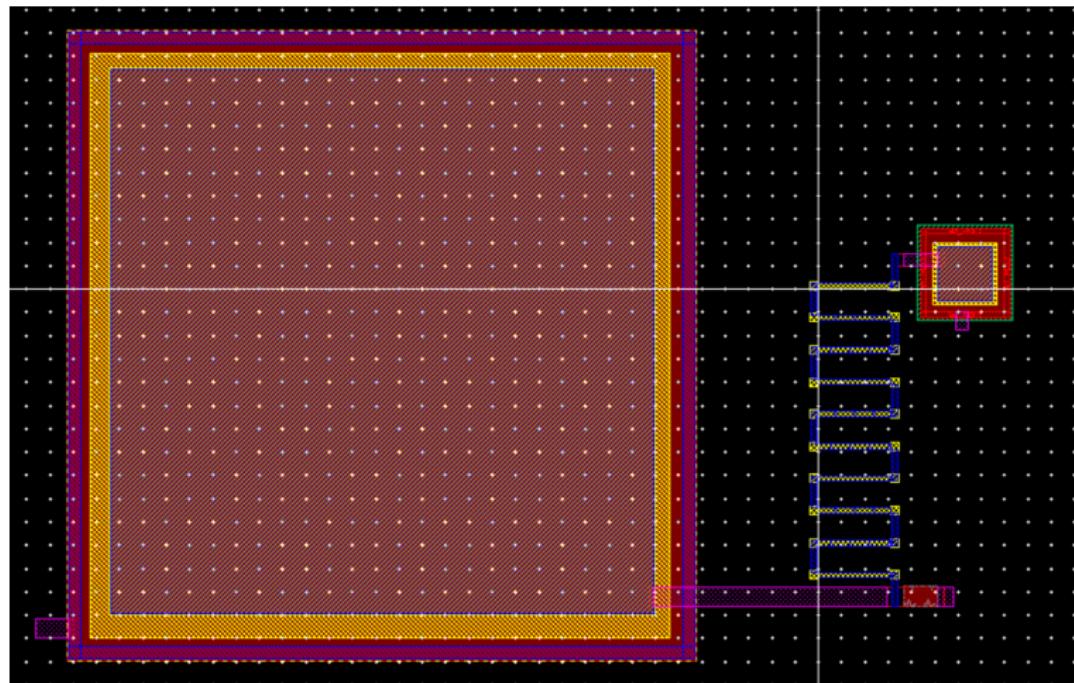
$$Edge = \sqrt{13514.1 \mu\text{m}^2} = 116.25 \mu\text{m} \quad (23)$$

- Looking at the extracted view, $L = W = 125.4 \mu\text{m}$ has been used since $C_{C2} = 12.46 \text{ pF}$ is achieved.



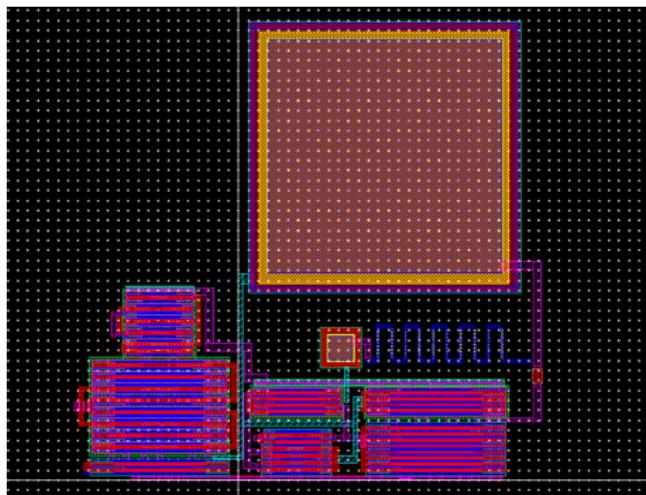
Compensation Network 5/5

In the complete scheme of the compensation network all the component are connected together:



Final Layout

- All the stages and the compensation network are connected together.



- There are reduced much as possible the connections length, the total area and the parasitic parameters.
- The structure implemented has a square form to better occupy the area of the chip without any waste.
- Metal2* is used to connect together the positive power supply of every stage, V_{DD} , and also for the negative one V_{SS} .
- Metal3* is used to connect each other all the three stages and the two compensation capacitance, because it was the only way to connect all without exploiting any long or complex routing.

Layout Dimensions



- Layout area is estimated using the ruler to obtain the total dimension of the chip.
- Base = $241.95 \mu m$.
- Height = $(477.6 - 241.95) \mu m = 235.65 \mu m$.
- Area $A = 0.057 mm^2$.
- The area obtained is less respect the one of the paper, because the compensation capacitance used are smaller respect the ones of the paper, that it has been said equal to about the 80% of the total layout area.

Extracted and Symbol view

- An extracted view is obtained from the layout one.
- Also the symbol view is made to use it for the various simulations, where it is necessary to place the *extracted* in the Setup Environment.

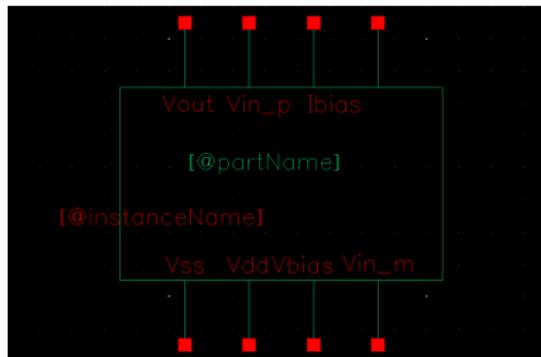
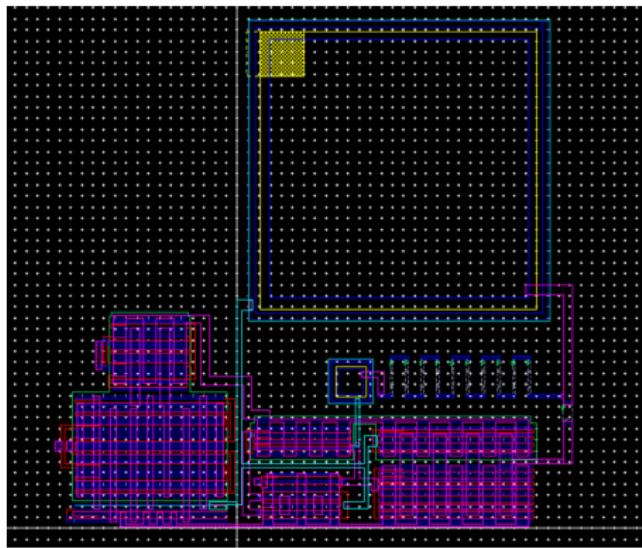
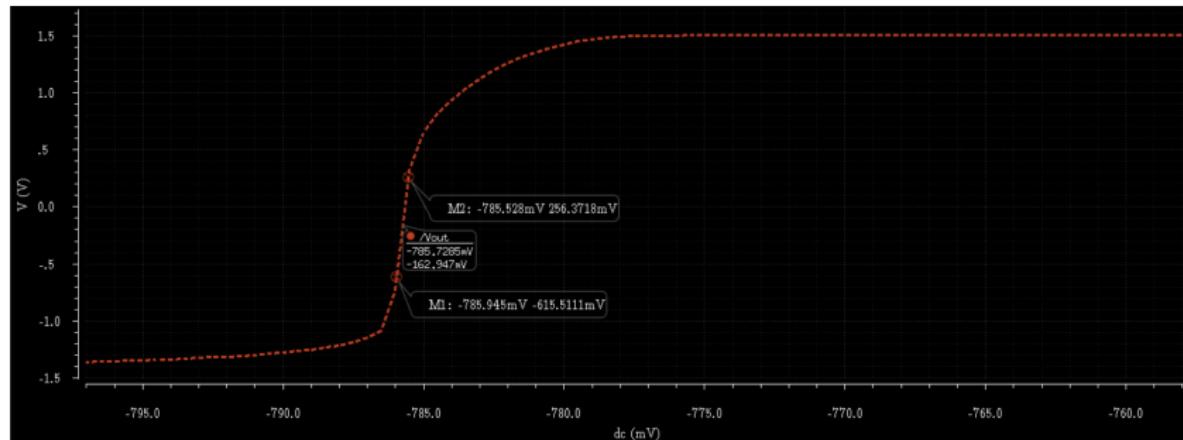


Figure: OTA Symbol View

DC sweep 1/2

Layout simulations

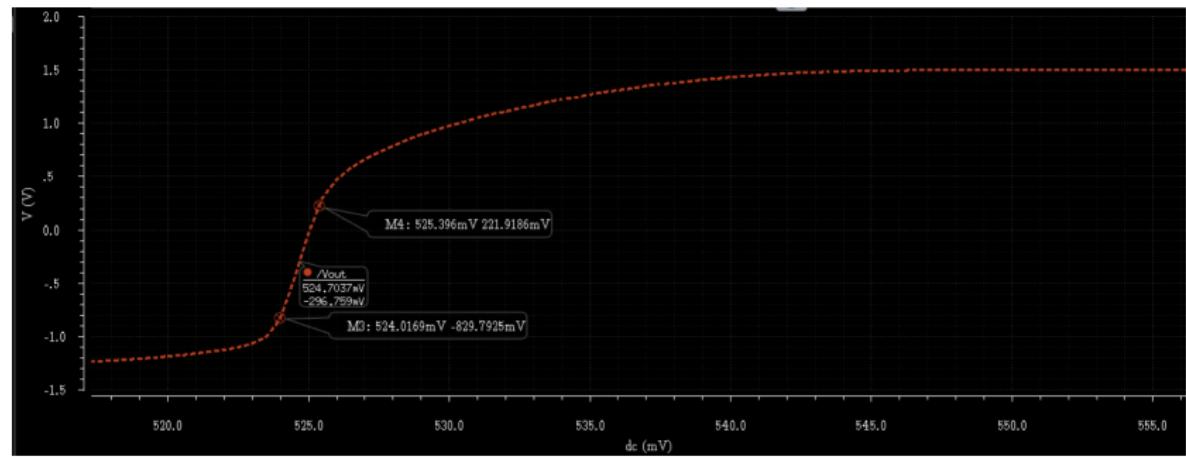
- Let's work in open loop, imposing $V_{inm} = V_{inp}$.
- Select at first V_{b2} generator to sweep between $-1.6V$ and $+1.6V$, linear sweep with step size of $0.5 mV$.
- The optimum bias point found is $V_{b2} = -785.7 mV$.



DC Sweep 2/2

Layout Simulations

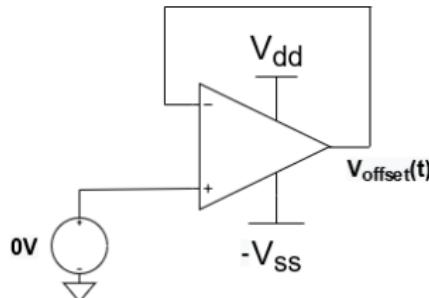
- Again, the same simulation as before has been performed, this time selecting V_{inp} generator to sweep.
- The optimum bias point found for $V_{inp} = 524.7 \text{ mV}$.



Input Offset Voltage

Layout Simulations

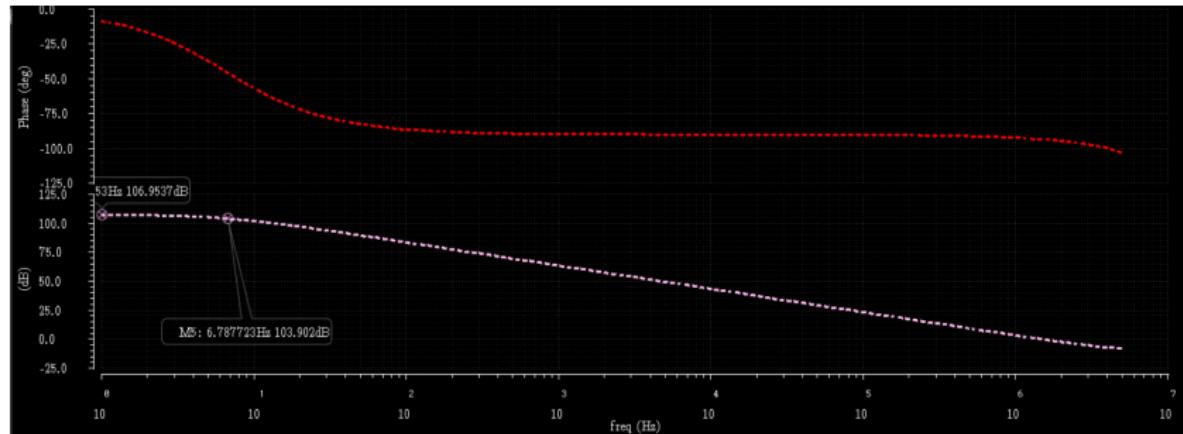
- To perform this simulation, a closed loop configuration has been set using $V_{out} = V_{inm}$.
- V_{inp} has been set to a DC Voltage= 0 and also AC Magnitude= 0.
- Looking at the output value, it is different from zero. The input offset voltage is equal to $-275 \mu V$, that it is generally a very small value for an OTA offset.



AC Open Loop 1/2

Layout Simulations

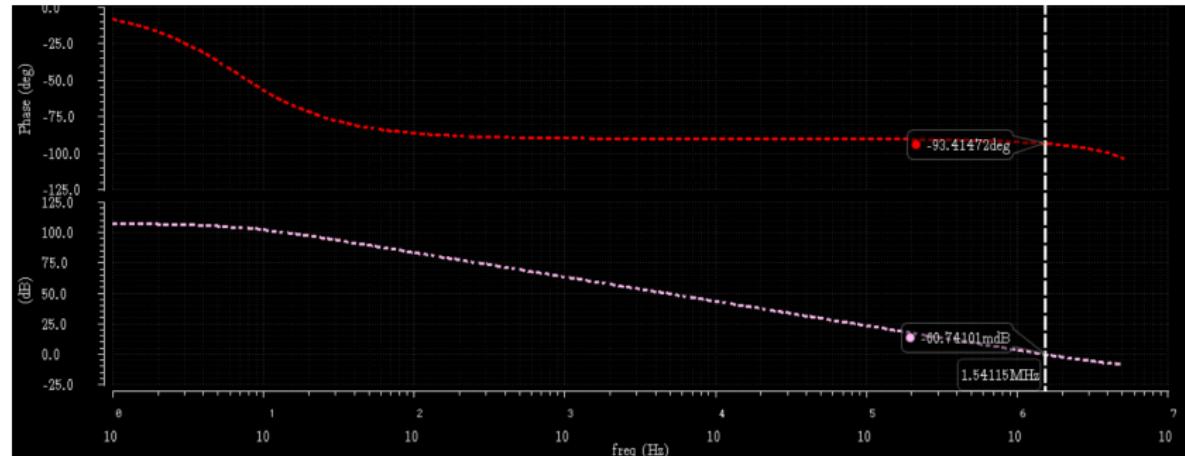
- Simulation in open loop is done to see at gain and phase Bode plots.
- Therefore, Choose Analysis/AC, sweep variable is the frequency, with a range from 1 Hz to 5 MHz, sweep type Logarithmic within 20 points per decade.
- Notice that the DC open loop gain is 107 dB, while the first pole has $f = 6.6 \text{ Hz}$ corresponding at gain 104 dB.



AC Open Loop 2/2

Layout Simulations

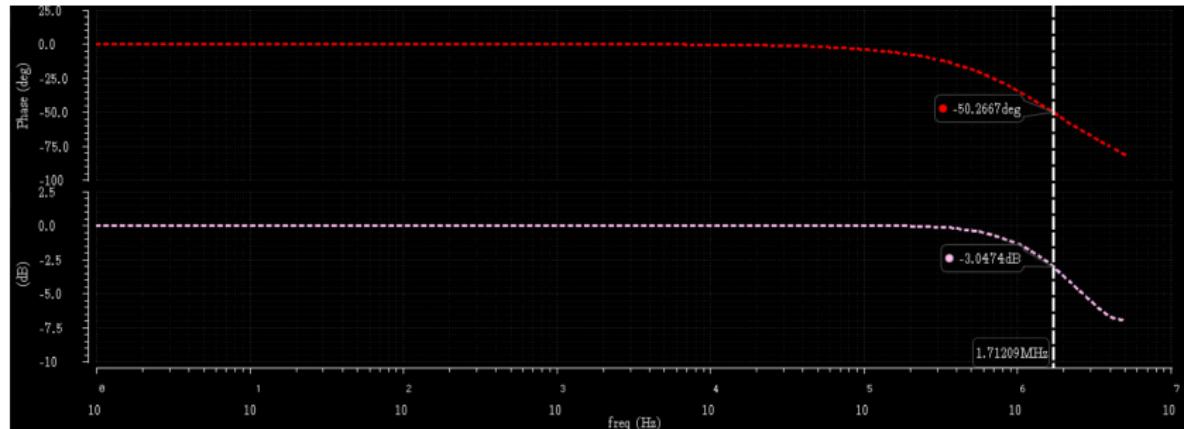
- At the transition frequency, when the gain equal to 0 dB, $f_T = 1.54 \text{ MHz}$ at the phase -93.4° .
- In this position the phase margin is evaluated, finding $PM = (180 - 93.4)^\circ = 86.6^\circ$.
- This is a very large value, so the system is in deep stability.



AC Closed Loop

Layout Simulations

- The Gain-BandWidth product is found at -3 dB .
- $GBW = 1.71 \text{ MHz}$ at a phase=50.2°



Step Response 1/4

Layout Simulations

- Simulation performed in closed loop condition.
- An input step is applied on V_{inp} , with an amplitude between -200 mV and 200 mV , rise time and fall time equal to 700 ns , pulse width = $2.5 \mu\text{s}$ and period = $6 \mu\text{s}$.
- Choose a .tran simulation with a stop time = $100 \mu\text{s}$.
- The rise time between 10% and 90% is $t_r = 583.6 \text{ ns}$.

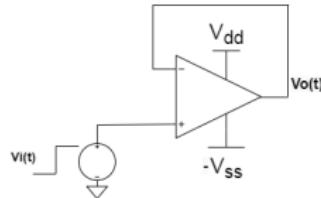
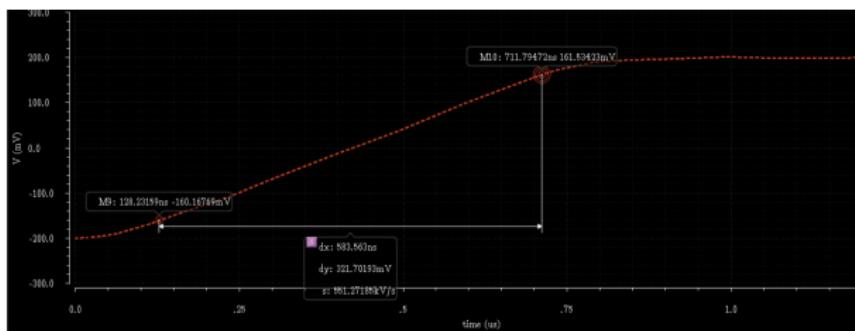


Figure: SR scheme



Step Response 2/4

Layout Simulations

- The settling time is the time required for the response curve to reach and stay within a range of 1% of the final value (i.e. 198mV).
- $\text{settling_time}^+ = 942.3 \text{ ns}$.

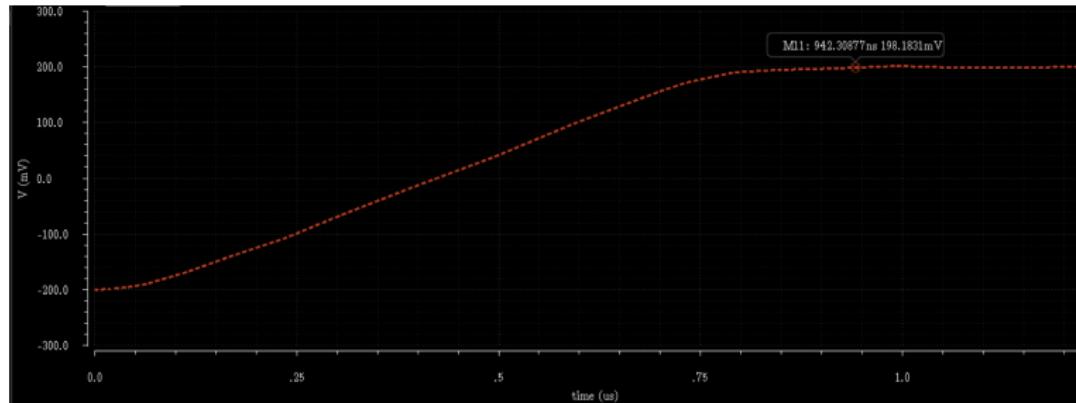
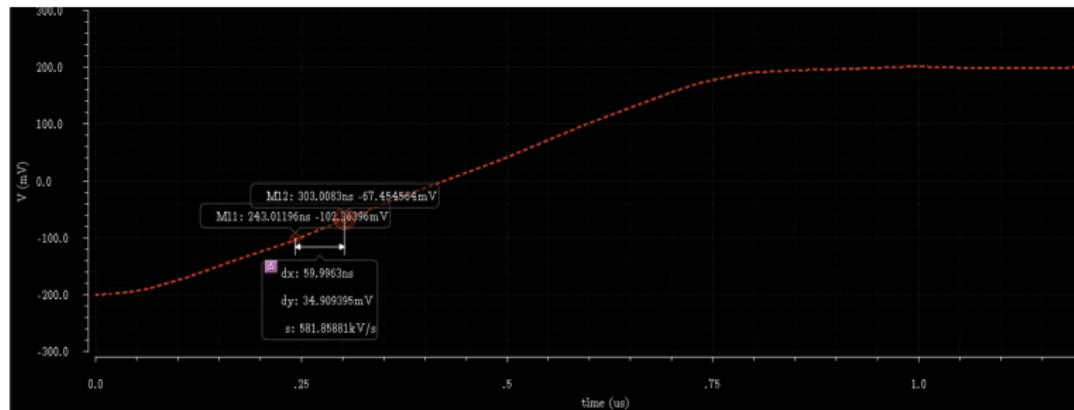


Figure: Positive Settling Time

Step Response 3/4

Layout Simulations

- The Slew rate is defined as the rate of change of the output voltage per unit time.
- It defines how fast is the circuit to respond at the input stimulus.
- Looking at the maximum slope points, $SR^+ = 0.58 \text{ V}/\mu\text{s}$



Step Response 4/4

Layout Simulations

- All the previous parameters have been also computed for the falling edges.
- $t_f = 575.21 \text{ ns}$
- $\text{settling_time}^- = 972.3 \text{ ns}$
- $SR^- = 0.61 \text{ V}/\mu\text{s}$
- The result are generally worst than rising edge but anyway comparable.

Common Mode Rejection Range 1/2

Layout Simulations

- The CMRR expresses the ability of a differential amplifier to reject the common mode voltage.
- To find it, the common mode gain has to be found.
- Let's put an AC signal both on positive and negative inputs and look at the DC gain.

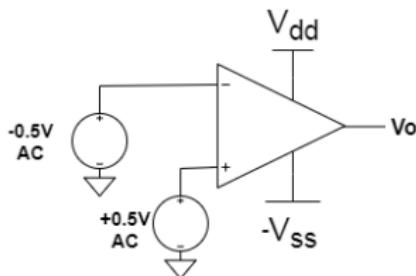


Figure: Scheme to determine A_d

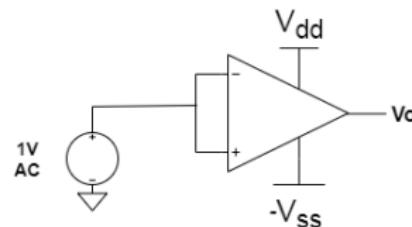
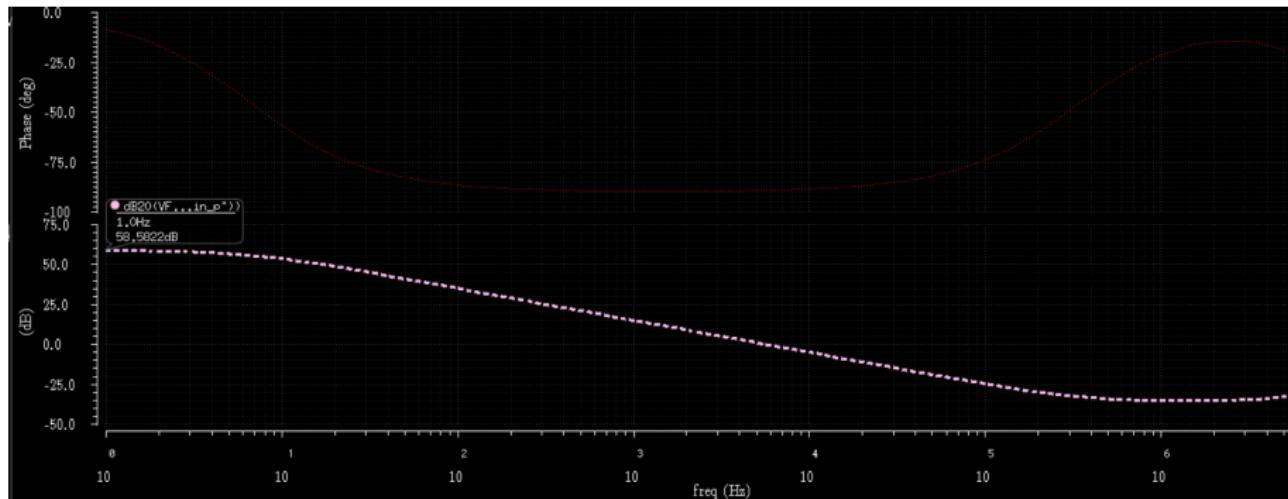


Figure: Scheme to determine A_c

Common Mode Rejection Range 2/2

Layout Simulations

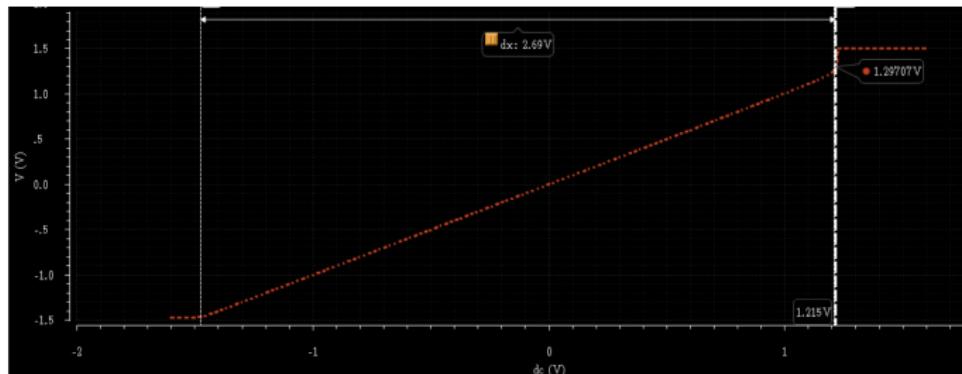
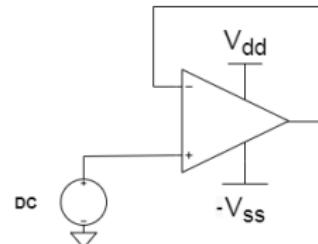
- $A_{d,dB} = 107 \text{ dB}$
- $A_{c,dB} = 58.6 \text{ dB}$
- $\text{CMRR} = A_{d,dB} - A_{c,dB} = 48.4 \text{ dB}$



Common Mode Range

Layout Simulations

- The CMR is the range of input voltage values for which it is guaranteed that all transistors remain in saturation.
- Let's make an input DC sweep in closed loop configuration.
- $CMR = CMR^+ - CMR^- = 1.209V - (-1.474)V = 2.683V$



Power Supply Rejection Range 1/2

Layout Simulations

- The PSRR define the capability of rejecting the power supply AC component amplification.
- Let's put an AC signal at VDD and see at the DC gain.

$$PSRR_+ = \frac{A_d}{\frac{dV_o}{dV_{DD}}} = 107 \text{ dB} - 58.8 \text{ dB} = 48.2 \text{ dB} \quad (24)$$

- Let's put an AC signal at VSS and see at the DC gain.

$$PSRR_- = \frac{A_d}{\frac{dV_o}{d(-V_{SS})}} = 107 \text{ dB} - 67.2 \text{ dB} = 39.8 \text{ dB} \quad (25)$$

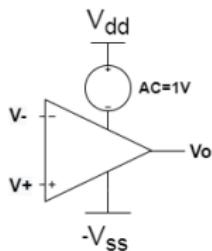


Figure: $PSRR_+$

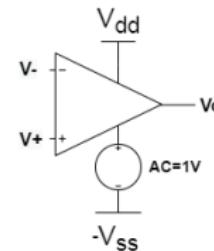


Figure: $PSRR_-$

Power Supply Rejection Range 2/2

Layout Simulations

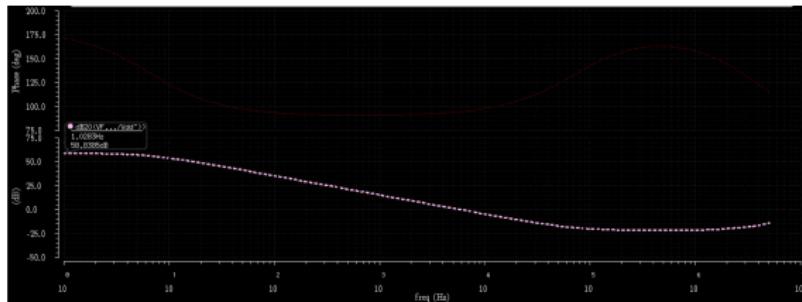


Figure: Positive Power Supply Rejection Range

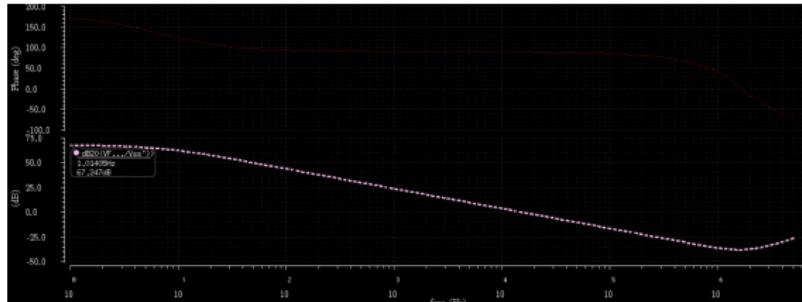
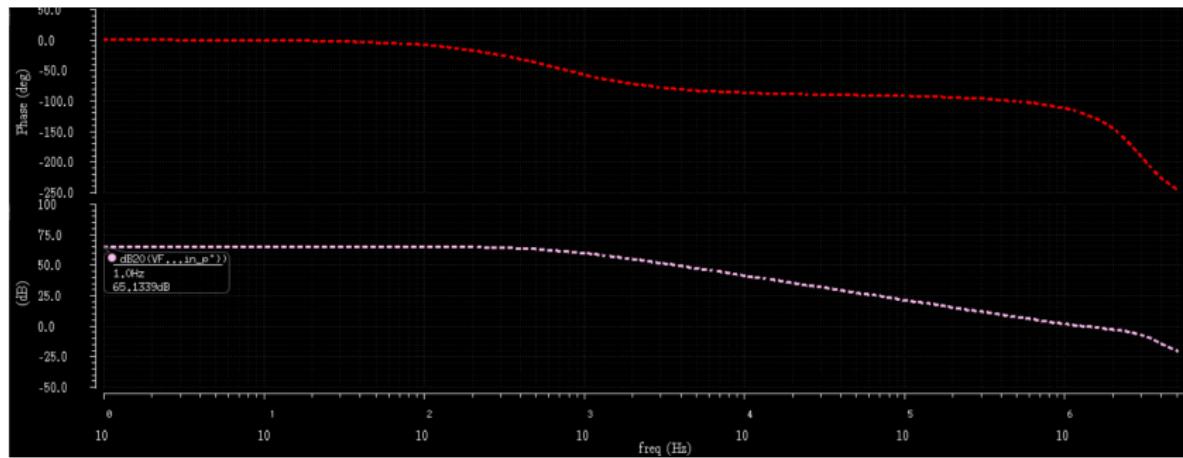


Figure: Negative Power Supply Rejection Range

$T = 85^\circ$ Simulations 1/3

Layout Simulations

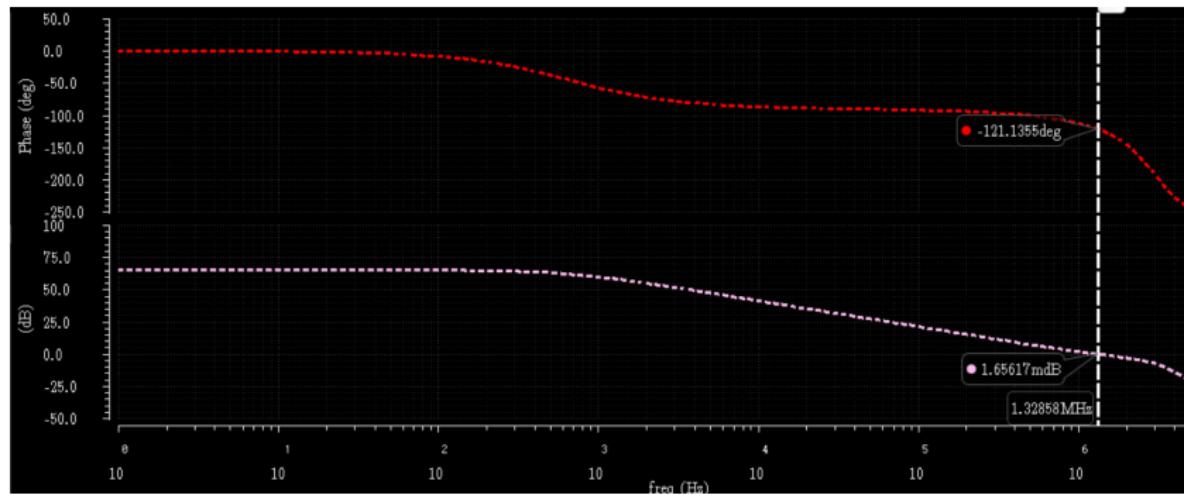
- An AC simulation has been performed at 85° .
- In this case DC open loop gain decrease to 65.13 dB
- the first pole is at $f = 652\text{ Hz}$.
- GBW remains anyway constant.



$T = 85^\circ$ Simulations 2/3

Layout Simulations

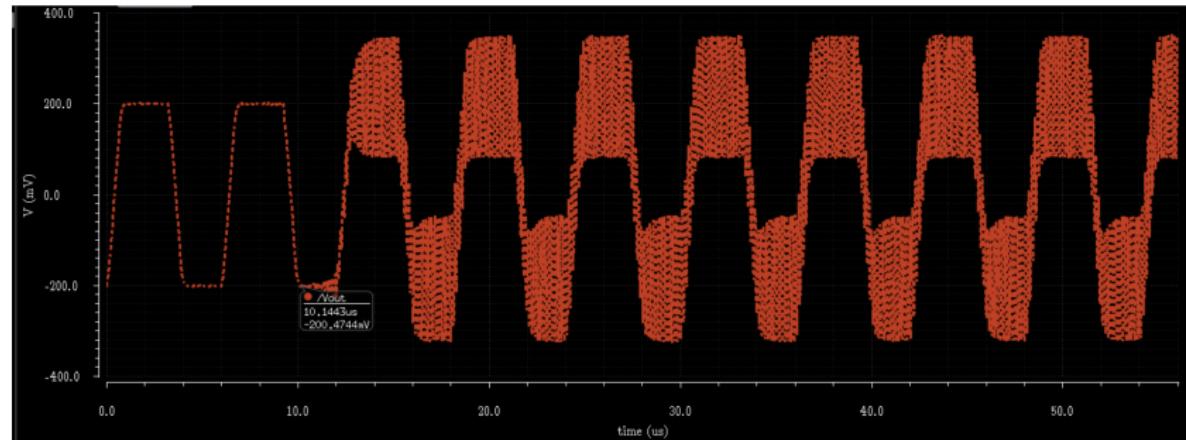
- The transition frequency is $f_T = 1.33 \text{ MHz}$ at the phase -121.1° .
- The phase margin decrease even at $PM = (180 - 121.1)^\circ = 58.9^\circ$



$T = 85^\circ$ Simulations 3/3

Layout Simulations

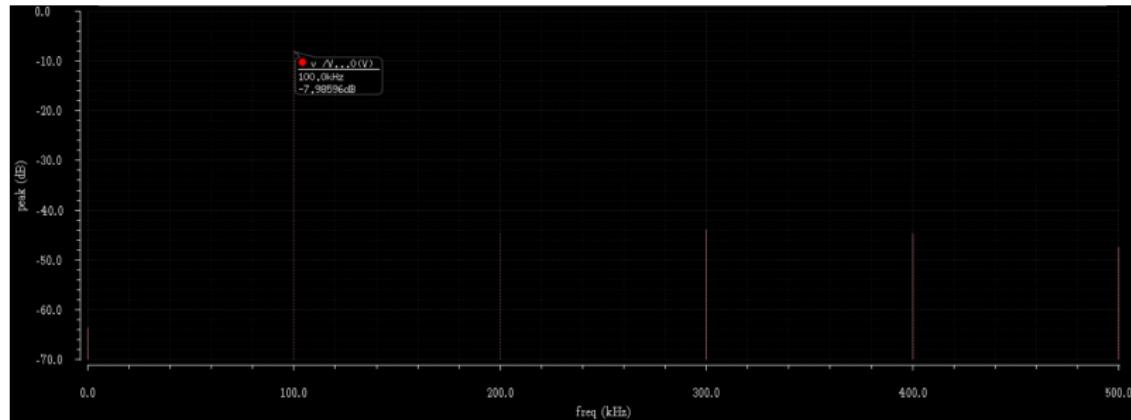
- Performing a step response at $T = 85^\circ$ with rise/fall time 700 ns , the system present an unstable behaviour:



Harmonic Distortion 1/2

Layout Simulations

- It provides a measure of the linearity of amplifier.
- This is done using input and output ports and an input source of 400 mV amplitude at 100 kHz and performing a *pss* simulation.



Harmonic Distortion 2/2

Layout Simulations

- Looking at the simulation results:

P_1	P_2	P_3
-8 dB	-44.8 dB	-44 dB

Using the Harmonics Distortion definition:

$$\begin{aligned} HD_2 &= P_2 - P_1 = -36.8 \text{ dB} \\ HD_3 &= P_3 - P_1 = -36 \text{ dB} \end{aligned} \tag{26}$$

- The same simulation has been performed for a 500 mV input amplitude:

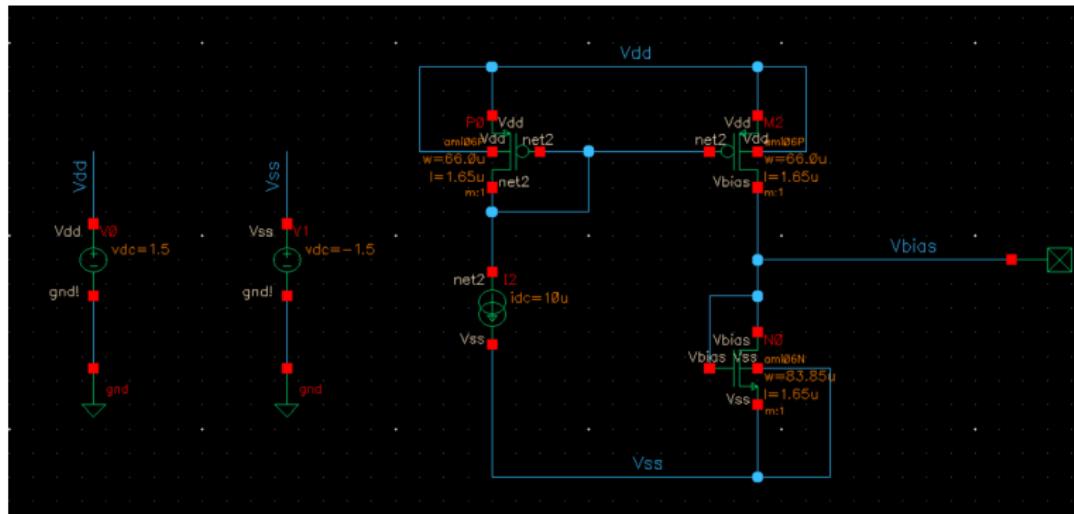
P_1	P_2	P_3
-6 dB	-34.5 dB	-35.3 dB

The HD values are:

$$\begin{aligned} HD_2 &= P_2 - P_1 = -28.5 \text{ dB} \\ HD_3 &= P_3 - P_1 = -29.3 \text{ dB} \end{aligned} \tag{27}$$

Voltage Reference 1/2

- Until now, voltage and current generator has been supposed to be ideal and external to the chip.
- In this section, a more realistic case is exploited in order to integrate them within the circuit.



Voltage reference 2/2

- The current can be expressed as:

$$I_D = \frac{1}{2} \beta_n \left(\frac{W}{L} \right)_{M0} (V_{GS} - V_{TH})^2 \quad (28)$$

Reversing the previous expression, the aspect ratio of M_0 can be found.

- However, a DC sweep of W_{M0} has been performed looking at the V_{bias} value, finding: In this way:

$$\left(\frac{W}{L} \right)_{M0} = \frac{83.85}{1.65} \quad (29)$$

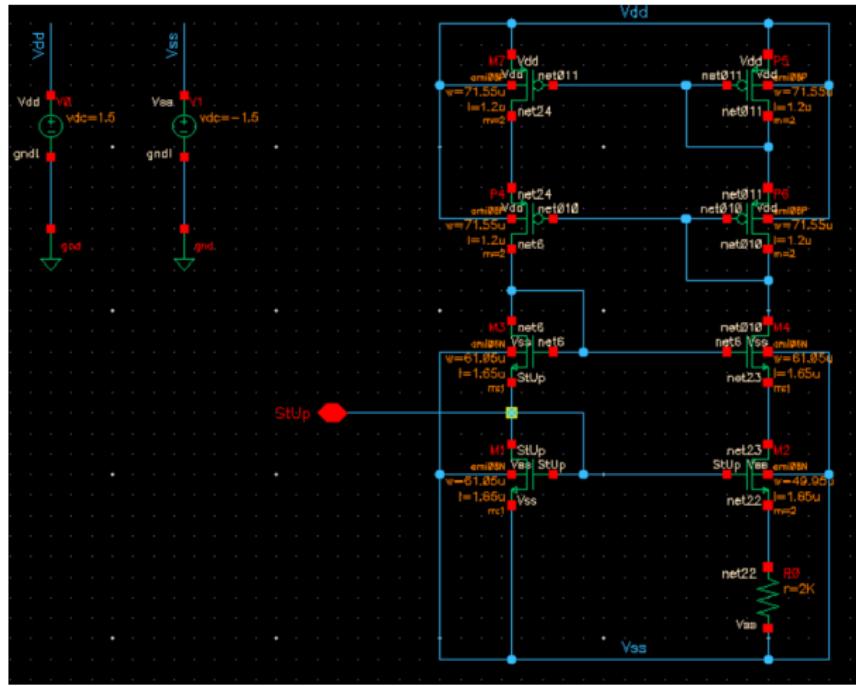
A *DC voltage node* simulation has been performed to verify that

$$V_{bias} = -785.8 \text{ mV}$$

Current Reference 1/3

Beta Multiplier

The beta multiplier has been designed in order to provide a reference current of $10\ \mu A$.



Current Reference 2/3

Beta Multiplier

- The main design formula for this kind of circuit is:

$$I_{ref} = \frac{2}{R^2\beta_1} \left(1 - \frac{1}{\sqrt{k}}\right) \quad (30)$$

Where k has been set equal to 2 and the resistance R equal to $2 k\Omega$.

- Inverting this equation, the aspect ratio of M_1 (and so of M_3 and M_4) can be found.

$$\left(\frac{W}{L}\right)_{M1} = \frac{2}{R^2 k_n I_{ref}} \left(1 - \frac{1}{\sqrt{k}}\right) = 37 \mu m \quad (31)$$

- Since $\beta_2 = k\beta_1$, the aspect ratio of M_2 is double than M_1 .
- Under the assumption that all the overdrives are almost equal, the PMOS aspect ratios are found.

Current Reference 3/3

Beta Multiplier

- Now, the transistor length has been fixed to:

$$\begin{aligned}L_n &= 1.65 \mu m \\L_p &= 1.2 \mu m\end{aligned}\tag{32}$$

- Finding these transistor widths:

$$\begin{aligned}W_2 &= 122 \mu m \\W_n &= 61 \mu m \\W_p &= 143 \mu m\end{aligned}\tag{33}$$

- At this point, a DC sweep of W_2 has been performed to find the exact value for which the reference current is $10 \mu A$, finding $W_2 = 100 \mu m$.
- An I_{bias} vs V_{DD} simulation has been performed, showing a quite stable behaviour of the current.
- One fundamental constrain is that the Beta Multiplier must be used with a start-up circuit.

Comparison between results of Schematic and Layout

PARAMETER	SCHEMATIC	LAYOUT
Technology	$0.6 \mu m$ CMOS	$0.6 \mu m$ CMOS
Area	-	$0.057 mm^2$
Power supply	$1.5 V$	$1.5 V$
Loading Capacitance	$500 pF$	$500 pF$
Input Offset Voltage	$277 \mu V$	$275 \mu V$
DC Gain	$107.7 dB$	$107 dB$
Gain-bandwidth Product	$1.65 MHz$	$1.71 MHz$
Phase Margin	87.4°	86.6°
CMRR @ DC	$48.35 dB$	$48.4 dB$
Positive(Negative) Slew Rate	$0.56(-0.57) V/\mu s$	$0.58(-0.61) V/\mu s$
Positive(Negative) Settling time at 1%	$931.1(905.54) ns$	$942.3(972.3) ns$

Table: COMPARISON SCHEMATIC VS LAYOUT

Comparison between results of Paper and Layout

PARAMETER	PAPER	LAYOUT
Technology	$0.35\ \mu m$ CMOS	$0.6\ \mu m$ CMOS
Area	$0.075\ mm^2$	$0.057\ mm^2$
Power supply	$1.5\ V$	$1.5\ V$
Loading Capacitance	$500\ pF$	$500\ pF$
Input Offset Voltage	$2.3\ mV$	$275\ \mu V$
DC Gain	$113\ dB$	$107\ dB$
Gain-bandwidth Product	$1.4\ MHz$	$1.71\ MHz$
Phase Margin	75°	86.6°
CMRR @ DC	$78\ dB$	$48.4\ dB$
Positive(Negative) Slew Rate	$2.2(-1.8)\ V/\mu s$	$0.58(-0.61)\ V/\mu s$
Positive(Negative) Settling time at 1%	$810(740)\ ns$	$942.3(972.3)\ ns$
HD2/HD3 @ $100kHz, 400mVpp$	$-54.25/ - 60.36\ dB$	$-36.8/ - 36\ dB$
HD2/HD3 @ $100kHz, 500mVpp$	$-48.20/ - 56.71\ dB$	$-28.5/ - 29.3\ dB$

Table: COMPARISON OTA PERFORMANCE PARAMETERS.