# SA 21.2: A Multistage Amplifier Topology with Nested Gm-C Compensation for Low-Voltage Application

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To design an operational amplifier for low-voltage applications, cascoding is no longer a suitable technique for achieving high dc gain. Instead, multiple cascaded stages must be used, with each stage a simple (noncascode) inverting or noninverting amplifier. In designing a multistage opamp with multiple feedback loops, special care must be taken to ensure stability [1, 2]. A well-known compensation technique is nested Miller compensation (NMC) [3]. The complexity of the transfer function of the NMC based multistage amplifiers is reflected on its stability conditions. This makes it difficult to devise a systematic design procedure that yields stable NMC-based amplifiers. A topology using nested transconductance ($G_m$)-capacitance compensation (NGCC) has a simple transfer function that yields simple stability conditions. These conditions can be exploited to simplify design.

Figure 1 depicts an n-stage NGCC amplifier topology consisting of n nested modules. In general, the i[th] module consists of a transconductor $G_{mi}$, module i + 1, a feed-forward transconductor $G_{mfi}$ and a compensation capacitor $C_i$. The dc voltage gain of the amplifier shown in Figure 1 is determined by the gain of the n+1 cascaded stages ($G_{m1}$, $G_{m2}$, ...., $G_{mn}$, $G_{mn+1}$). The feed-forward transconductance $G_{mfi}$ bypasses all stages from i +1 to n at high frequencies, when the gain of these stages drops. This extends the bandwidth of the overall amplifier.

Assume that the transconductance and the output conductance of the i[th] amplifier $G_{mi}$ are $g_{mi}$ and $g_{oi}$ respectively, and that the transconductance of $G_{mfi}$ is $g_{mfi}$. By making $g_{mi} = g_{mfi}$, the NGCC based amplifier, in Figure 1, has the transfer function:

$$\frac{V_o(s)}{V_i(s)} = \frac{-A_0}{\left(1+A_0 s/f_1\right)\left(1+s/f_2+s^2/(f_2f_3)+\ldots+s^{n-1}/\left(\prod_{i=2}^{n} fi\right)\right)} \tag{1}$$

$$where \quad A_o = \prod_{j=1}^{n} k_j, \qquad f_i = \frac{g_{mi}}{C_{mi}} \ \ and \ \ k_i = \frac{g_{mi}}{g_{oi}}$$

The regularity and modularity of the NGCC topology allows writing the transfer function for a general n-stage amplifier by inspection (Figure 1).

It is possible to find the values of the cut-off frequencies $f_1$, $f_2$, ..., $f_n$ based on the desired gain bandwidth, phase margin, settling time and power consumption. Once the cutoff frequencies are determined, the transconductance and the compensation capacitance of each stage can be determined.

The stability conditions of the NGCC-based topology can be derived by applying the Routh stability criterion on the unity-gain closed-loop transfer function. It can be shown that a four-stage NGCC amplifier must satisfy the following stability condition:

$$f_4 > f_2 \frac{1}{(1-f_1/f_3)} \tag{2}$$

The simplicity of the above stability conditions can be traced to the simplicity of the transfer function of (1). In contrast, the stability conditions of the multistage NMC amplifiers are complex. It is, therefore, much easier to design stable multistage NGCC amplifiers. The effect of the $G_m$ feed-forward on the stability is demonstrated by comparing the root loci of the NMC and NGCC topologies.

The bandwidth of a four-stage NGCC amplifier is compared with that of an NMC amplifier of similar complexity, assuming that the frequency is normalized with respect to the gain bandwidth (GB). It can be demonstrated that

$$\frac{f_4}{GB} = \frac{f'_4}{GB'} - \frac{f'_2 + f'_3}{GB'} \tag{3}$$

where GB and $f_4$ (GB′ and $f'_4$) are the gain-bandwidth product of the overall amplifier and the cut off frequency of the last stage of NGCC (NMC) amplifier, respectively. This implies that $f_4$/GB< $f'_4$/GB′. If both amplifiers are compared for the same power (i.e. $f_4 = f'_4$), the GB of the NGCC is greater than that of the NMC.

The extra $G_m$ feed-forward stages distinguish the NGCC topology from the NMC topology. The area and power overhead due to the $G_m$ feed-forward stages, in the NGCC architecture, can be reduced significantly by proper implementation of these stages. Figure 2 depicts the transistor level realization of the basic module of the NGCC amplifier. The $G_{m1}$ block is realized using the non-inverting stage $M_{11}$-$M_{14}$. The second stage, $G_{m2}$, is made up of the inverting stage $M_{21}$ and $M_{22}$. The simplest way to realize the feed-forward stage $G_{mf1}$ is to use a single MOS transistor ($M_{f1}$), driven by the input and connected to the output node. To ensure that $g_{m1} = g_{mf1}$, the transistor $M_{f1}$ is the same size as $M_{11}$ and their layouts are closely matched. This implementation ensures that both silicon area and power consumption of the NGCC amplifier will not be greater than that of the NMC amplifier. The same approach can be extended to construct multistage amplifiers, such as the four-stage NGCC amplifier shown in Figure 3.

The four-stage NGCC amplifier shown in Figure 3 is fabricated through MOSIS using a 2.0μm digital CMOS process. A ±1.0V supply voltage is used. The opamp tested was loaded with a 20pF capacitor in parallel with a 10kΩ resistor. Figure 4 shows the frequency response of the opamp. The opamp is configured as a unity gain follower to measure the response to a 100kHz, 100mV step input shown in Figure 5. Table 1 summarizes the opamp performance for two different cases of unity gain frequencies.

*References:*

[1] Pernici, S., G. Nicollini, R. Castello, "A CMOS Low-Distortion Fully Differential Power Amplifier with Double Nested Miller Compensation," IEEE Journal of Solid-State Circuits, vol. 28, no. 7, pp. 758-763, July, 1993.

[2] Op't Eynde, F., et al., "A CMOS Large-Swing Low-Distortion Three-Stage Class AB Power Amplifier," IEEE Journal of Solid-State Circuits, vol. 25, no. 1, pp. 265-273, Jan., 1990.

[3] Eschauzier, R., J. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*, Kluwer Academic Publishers, Boston, 1995.

**Figure 1: Conceptual NGGCC amplifier topology.**

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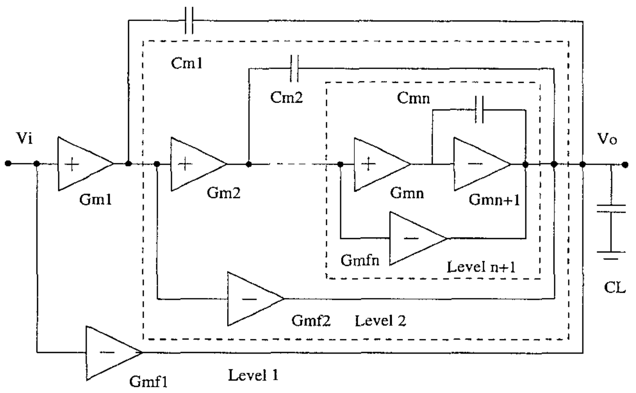


**Figure 1: Conceptual NGGCC amplifier topology.**

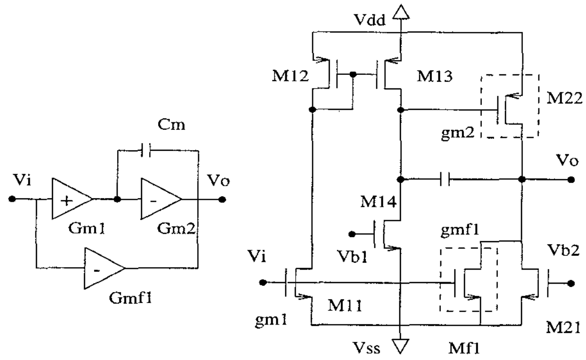


**Figure 2: Realization of an NGCC model.**

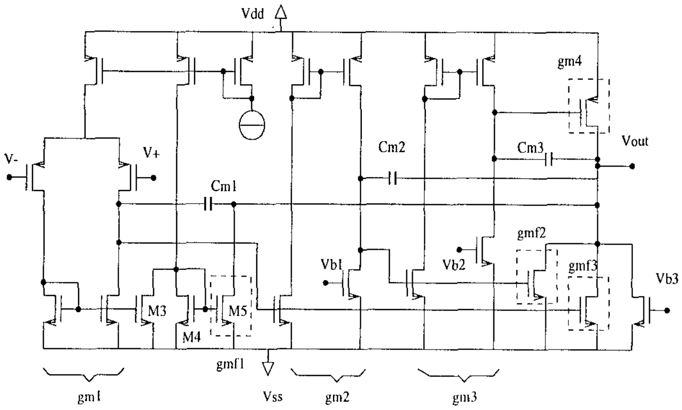


**Figure 3: A four-stage NGCC operational amplifier.**

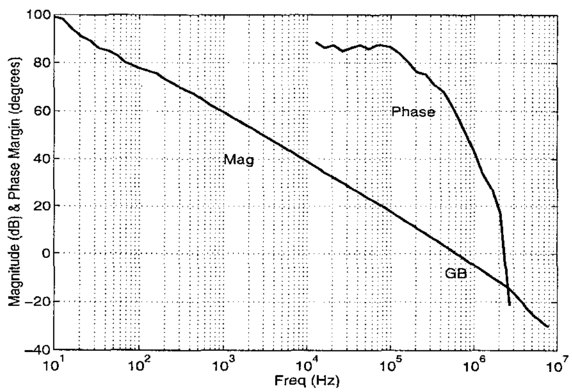


**Figure 4: Measured AC response of the NGCC opamp.**

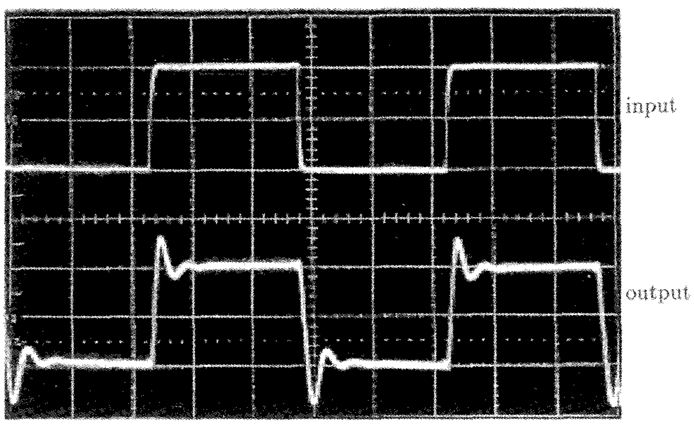


**Figure 5: Measured step response of NGCC opamp.**

| | | |
|---|---|---|
| Power consumption | 0.68mW | 1.4mW |
| dc gain | ≈100dB | ≈100dB |
| Gain bandwidth | 610kHz | 1.0MHz |
| Phase margin | 60° | 58° |
| Input offset | 5.2mV | 5.2mV |
| Slew rate | 2.5V/µs | 5.0Vµs |
| Power supply | ±1.0V | ±1.0V |
| Load condition | 10kΩ//20pF | 10kΩ//20pF |
| Area | 0.22mm² | 0.22mm² |

**Table 1: Measured performance of the 4-stage NGCC opamp.**

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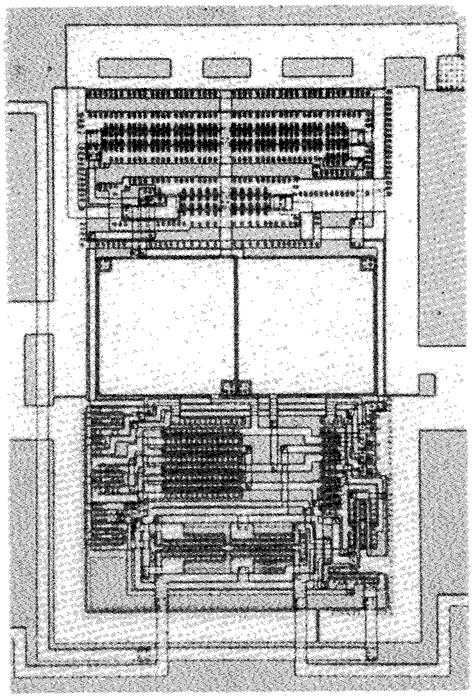

Figure 5a: Micrograph of compact opamp.

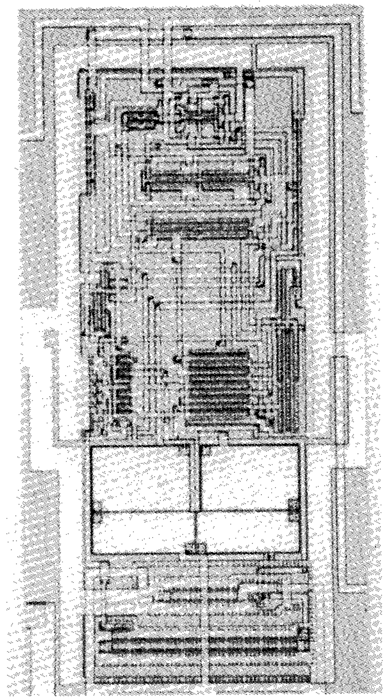

Figure 5b: Micrograph of compact rail-to-rail opamp.

## SA 21.3: A High-Performance Autozeroed CMOS Opamp with 50μV Offset

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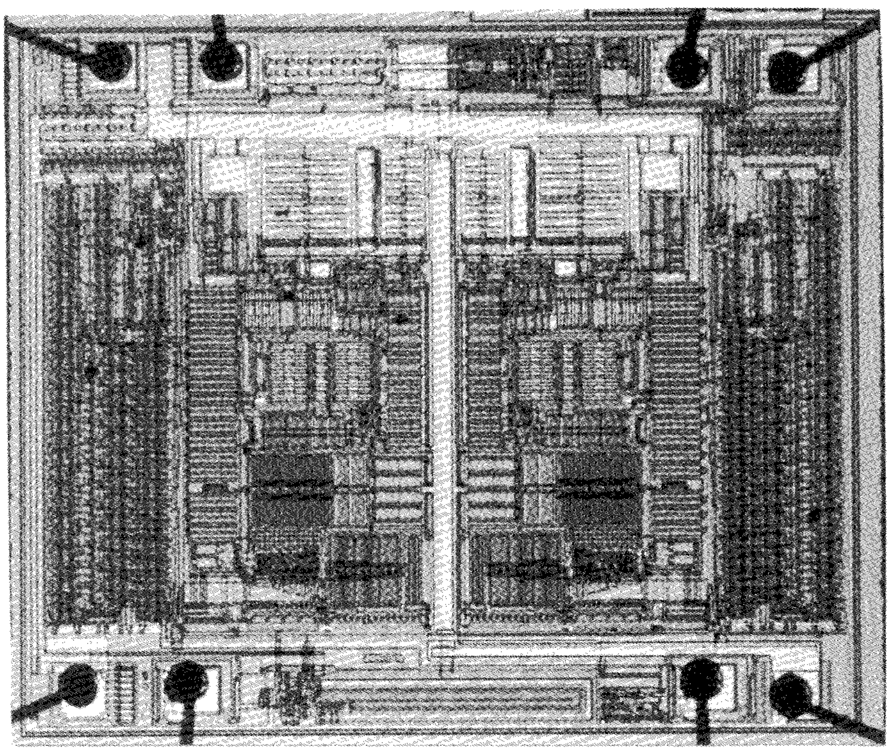

Figure 2: Die micrograph.