SIMULAZIONI

SCHEMATICO

(*) $V_{out} = 0 \Rightarrow V_{in,p} \cong 276\,\mu V$ (INPUT OFFSET VOLTAGE) [CLOSED LOOP CONFIG. — INPUT DC SWEEP @ $V_{out}=0$]

- DC SWEEP $\Rightarrow V_{in,m} = V_{in,p}$ (or V_{b2})
  ① ADE / DC / component parameter / select component [$V_{in,p}$] / sweep [-1,5, +1,5] / step [0,5m], output [V_{out}]
  ② Prima V_{b2}, poi $V_{in,p}$. Trovo $\begin{cases} V_{b2} = -748\,mV \\ V_{in,p} = 525\,mV \end{cases}$
  Inoltre (*)
- AC OPEN LOOP $\Rightarrow$ AC / [1, 15M] / 15 points
  DC gain = 107,7 dB
  pole (@ 104,7 dB) = 6,3 Hz
  PM = 180° − 92,6° = 87,4° (@ f_T = 1,49 MHz)
- AC CLOSED LOOP $\Rightarrow$ GBW = 1,65 MHz
  PM (closed loop) = 131° ?
- STEP RESPONSE $\Rightarrow$ Period = 6 µs, $t_{RISE} = t_{FALL} = 500\,ns$
  $SR^+ = 956\ V/\mu s$
  RISE TIME [10 % ÷ 90 %] = 578,4 ns (−160 mV ÷ +160 mV)
  SETTLING TIME$^+$ (1 %) = 931 ns (198 mV)
  $SR^- = -957\ V/\mu s$
  FALL TIME = 569 ns
  SETTL. TIME$^-$ = 905,5 ns (−198 mV)
- CMRR $\Rightarrow$ open loop, AC1 sta in $V_{in,p}$ / $V_{in,m}$ $\Rightarrow A_d = 107,7$ dB
  $A_c = 59,35$ dB $\Rightarrow$ CMRR = 48,35 dB
- CMR $\Rightarrow$ closed loop, DC sweep (V_{in-p})
  $CMR^+ = 1,21V$
  $CMR^- = -1,47V$
  $\Rightarrow$ CMR = 2,68 V
- PSRR $\Rightarrow$ AC1 in V_{DD} ($PSRR^+$) e V_{SS} ($PSRR^-$) $\Rightarrow$ OPEN LOOP

Continua...

V_{DD} [Ac_1] $\Rightarrow$ $A_{ps^+} = 59,6$ dB $\Rightarrow$ $PSRR^+ = 48,1$ dB

V_{SS} [Ac_1] $\Rightarrow$ $A_{ps^-} = 67,3$ dB $\Rightarrow$ $PSRR^- = 40,6$ dB

- Total bias current $\Rightarrow$ 6,8 mA ? 6,77 mA nel layout!

LAYOUT