BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI

I Semester 2018-2019

CS F342 Computer Architecture

Lab Exam

Date: 18/11/2018 TIME: 90 Minutes MM: 33

INSTRUCTIONS: (i) Create a folder on desktop, rename it to your IDNO. (ii) Rename the project with your IDNO (iii) Write your IDNO and name in .v file. Write all modules in a single .v file. Put this .v file in the folder you created on desktop.

On command prompt type and run the following command to set the path:

set path=%PATH%;C:\iverilog\bin;C:\iverilog\gtkwave\bin

Q. A digital circuit is to be designed with the following specifications: At power on the circuit is in some initial state T0 and remains in that state till a START signal is received. Upon receiving the start signal a 4-bit counter, A, and a Flipflop G are initialized to zero and the circuit goes to next state T1. In this state an external input X is checked on every clock edge and if found to be '1' then the counter is incremented by 1 at the same clock edge and the circuit goes to T2. If X is zero, then the counter is not incremented and circuit remains in T1. In T2 the counter output is checked for maximum value (1111) (Assume that a signal 'Z' if equal to 1 indicates that the counter has reached maximum value). If the output of counter if found to be '1111' then G is set to 1 in the same clock cycle and the operation stops. If the counter value is not '1111' then depending on value of X the operation continues.

The Block diagram and the ASM chart of the circuit is shown below in **Fig1.** and **Fig 2.**

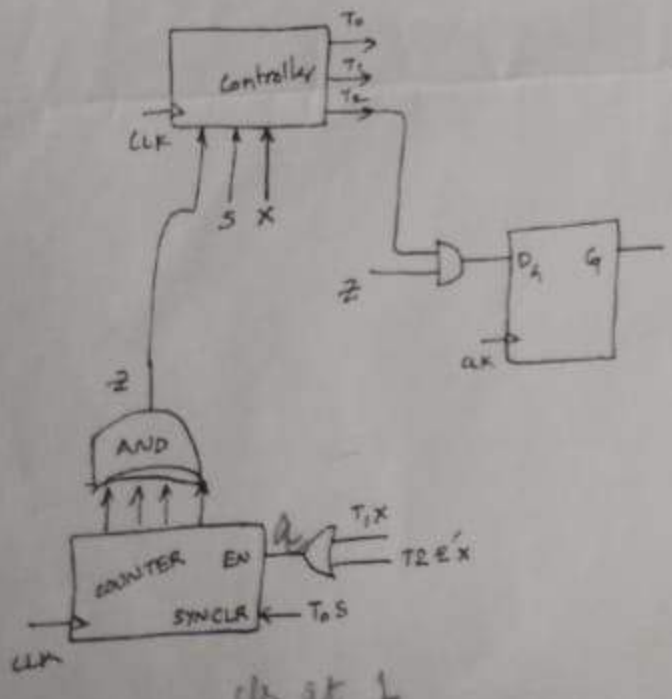


Fig 1.

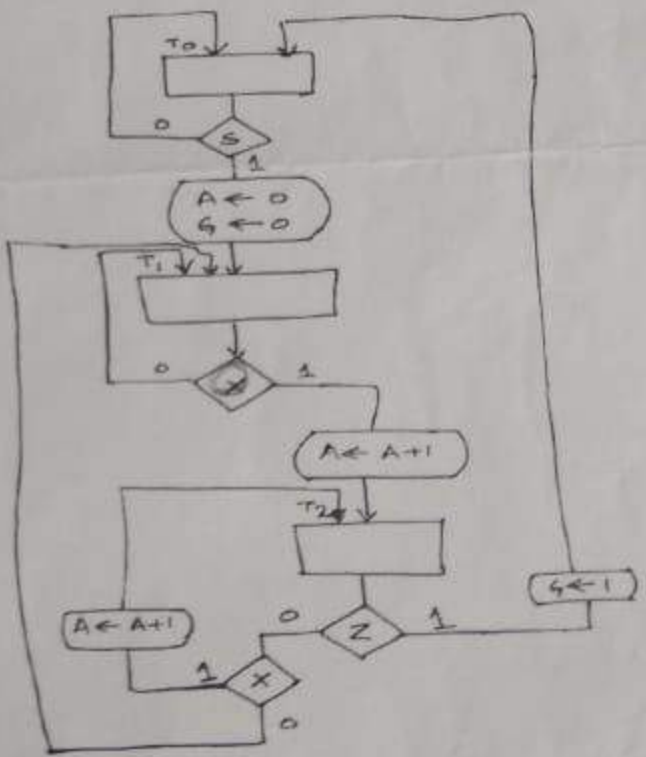


Fig 2.

The control logic circuit is shown in **Fig3** below.

PTO

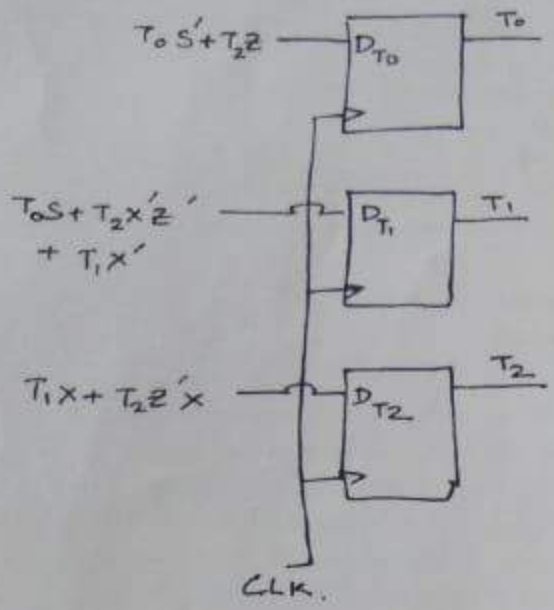
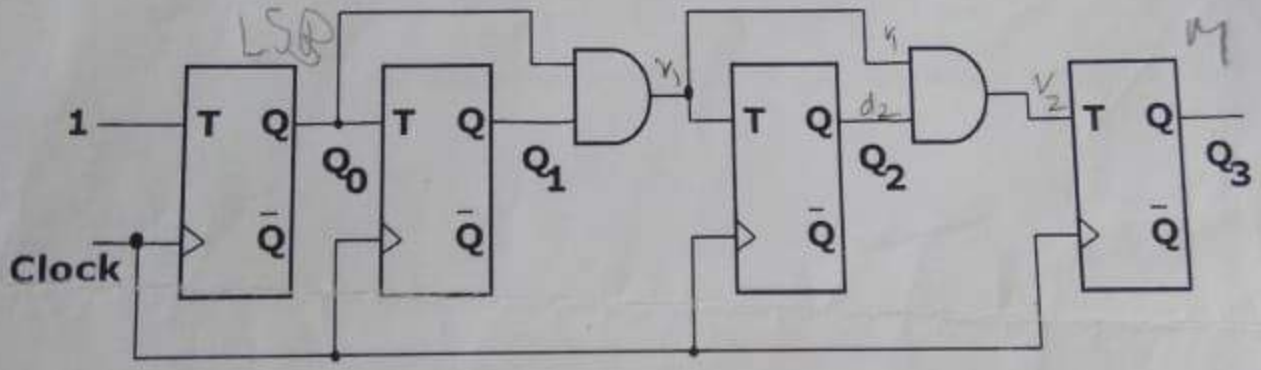


Fig 3



4-bit synchronous up counter

Fig.4

Implement the circuit in different modules stated as follows:

(1) **ControlLogic:** This module takes as input S, Z, X and CLK and outputs three states T0, T1 and T2. The circuit diagram for the control logic is given above in **Fig3**. Implement the circuit using **gate level modeling**. Also write sub modules for d-ff () . d_ff() can be implemented in behavioral modeling.

(2) **TFF:** This module implements the functionality of a T-Flip flop with a synchronous clear. Implement this module using behavioral modeling.

(3) **COUNTER_4BIT:** This module implements the functionality of a 4-bit synchronous binary UP counter with a synchronous clear. Implement this module as shown in Fig4. above. Use TFF modules for your implementation.

(4) **INTG:** This module integrates the above modules as per the datapath shown above in **Fig 1**. The inputs to this module are S and CLK and outputs are counter values and G.

(5) **Testbench:** With S=1 and X=1 apply a clock of 1KHz and check the output of counter and G.