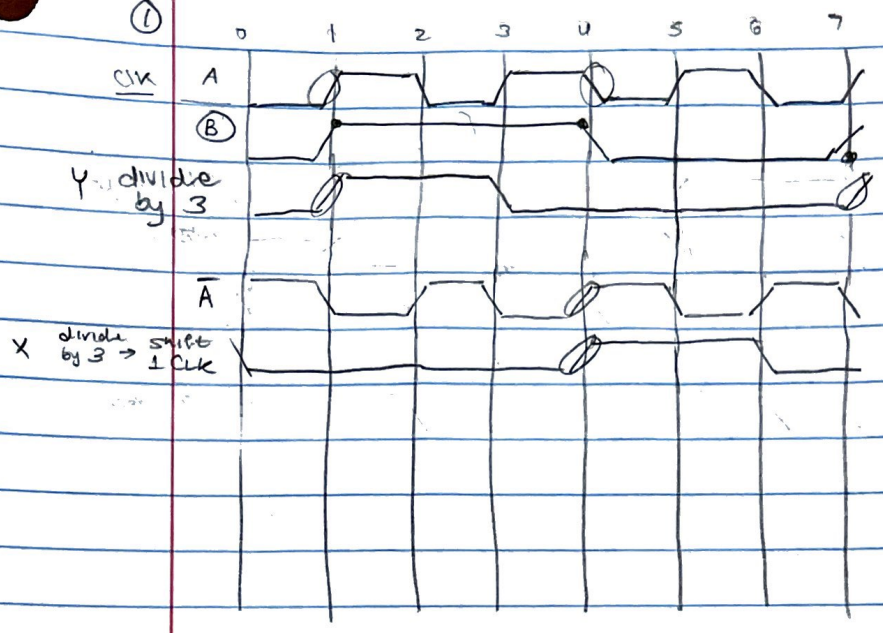
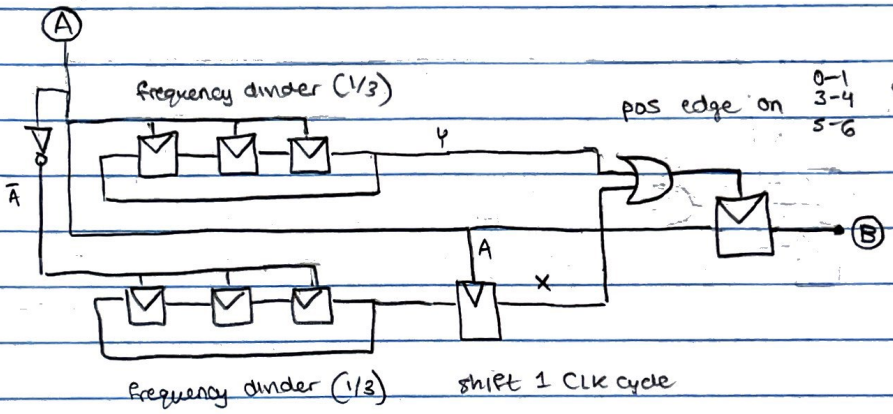
Gan Aher HW #4

①



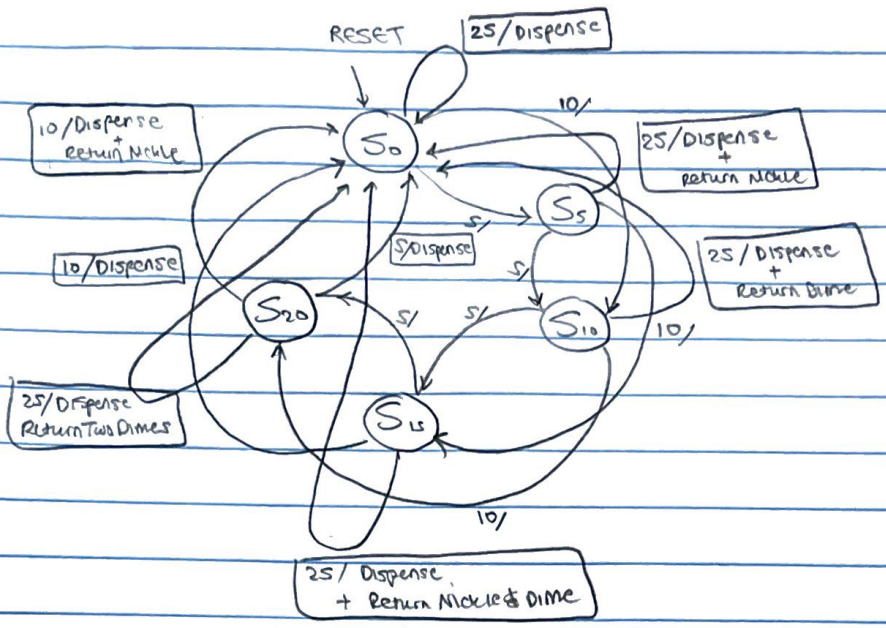
t	A	B	
0	0	0	*
1	1	1	
2	0	1	
3	1	1	
4	0	0	
5	1	0	
6	0	0	*
7	1	1	

frequency divider (divide by 3)



(b)

FSM



TRUTH TABLE

State	X	State+		
S_0	5	S_5		
S_5	5	S_{10}		
S_{10}	5	S_{15}		
S_{15}	5	S_{20}		
S_{20}	5	S_0	Dispense	
S_0	10	S_{10}		
S_5	10	S_{15}		
S_{10}	10	S_{20}		
S_{15}	10	S_0	Dispense	
S_{20}	10	S_0	Dispense	Return Nickle
S_0	25	S_0	Dispense	
S_5	25	S_0	Dispense	Return Nickle
S_{10}	25	S_0	Dispense	Return Dime
S_{15}	25	S_0	Dispense	Return Nickle Dime
S_{20}	25	S_0	Dispense	Return Two Dimes

a b c (State)	x y (Signal)	Dispense	Return
0 0 0	0 1	0	0 0 0
0 0 1	0 1	0	0 0 0
0 1 0	0 1	0	0 0 0
0 1 1	0 1	0	0 0 0
1 0 0	0 1	1	0 0 0
0 0 0	1 0	0	0 0 0
0 0 1	1 0	0	0 0 0
0 1 0	1 0	0	0 0 0
0 1 1	1 0	1	0 0 0
1 0 0	1 0	1	0 0 1
0 0 0	1 1	1	0 0 0
0 0 1	1 1	1	0 0 1
0 1 0	1 1	1	0 1 0
0 1 1	1 1	1	0 1 1
1 0 0	1 1	1	1 0 0

OR of ANDs

$\bar{a}\,\bar{b}\,\bar{c}\,x\,y$

$\bar{a}\,b\,c\,x\,\bar{y}$

$a\,\bar{b}\,\bar{c}\,x\,\bar{y}$

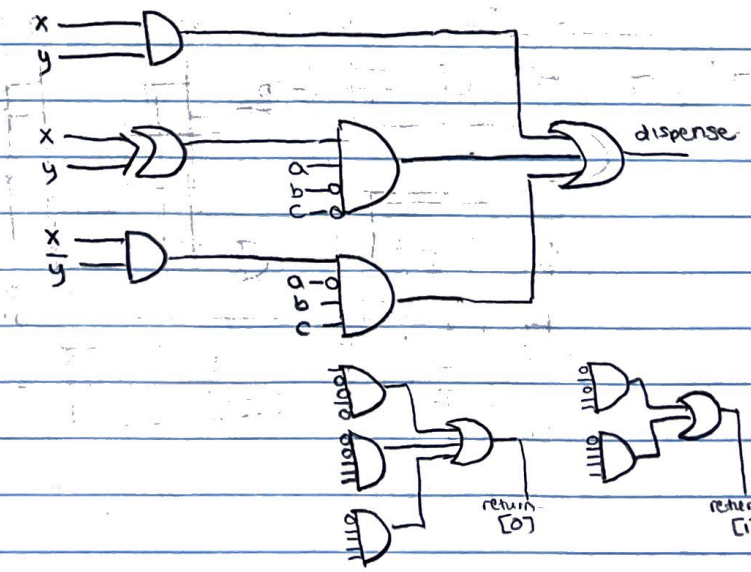
$\bar{a}\,\bar{b}\,\bar{c}\,x\,y$

$\bar{a}\,\bar{b}\,c\,x\,y$

$\bar{a}\,b\,\bar{c}\,x\,y$

$\bar{a}\,b\,c\,x\,y$

$a\,\bar{b}\,\bar{c}\,x\,y$



(c)

$e^{-\frac{t}{\tau}}$ t seconds $\tau = 20$ seconds

a.)

$0.99 = e^{-t/20} \rightarrow \ln(0.99) = -t/20$

$\rightarrow -20 \ln(0.99) = t = \boxed{0.201 \text{ sec}}$

b.)

$P = e^{-(3.60)/20}$

$\boxed{P = 1.23 \times 10^{-4}}$

(2) Combination Logic Review + HDL Practice ALU

- mux32.sv
- add32.sv
- testbench
- Makefile
- README

AND OR XOR MUX2
NAND NOR NOT

ADD32 from diagram on (pg 240) (32-bit CLA adder)

submodules
- 4-bit CLA block (×8)
  - ↳ 4-bit ripple carry adder
    - ↳ 1-bit ripple carry adder (×4)
  - ↳ generate-propagate logic

MUX32 from diagram on (pg 83) (Wider Multiplexers)

32:1 multiplexer needs $\log_2 32$ select lines $= 5$

S_0 S_1 S_2 S_3 S_4

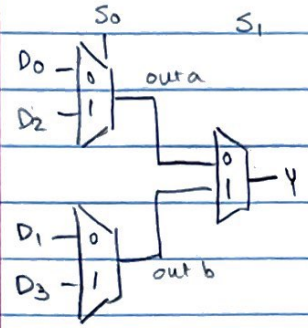
32 data 16 data 8 data 4 data 2 data

16 [2:1] 8 [2:1] 4 [2:1] 2 [2:1] 1 [2:1]

2 [16:1] 2 [8:1] 2 [4:1]

submodules
- 4:1 $\log_2 4 = 2$
- 8:1 $\log_2 8 = 3$
- 16:1 $\log_2 16 = 4$
- 32:1 $\log_2 5 = 32$

4:1 mux



$\overline{D_0}$	$\overline{D_2}$	$\overline{D_1}$	$\overline{D_3}$	sel 0	sel 1	expected Y
1	1	0	0	0	0	1
1	1	0	0	0	1	0
1	1	0	0	1	0	1
1	1	0	0	1	1	0

D_0	D_1	D_2	D_3
1	0	1	0

8:1 mux

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7

16:1 mux

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Meta Data

Reading: did in previous weeks

written part: ~~7~~ hours (1a and 1b took a long time)

↑ I think I got it (2 hours) drawing FSM wasn't helpful

↑ probably did it very wrong (5 hours?)

↳ took a long time but I think I mostly understand it

Verilog part: 3 hours (pretty straightforward, just didn't understand always-comb vs. assign and verilog got mad)