Paper / Subject Code: 49374 / Digital Logic & Computer Architecture

1T01873 - S.E. Computer Science & Engineering (Artificial Intelligence & Machine Learning) (R-2019) SEMESTER - III / 49374 - Digital Logic & Computer Architecture QP CODE: 10014070 DATE:29/11/2022 (3 hours) Total Marks: 80

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N.B.		 Question No. 1 is compulsory Attempt any three questions from remaining five questions Assume suitable data if necessary and justify the assumptions Figures to the right indicate full marks 	
Q1	A	Convert i) 123 in to binary ii) (AB9) ₁₆ in to Decimal iii) (351) ₈ in to decimal iv) 129 in to BCD v) 64 in to gray code	05
01	В	Draw the single and double precision format for representing floating point number using IEEE 754 standards and explain the various fields	05
Ω1	C	Explain SR Flip Flop	05
	D	Differentiate between Hardwired control unit and Micro programmed control unit	05
Q2	A	Draw the flow chart of Booths algorithm for signed multiplication and Perform 5 x 2 using booths algorithm	10
	В	Explain the different addressing modes.	10
Q3	A	For 132.65 obtain the IEEE 754 standards of Single precision and Double precision format	10
	В	Explain Micro instruction format and write a microprogram for the instruction ADD R_1 , R_2	10
Q4	A	Consider a 4-way set associative mapped cache with block size 4 KB. The size of the main memory is 16 GB and there are 10 bits in the tag. Find-1. Size of cache memory 2. Tag directory size	10
	В	Explain Flynn's classification	10
Q5	A	Explain different types Distributed and Centralized bus arbitration methods	10
	В	Describe the detailed Von-Neumann Model with a neat block diagram	05
	C	Describe the characteristics of Memory.	05
Q6	*	Write Short notes on	20
377		a) Grey code, BCD, Excess-3 Code with example	
	0	b) Encoder and Decoder	
		c) Cache coherence	
		d) Instruction Pipelining	

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