Module 5-
Memory Organization

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Characteristics of Memory

- Location
- Capacity
- Unit of transfer
- Access method
- Performance
- Physical type
- Physical characteristics
- Organization

Characteristics of Memory

Location

- CPU
- Internal
- External

Capacity

- Word size
- Number of words

Unit of transfer

- Internal - Usually governed by data bus width
- External - Usually a block which is much larger than a w
- Addressable unit - Smallest location which can be unique addressed

Characteristics of Memory

Access method

Sequential
- Start at the beginning and read through in order
- Access time depends on location of data and previous locati
- e.g., tape

Direct
- Individual blocks have unique address
- Access is by jumping to vicinity plus sequential search
- Access time depends on location and previous location
- e.g., disk

Random
- Individual addresses identify locations exactly
- Access time is independent of location or previous access
- e.g., RAM

Associative
- Data is located by a comparison with contents of a portion c
- Access time is independent of location or previous access
- e.g., cache

Characteristics of Memory

Performance

Access time

- Time between presenting the address and getti
  valid data

Memory Cycle time

- Time may be required for the memory to “reco
  before next access
- Cycle time is access + recovery

Transfer Rate

- Rate at which data can be moved

Characteristics of Memory

Physical Types

Semiconductor - RAM
Magnetic - Disk & Tape
Optical - CD & DVD

Physical Characteristics

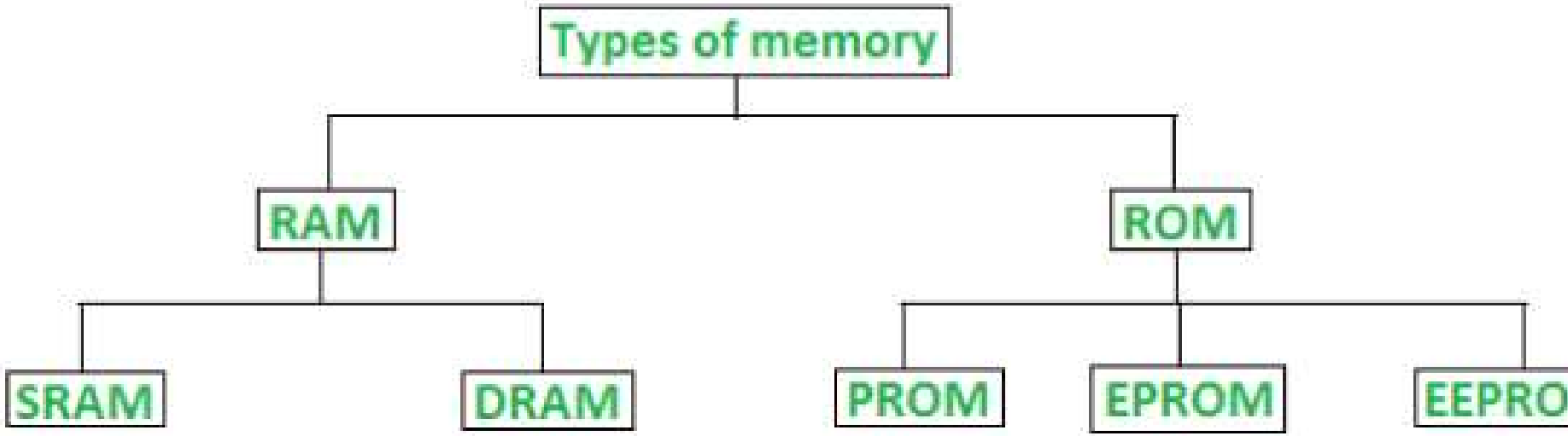
- Decay
- Volatility
- Erasable
- Power consumption

Characteristics of Memory

Organization

- Physical arrangement of bits into words
- Not always obvious
- e.g., interleaved

Types of RAM and ROM



Random Access Memory (RAM)

- The programs and data that the CPU requires during the execution of a program are sto
  this memory.
- It is a volatile memory as the data is lost when the power is turned off.
- Types
  1. Static RAM (SRAM)
     -It is a form of a semiconductor
     -It is widely used in microprocessors
     -SRAM comprised of flip flops

  2. Dynamic RAM (DRAM)
     -It is made of Capacitors and has smaller data life span than Static RAM.
     -DRAM changes its state from 0 to 1 over a period of time, due to the slow leaka
     charge from the capacitor.
     -To prevent this, DRAM requires an external memory refresh, which rewrites the
     the capacitors, restoring them to their original charge.

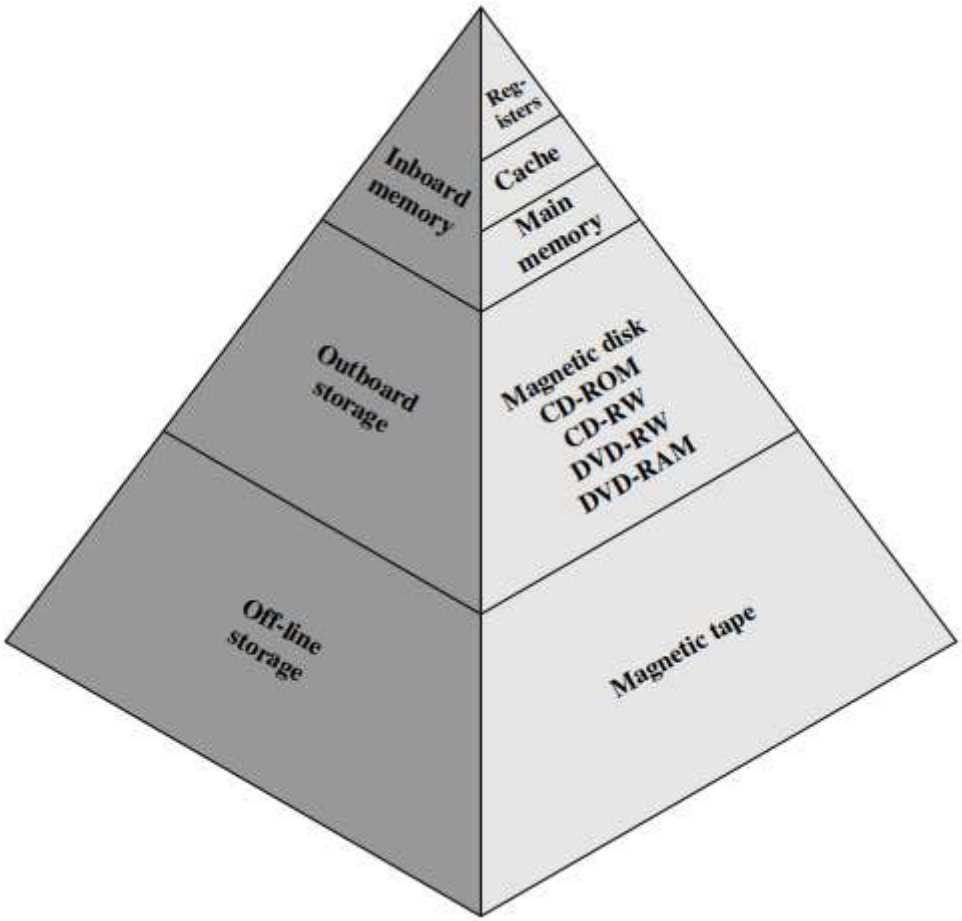
Read-Only Memory (ROM)

- It is used to permanently store data that does not need to be modified.
- ROM is non-volatile memory, which means that the data stored in it is retained even w
  power is turned off.
- Types
  1. PROM (Programmable read-only memory)
     -It can be programmed by the user.
     -Once programmed, the data and instructions in it cannot be changed.

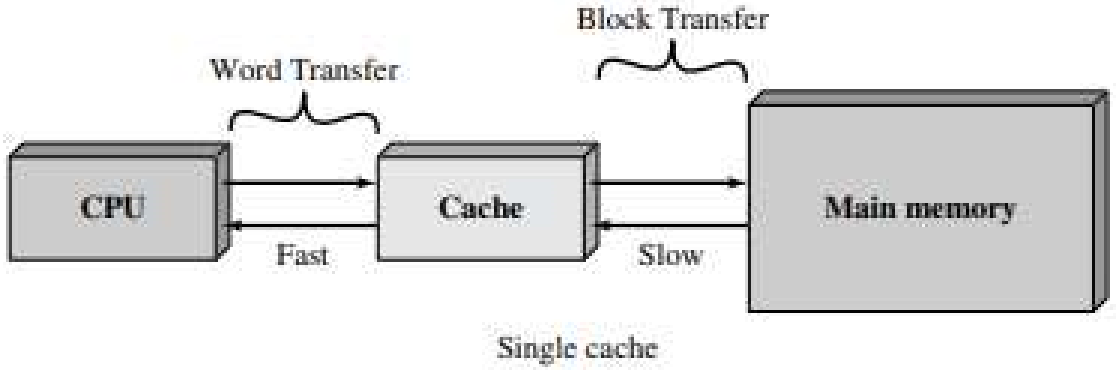
  2. EPROM (Erasable Programmable read-only memory)
     -It can be reprogrammed.
     -To erase data from it, expose it to ultraviolet light.

  3. EEPROM (Electrically erasable programmable read-only memory)
     -The data can be erased by applying an electric field, with no need for ultraviolet

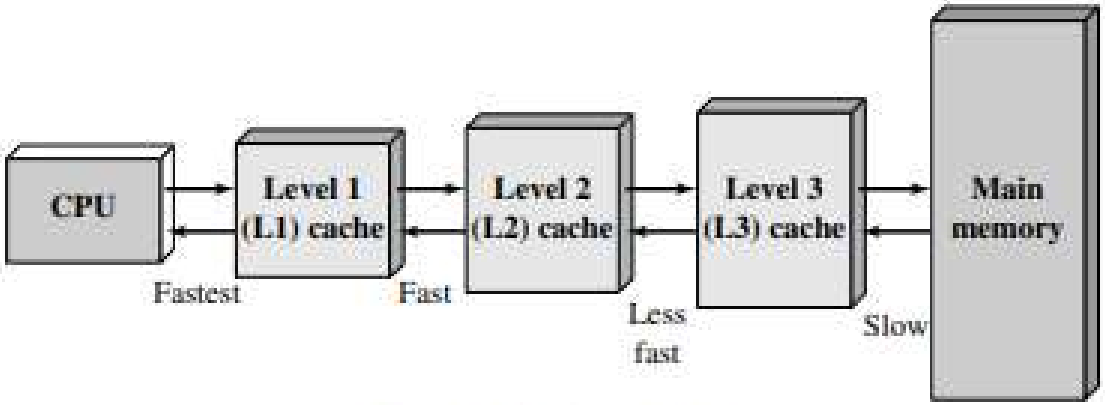
Memory Hierarchy



Cache Memory



Single cache



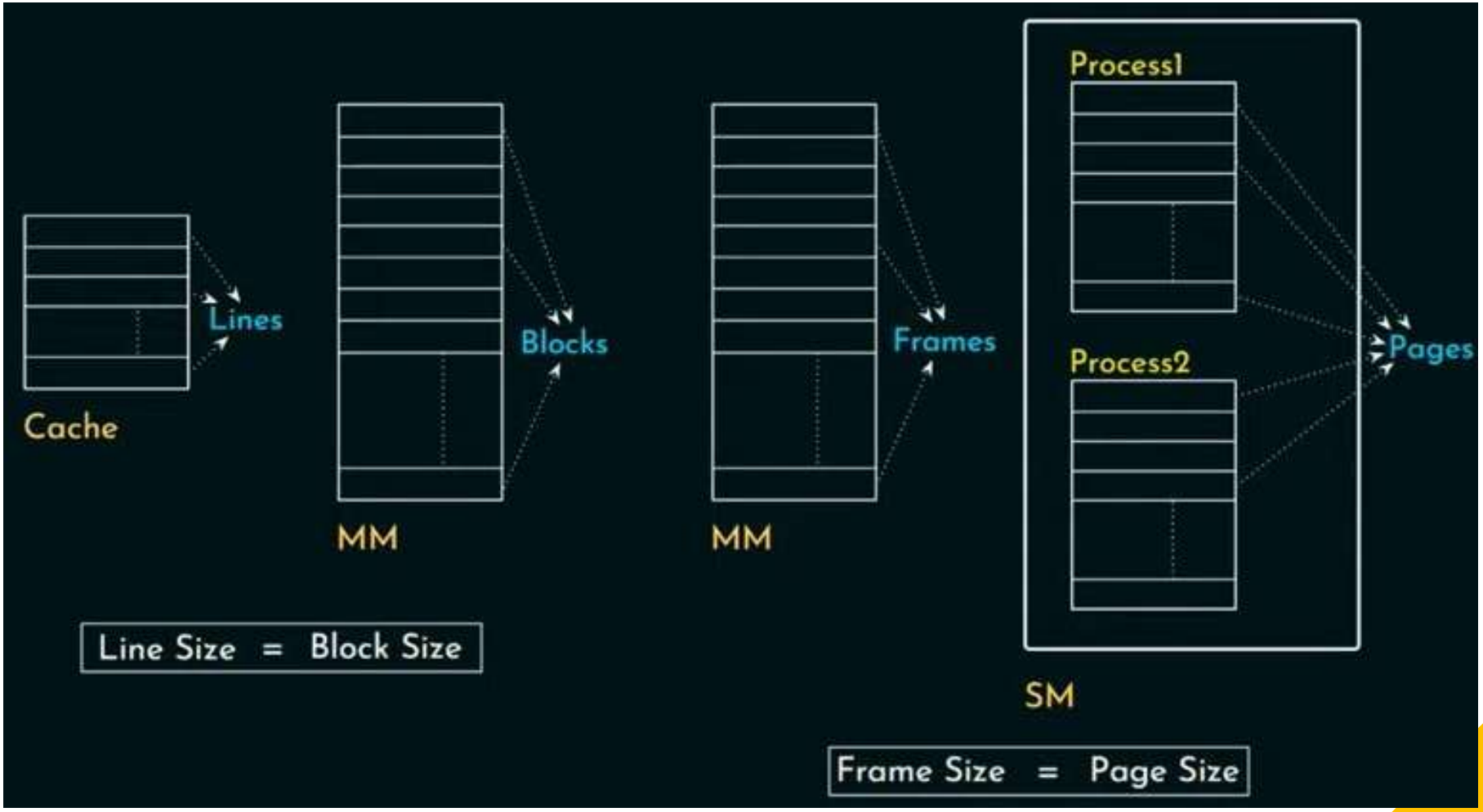
Three-level cache organization

Cache and Main Memory

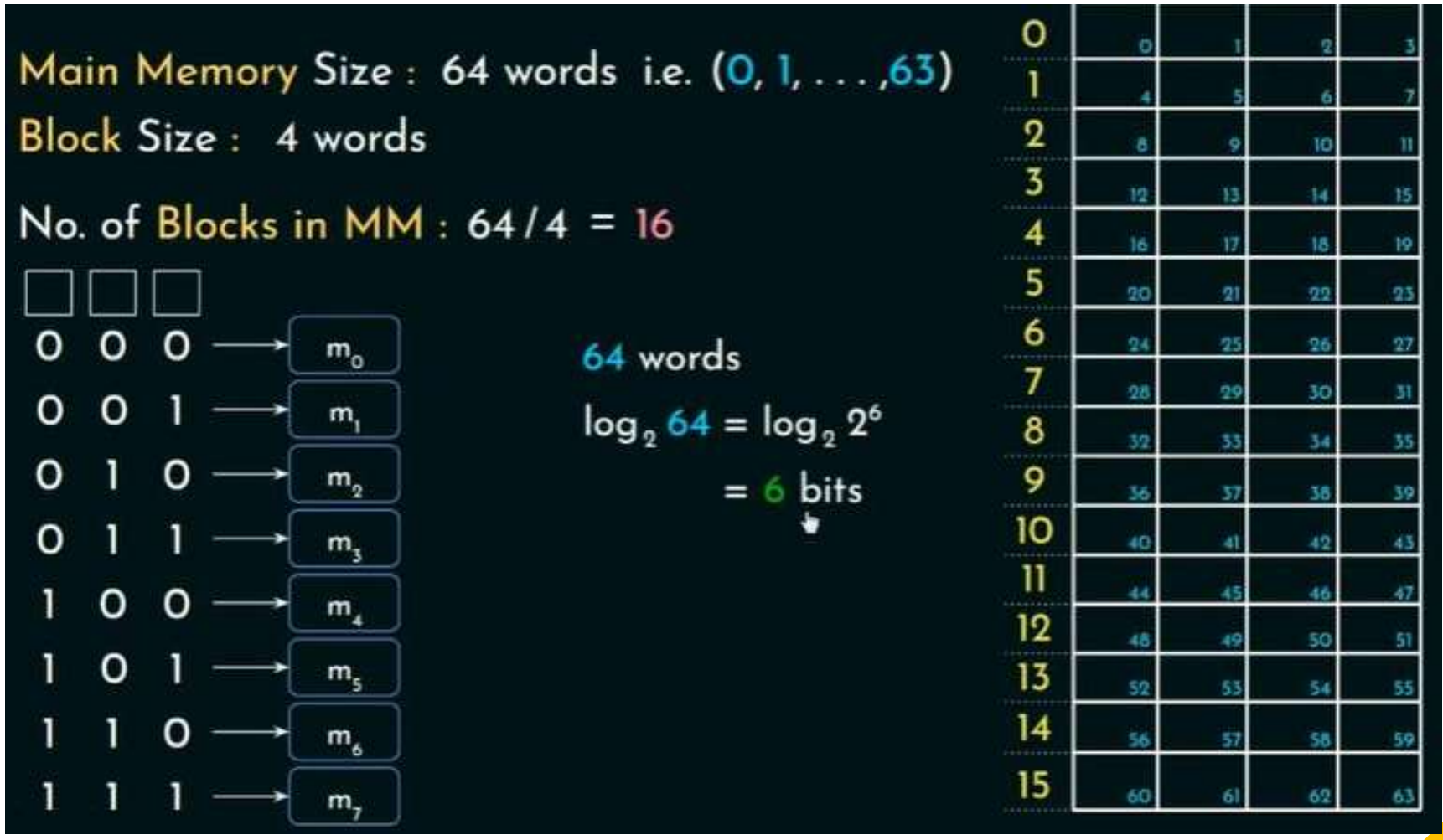
Cache Mapping Techniques

- Direct Mapping
- Associative Mapping
- Set-Associative Mapping

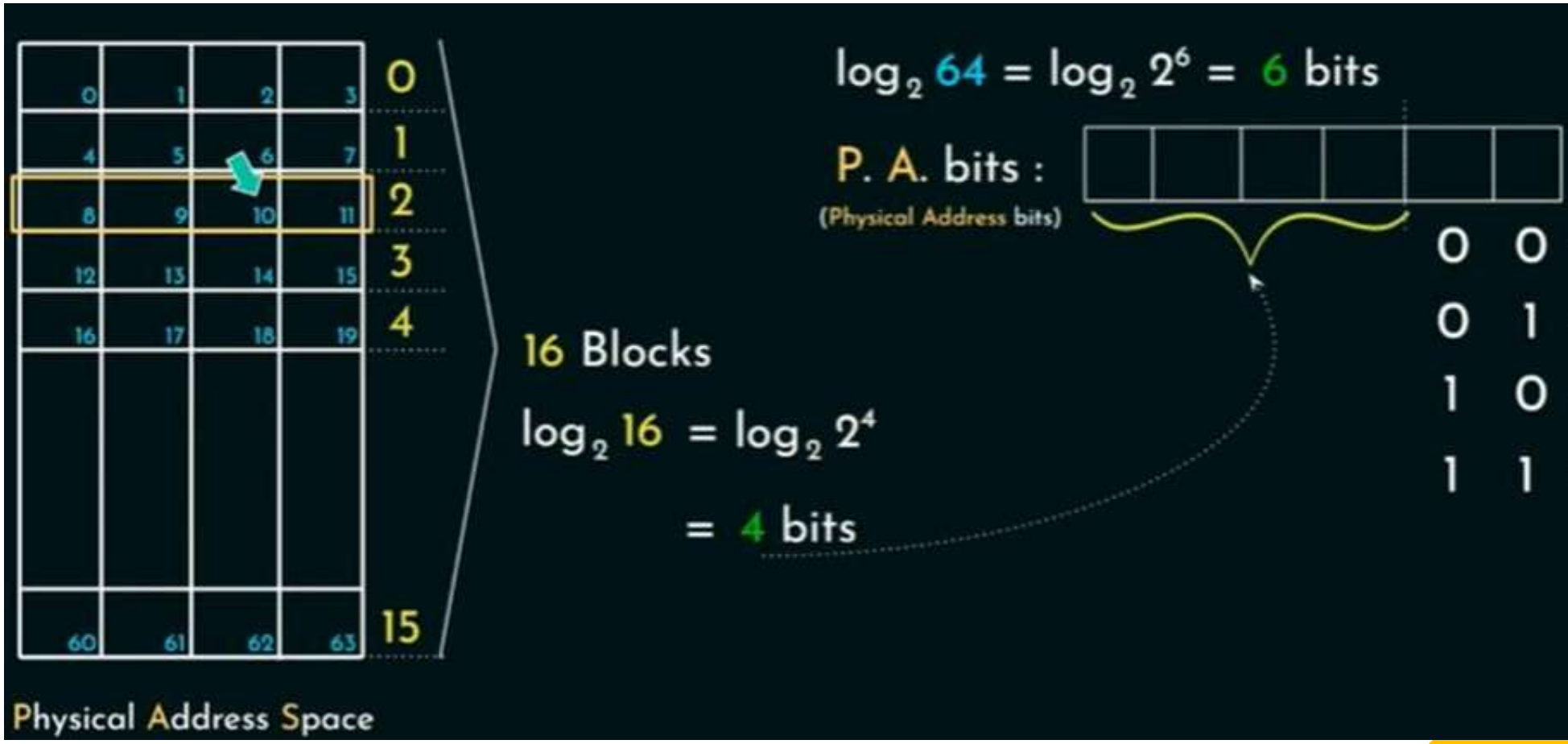
Cache Mapping



Direct Memory Mapping



Direct Memory Mapping



Direct Memory Mapping

Cache Size : 16 words

Block Size : 4 wo

Line Size : 4 words

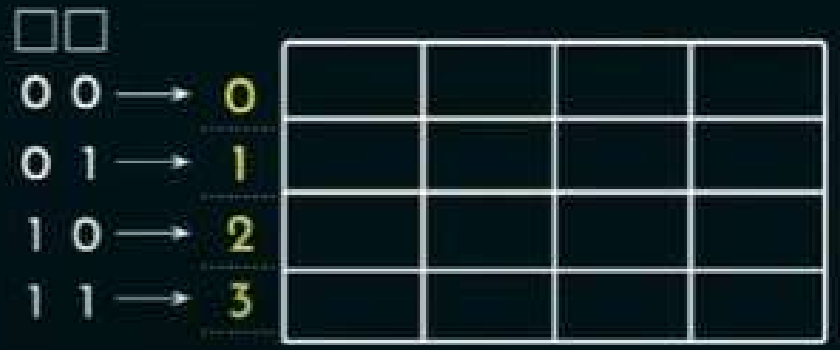
Block Size = Line

No. of Lines in Cache : 16 / 4 = 4 i.e. 0, 1, 2, 3

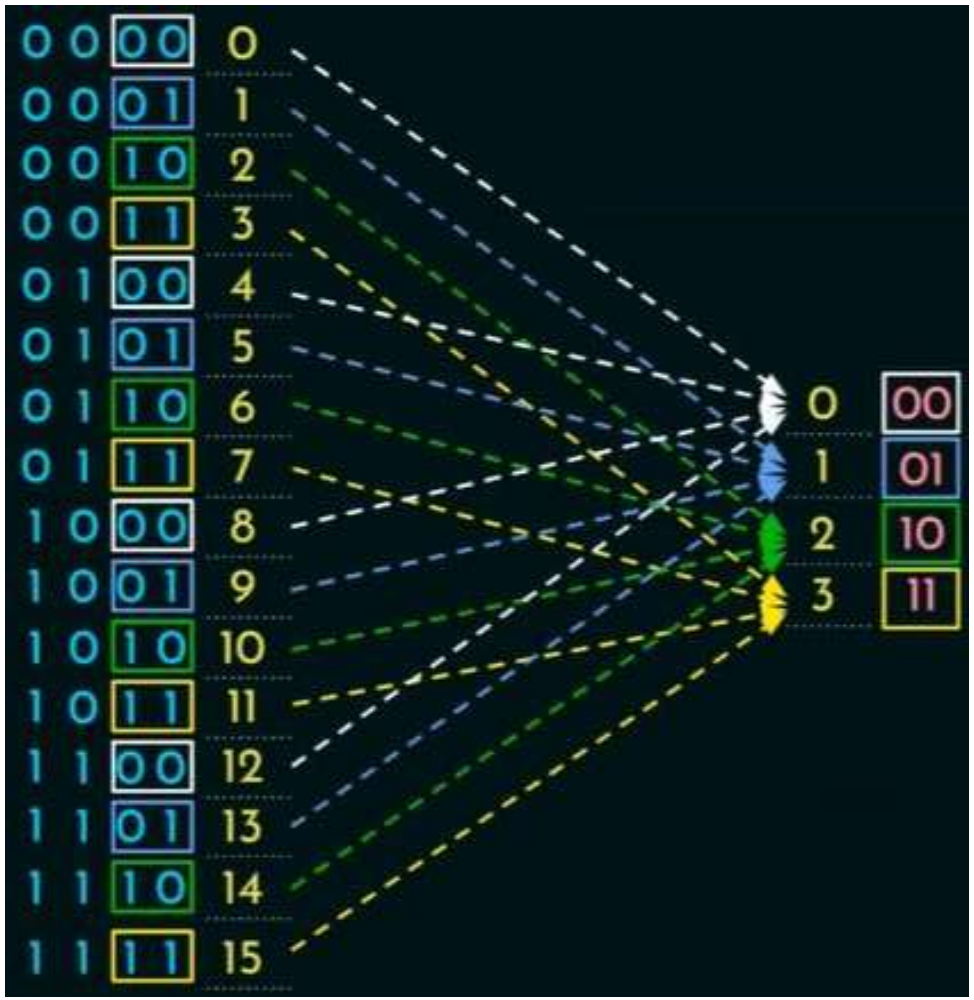
4 Lines

$\log_2 4 = \log_2 2^2$

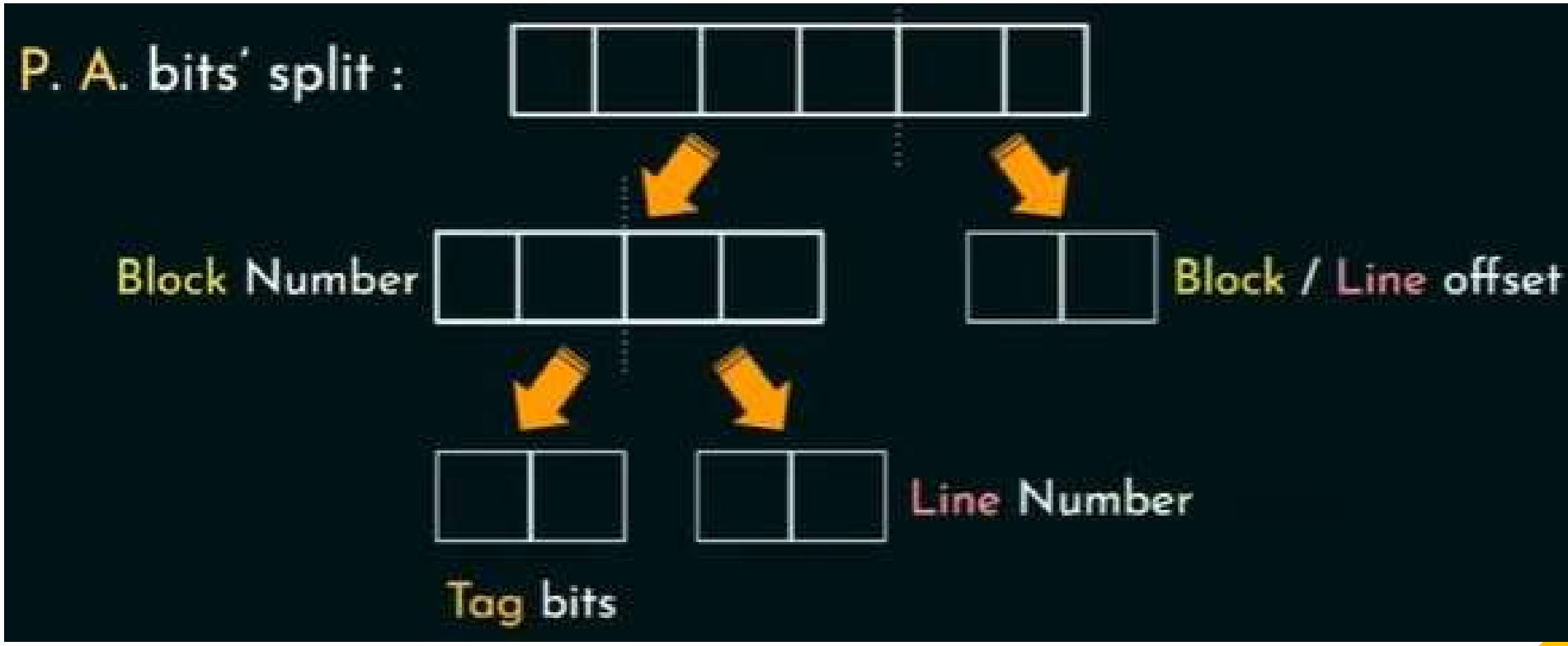
$= 2$ bits



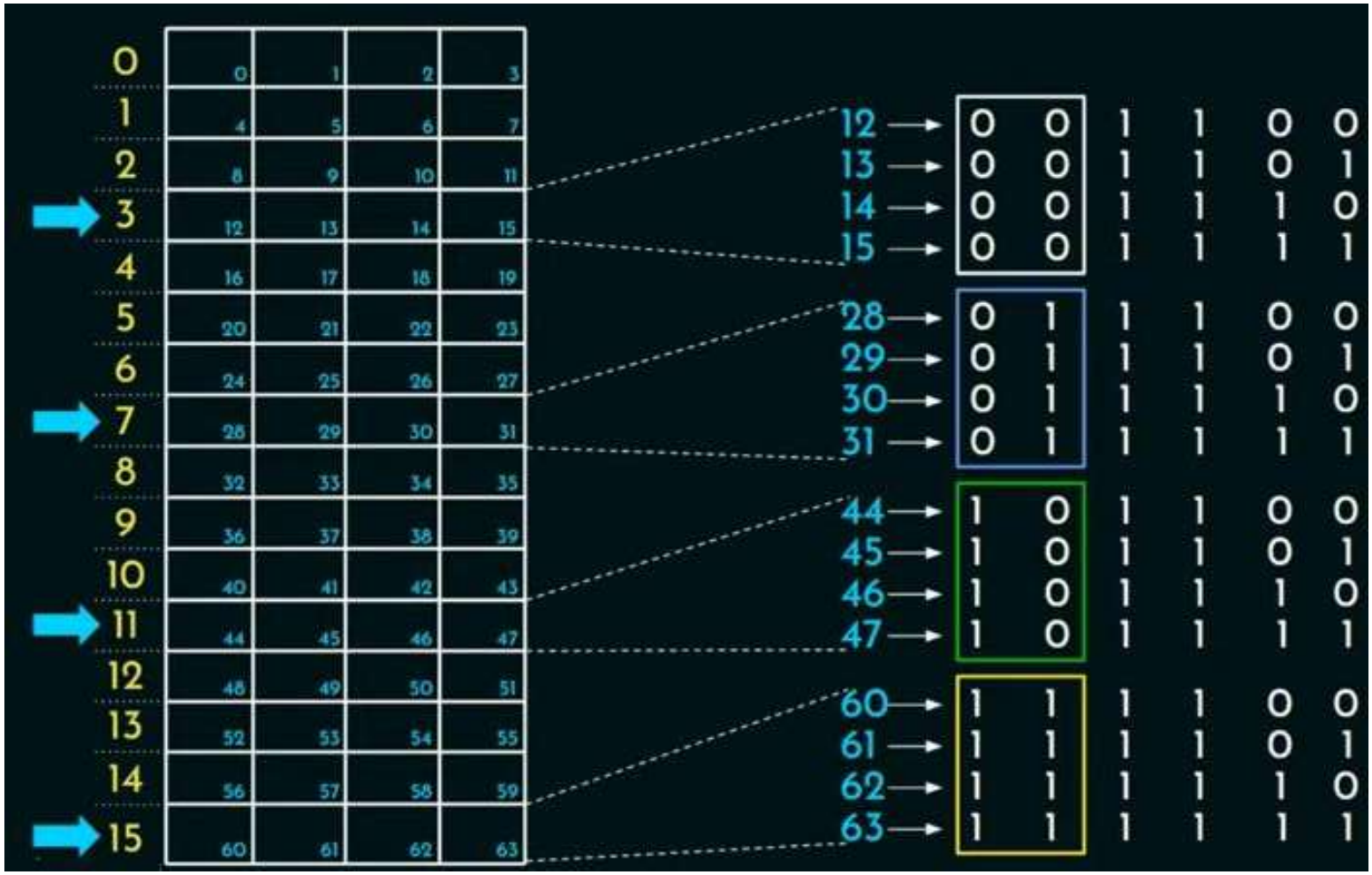
Direct Memory Mapping



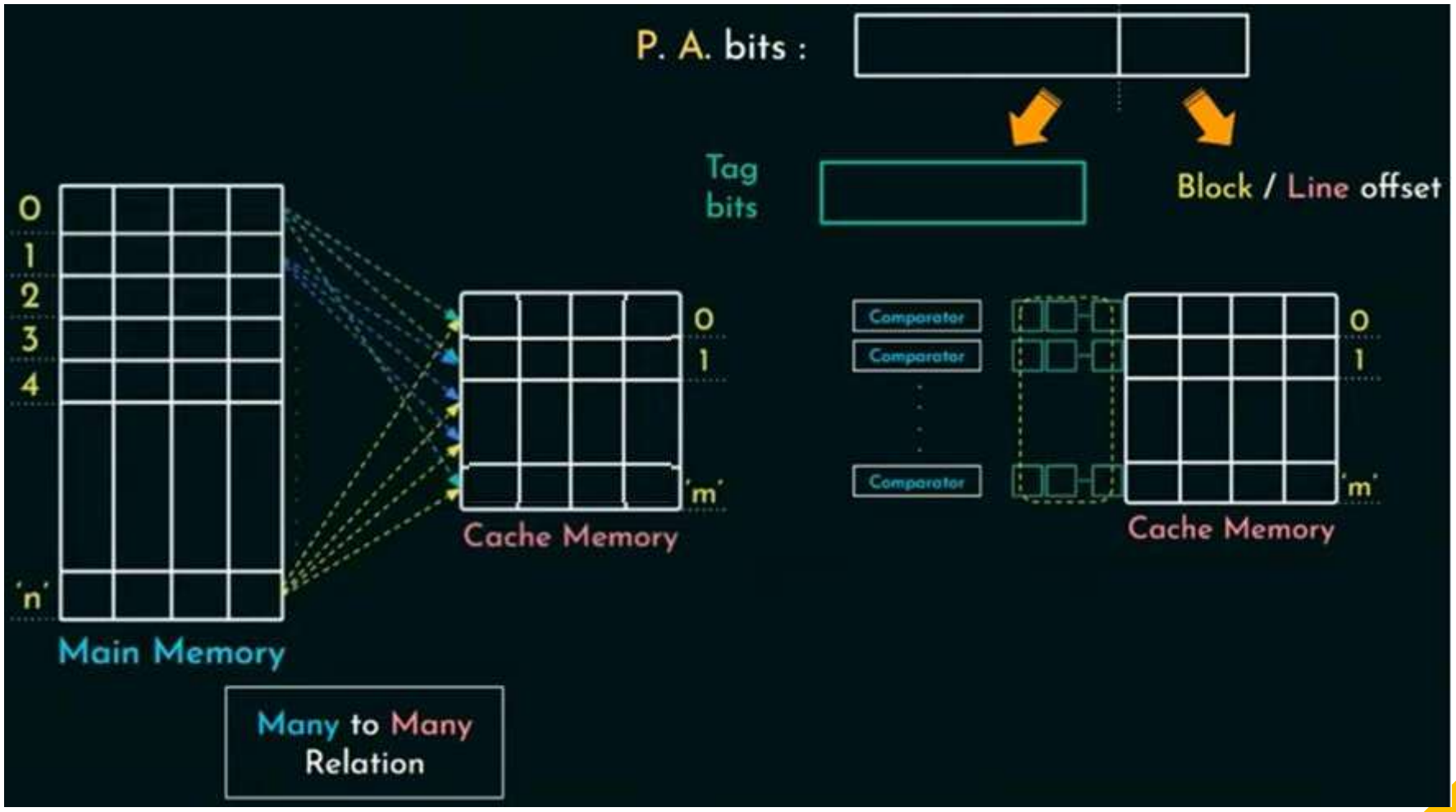
Direct Memory Mapping



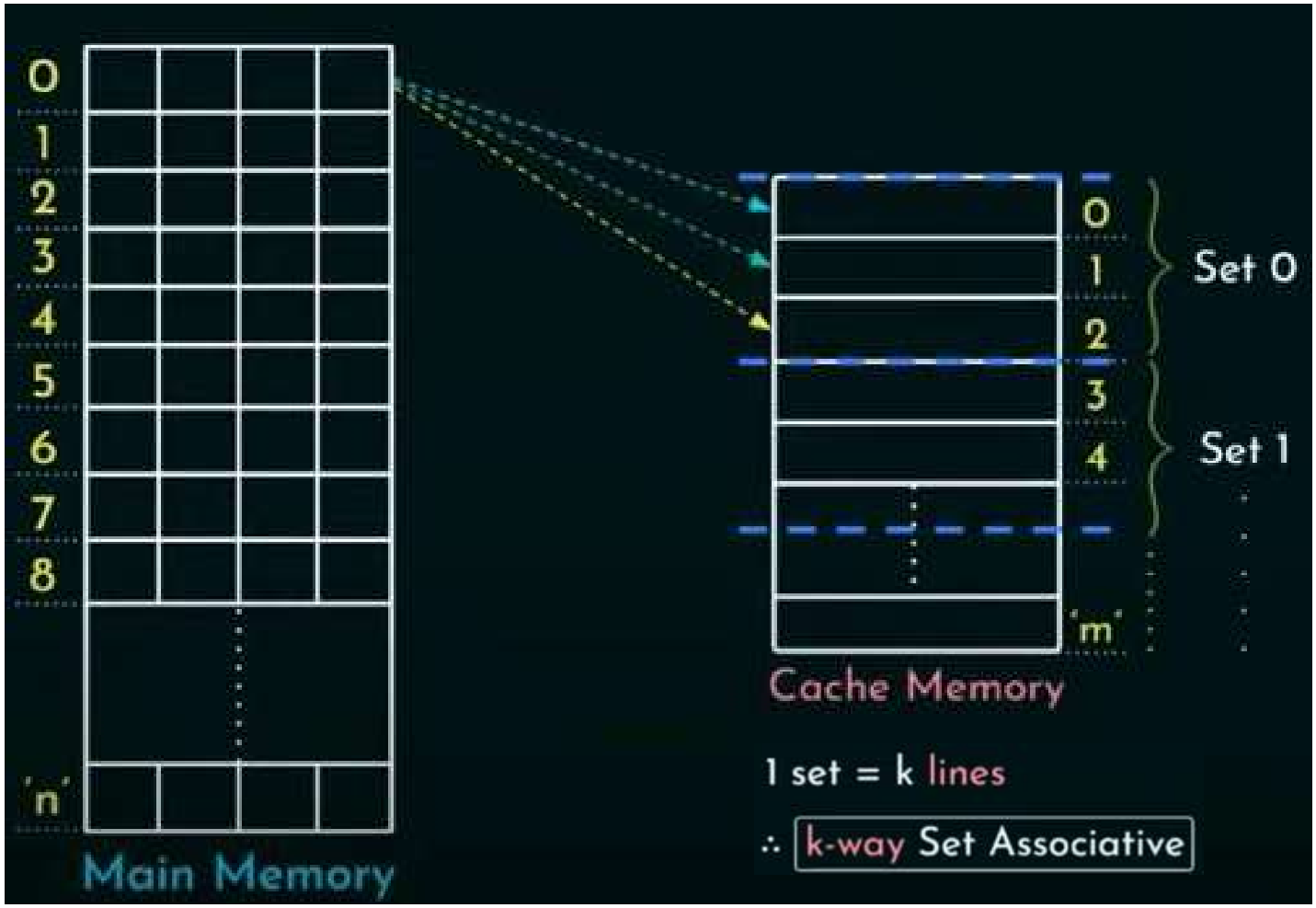
Direct Memory Mapping



Associative Mapping

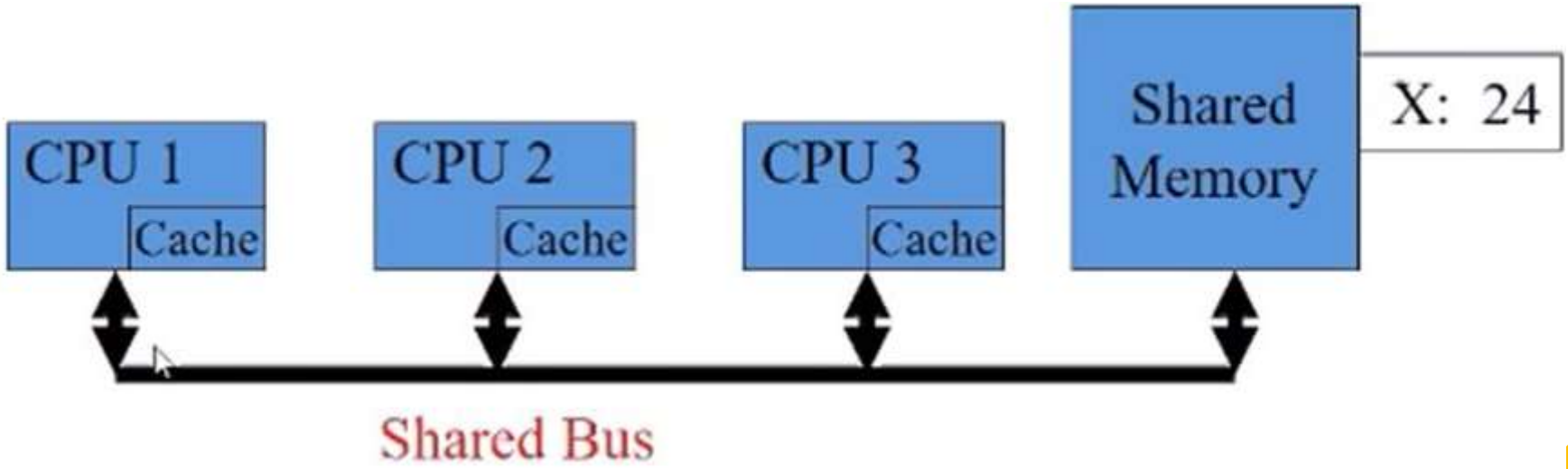


Set Associative Mapping



Cache coherence

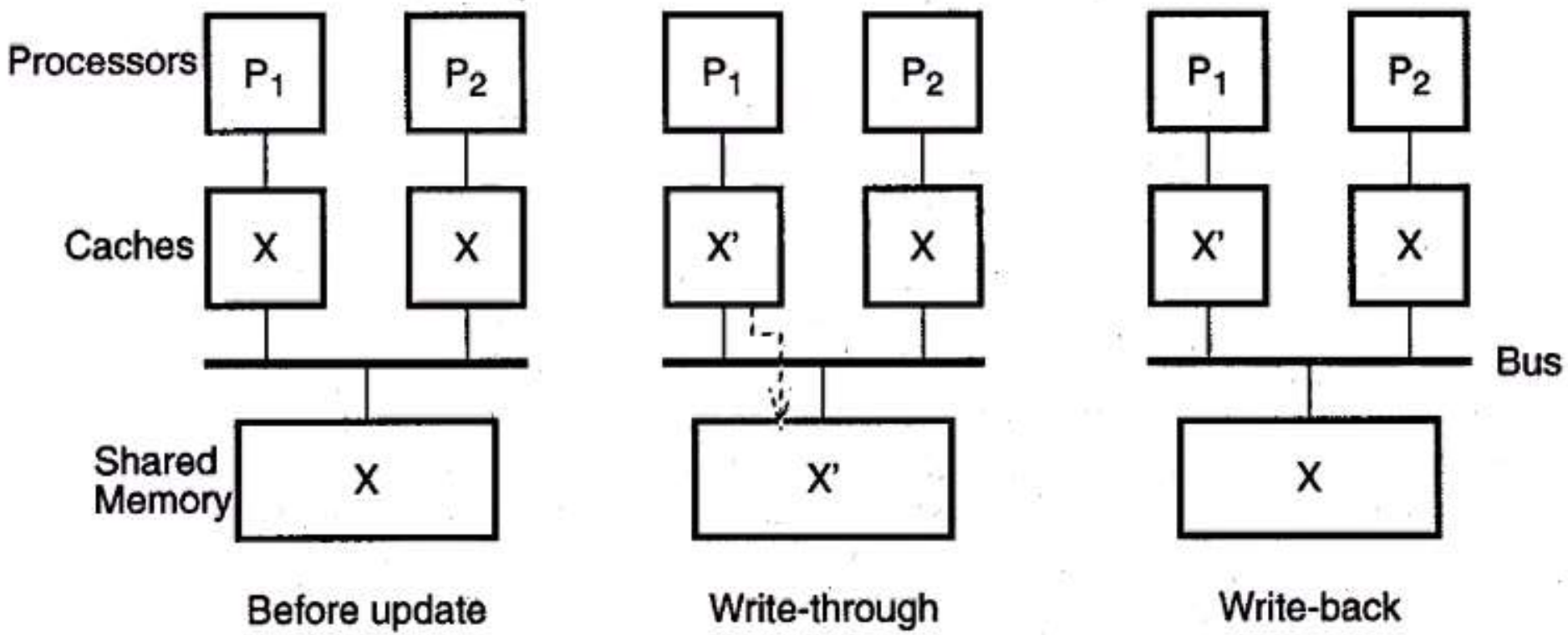
- Caches in multiprocessing environment introduce the cache coherence problem.
- In a shared memory multiprocessor with a separate cache memory for each processor, v
  multiple processors maintain locally cached copies of a unique-shared memory locatio
  local modification of the location can result in globally inconsistent view of memory.
- Cache coherence schemes prevent this problem by maintaining a uniform state for each
  cached block of data.



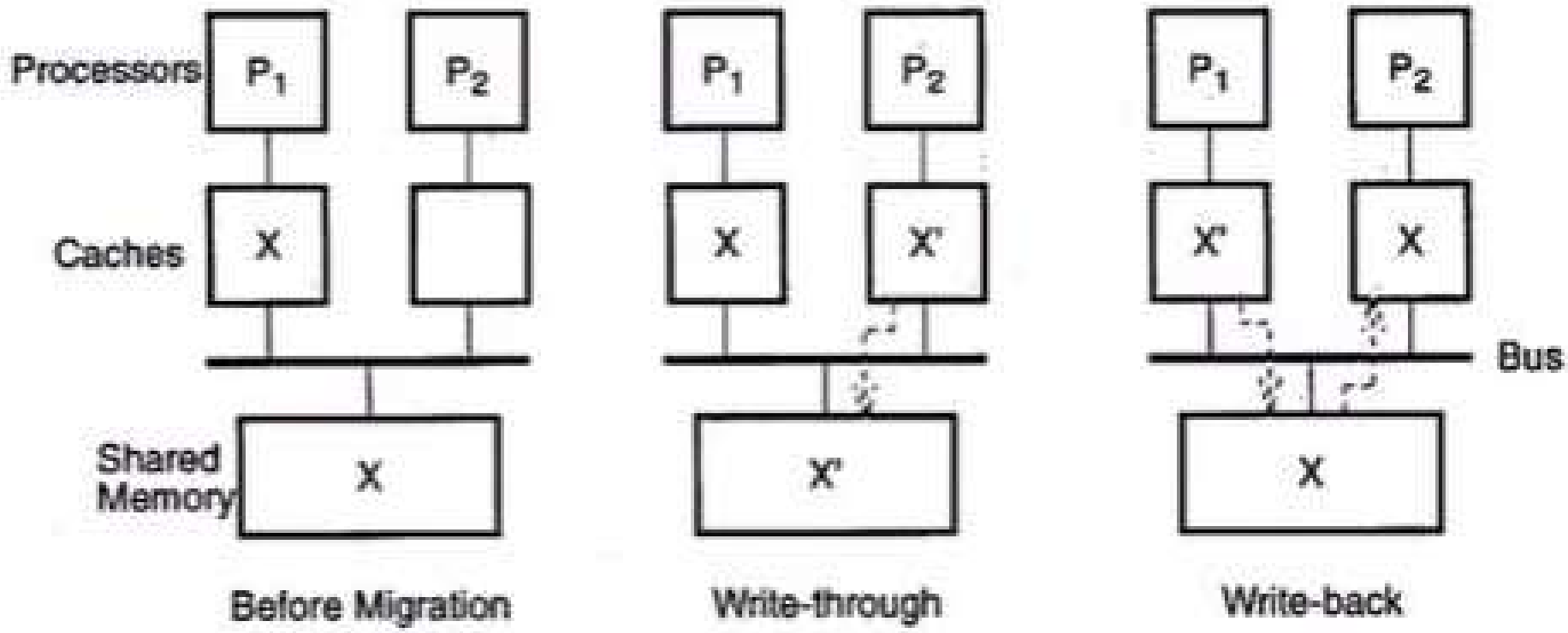
Causes of Cache inconsistency

- Sharing of writable data
- Process migration
- I/O activity

Inconsistency in Data sharing



Inconsistency after Process migration



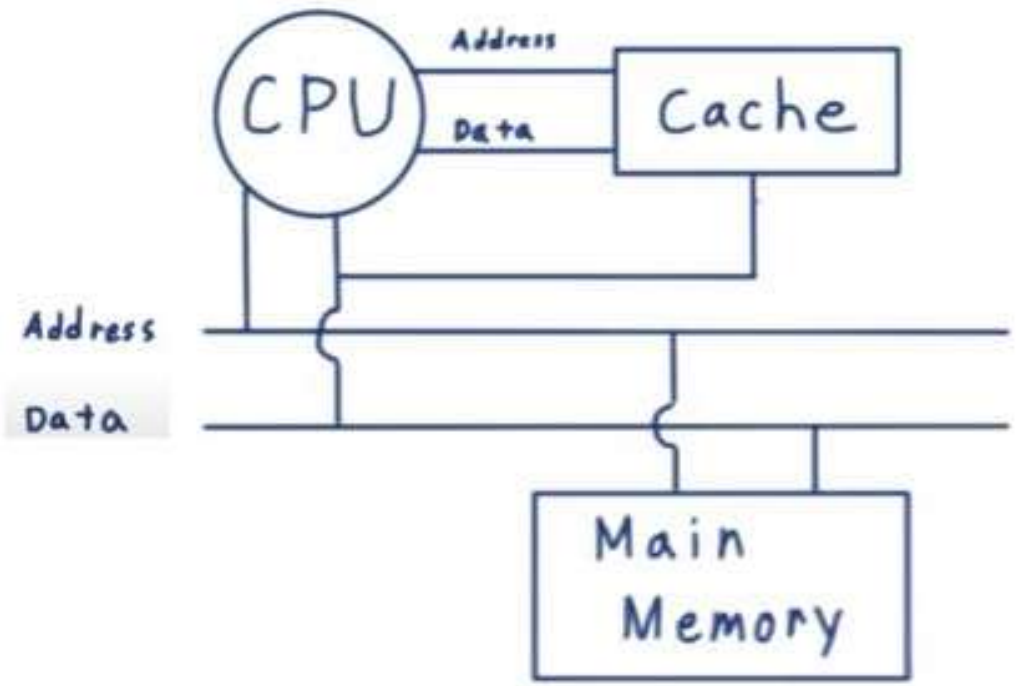
Write policies

Hit

- Write-through policy
- Write-back policy

Miss

- Write Allocate
- Write Around



Thank You