Robustness Analysis of 3-2 Adder Compressor Designed in 7-nm FinFET Technology

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***Abstract*—Adder compressors (ACs) have been employed for several prominent computing datapaths as multipliers, machine learning, discrete transforms, and filters. This brief investigates the robustness of the 3-2 AC against the process, voltage, and temperature (PVT) variability targeting a design for a predictive ASAP7 7nm FinFET technology. The variability impacts on the delay, power, and product-delay-power (PDP) of the 3-2 AC for both super- and near-threshold voltages operating regimes are herein evaluated. Our results demonstrate that process is the main concern among the variability issues for both operating regimes, presenting an even more alarming level of variability in near-threshold operation.**

***Index Terms*—Adder compressor, FinFET technology, PVT variability, reliability.**

I. Introduction

MULTI-OPERAND arithmetic operations are prominent alternatives for improving the design efficiency of parallel datapaths. The most efficient way to accomplish multi-operand addition is using N-2 adder compressors (ACs), which compress the N operands to just two [1]. The compression operation is also called a carry-save due to its capability of postdating the carry propagation to be recombined once in the final recombination adder. The recombination completes the adder tree propagating the carry for just two remaining operands.

The reduced carry propagation of AC offers savings in the circuit area, critical path, and dynamic power dissipation compared with a tree implemented with just two-operand adders. The drawback of the AC design alternative is that one can obtain just the final value of the addition tree, making intermediate sum values nonexistent for reusing purposes. Even that, ACs have been employed for several prominent computing kernels as multipliers, multiply-accumulate (MACs) systolic arrays for machine learning [2], digital filters [3], discrete transforms [4], [5], [6] and video processing [7], [8], [9]. Nevertheless, to the best of our knowledge, the adder compressor's robustness has received little to no attention from researchers in the reliability field.

Variability is a meaningful concern in reliable circuit design and even more critical towards recent industrially adopted technologies such as FinFETs. Although FinFET nodes have brought many advances, such as less power consumption, it has also brought some challenges, requiring a deep and detailed analysis of the variability impact caused on the circuits.

This brief presents a robustness analysis of a 3-2 adder compressor designed in a 7nm FinFET technology. The robustness analysis evaluates the design performance under the effects of the process, voltage, and temperature (PVT) variations. It provides additional statistical metrics to measure the performance, defining the chip's immunity to variations and driving power-performance-area (PPA) improvements. We evaluate the robustness analysis at a super-threshold voltage (i.e., 700mV) and the trade-off in power and delay if scaling the voltage to the near-threshold (i.e., 350mV).

This brief is organized as follows. Section II explains adder compressors, provides background about variability in FinFETs and presents the main related works. Section III describes the design methodology adopted in this brief. Section IV and Section V present the discussion of the results considering super- and near-threshold operation regimes, respectively. Finally, Section VI concludes this brief.

II. Background

This section revises the transistor-level implementation of the 3-2 adder compressor, presents the principal sources of variability in FinFETs, and highlights the main related works.

A. 3-2 Adder Compressor

The key idea of AC relies on adding more than two operands simultaneously with a reduced critical path [10]. The 3-2 adder compressor is one of the most commonly used compressors. The single-bit 3-2 AC compresses the three operands into two without a carry propagation. The n-bit *Sum* is the $A+B+C$ result value before considering the *Cout* (carry out). Then, the final $A+B+C$ addition S is given in (1). Note that

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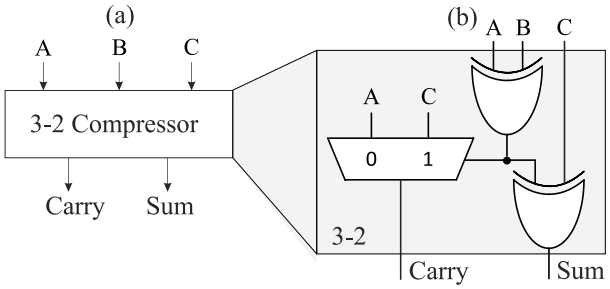

Fig. 1. (a) Block diagram representation of 3-2 adder compressor (b) Conventional implementation of 3-2 adder compressor.

TABLE I
MAIN DEVICE PARAMETERS AND LAYOUT LAYERS [16]

Device Parameters			Layout Layers (nm)		
Gate Length (LG)		21nm		Width	Pitch
Fin Width (WFIN)		6.5nm	**Fin**	6.5	27
Fin Height (HFIN)		32nm	**Active**	54	108
Oxide Thickness (Tox)		2.1nm	**Gate**	21	54
Channel Doping		$1\times10^{22}m^{-3}$	**SDT/LISD**	25	54
Source/Drain Doping		$2\times10^{26}m^{-3}$	**LIG**	16	54
Work-	**NFET**	4.3720eV	**VIA0-3**	18	25
Function	**PFET**	4.8108eV	**M1-3**	18	36

the first *Cout* generation starts in the second LSB (least significant bit) position, which made it shift left in (1). The 3-2 is the most simple structure of AC, which adds three operands simultaneously, with a simple critical path of two XOR gates, as shown in Fig. 1. It is noticeable that the 3-2 adder compressor can operate as a mux-based full-adder if we use the carry input as an operand.

$$S = Sum + Carry << 1 \tag{1}$$

B. Variability in FinFETs

The technology scaling to maintain the pace of performance and density gain results in increased design complexity with more potential variability sources. Variability is related to the random deviation, which causes an increase or decrease in typical design specifications [11]. Due to the variability, each circuit can present a different electrical behavior, such as abnormal power dissipation and performance deviation.

The main issue associated with variability is the uncertainty about the correct circuit operation because there is no guarantee that a circuit will behave as expected after the manufacturing process. The unexpected behavior can stimulate the circuit degradation besides making it inappropriate for the initial purpose [12]. The variability sources can be divided into three categories: Environmental, reliability, and physical [13].

Environmental sources are deviations in the operating conditions during the circuit lifetime, such as variations in switching frequency, temperature, supply voltage, and noise. Reliability sources relate to transistor aging due to the rising electrical fields through the oxide thickness presented in modern circuits. Finally, physical sources are associated with structural variations during the manufacturing process.

In FinFETs, the main sources of process variability are the line edge roughness (LER) and metal gate granularity (MGG) [14]. LER corresponds to a deviation in the transistor edge position compared with the best-fit line of the ideal shape. MGG refers to the random orientation of the different metal grains leading to variations in the gate work function. In general, the electrical behavior of circuits designed in FinFET is more impacted by MGG than LER variations [15].

C. Related Works

A novel non-hierarchical 8-2 adder compressor with a limited carry propagation path for N-bit operands was designed in [1], minimizing both circuit delay and power dissipation. The results presented in [4] showed that discrete Tchebichef transform (DTT) solutions with adder compressors minimize the cell area and power dissipation. The authors used the 4-2, 6-2, and 8-2 adder compressors to provide power-efficient DDT. Similarly, the work in [5] used efficient 4-2 and 8-2 adder compressors for the power-efficient 2D discrete cosine transform (DCT) implementation.

In [6], the use of 5-2 adder compressors improved the power efficiency of the split-radix butterfly. The results showed that the best-proposed split-radix saves up to 47.28 % of power dissipation. In [7], a new compressor was proposed and used to implement additions and subtractions of the Hadamard transforms module (HTM) while using conventional 4-2 and 8-2 adder compressors to implement the sum of absolute values (SAV) module. An 8-2 adder compressor was explored in the addition tree of the sum of squared differences (SSD) architecture in [8]. The results revealed that the SSD employing the 8-2 hierarchical adder compressor saves on average 29.4% of total power dissipation.

In the literature, several works explore the use of adder compressors to improve the area and total power dissipation in several applications. However, a few research proposed robustness analysis, mainly in FinFET circuits. For this reason, this brief evaluates the impact of PVT variations on a 3-2 adder compressor, as it is one of the most widely used compressors.

III. EVALUATION METHODOLOGY

This brief evaluates the impact of PVT variations on a 3-2 adder compressor using the 7nm FinFET process design kit (PDK) developed by Arizona State University in partnership with ARM for academic use [16]. The ASAP7 PDK considers realistic design conjectures regarding lithography steps and the current technology competencies of commercial nodes. Table I shows a summary of device parameters and layout layers from ASAP7 PDK.

The design flow of this brief is composed of ten steps, as shown in Fig. 2. The design specification ❶ defines the number of fins of all transistors of a 3-2 adder compressor and the technological model used. We adopted the regular threshold voltage (RVT) model from ASAP7 at a typical configuration (TT). Multi-gate devices present similar mobility and threshold voltages. Therefore, we adopt equal sizing for both PFET and NFET transistors (i.e., three fins). We also consider the same sizing for all transistors, aiming not to stress the routability

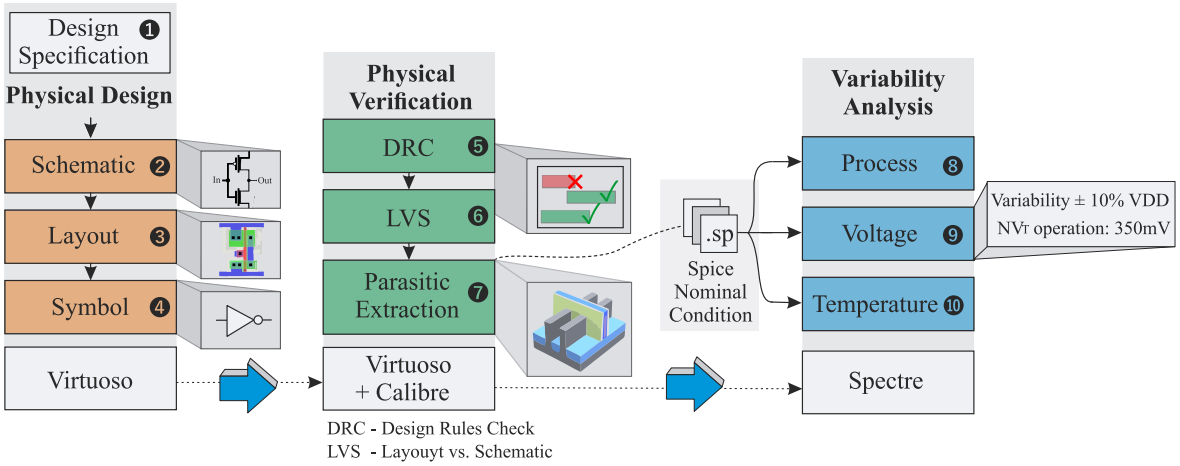

Fig. 2. Design flow adopted in this brief. The flow starts with design specification ❶, the circuit schematic ❷ description, and the layout design ❸, with a correspondent symbolic creation ❹ using the Cadence Virtuoso tool. The layout passes through the design rule check (DRC) ❺ to verify the correctness with the process rules, and layout versus schematic (LVS) ❻ to verify the physical correctness in comparison with the layout both including the Siemens Calibre tool to Cadence Virtuoso. The circuit parasitic is extracted to generate a physically-aware spice model of the 3-2 AC logic cell. Finally, the post-layout variability is evaluated for process ❽, voltage (±10%) ❾ and temperature (from −50°C to 150°C) ❿ in a Monte Carlo simulation using Cadence Spectre considering both super- and near-threshold regimes, i.e., operating at 700mV and 350mV respectively.

and to prevent the layout against poor density [17]. We implement the physical design of the schematic ❷, layout ❸, and symbol ❹ of 3-2 AC employing the Cadence Virtuoso tool. We set the height of the circuit as 7.5 tracks of metal 2 (M2).

The layout passes through a verification flow composed of a design rule check (DRC) ❺ and layout versus schematic (LVS) steps ❻ as well as the parasitic extraction steps employing Mentor Graphics Calibre and Cadence Virtuoso tools. A new SPICE-level netlist is generated with information extracted from the layout, the parasitic wire resistances, and capacitances (RC) ❼. This extracted SPICE file contains extra layout-driven details to perform more accurate electrical simulations.

According to [15], work-function (WF) is the most influenced parameter by process variations in FinFET technologies. Therefore, the process variability ❽ is taken through 2,000 Monte Carlo (MC) simulations with the WF parameter modeled as a Gaussian function with 3σ of deviation and 5% of fluctuations. The normalized standard deviation (σ/μ) indicates the circuit sensitivity against process variations. A design is considered robust if it has the lowest value for the σ/μ relation. For environmental factors, we perform ±10% of the nominal supply voltage deviation (i.e., 700mV) to represent the voltage variability ❾ and also simulated the operation at a near-threshold regime (i.e., 350mV). Also, we evaluate the temperature variability ❿ using the range from −50°C to 125°C.

IV. Super-Threshold Voltage Operation

This section presents the results considering super-threshold voltage operation (700mV). Table II shows the behavior of the 3-2 adder compressor in nominal conditions and under the effects of process variations. The nominal column is considered a reference, representing the values without any variability. Power is the most impacted by process variability

TABLE II
Influence of Process Variation on Power, Delay, and PDP of the 3-2 AC at Super-Threshold Regime

Metrics		Nominal	Mean	Sigma	Min	Max	σ/μ(%)
Power (nW)		420	449	171	376	5010	38.08
Delay (ps)	Sum	24.8	26.1	5.1	16.4	57.3	19.69
	Cout	39.7	42.1	8.7	26.3	99.6	20.74
PDP (aJ)	Sum	10.4	11.5	3.0	9.7	82.5	26.07
	Cout	16.7	18.4	4.9	15.5	13.2	26.63

at super-threshold voltage operation among the three metrics analyzed, with a deviation of 38% from the nominal value. The impact on delay is around 20% for both outputs (*Sum* and *Cout*) of the adder compressor evaluated. Similar behavior happens for PDP since the impact on both outputs is around 26%. The Min and Max columns represent the minimum, and maximum values for each metric, considering all 2, 000 MC simulations.

Fig. 3 presents the delay variability histogram for the worst paths between the inputs up to *Sum* and *Cout* outputs. This histogram shows the behavior of the 3-2 adder compressor delay variability through the 2, 000 MC simulations performed in this brief. The *Cout* output presents a smaller density due to the significant deviation, with a mean value of 42.1ps and a standard deviation of 8.7ps.

Fig. 4 indicates the PDP behavior under variations of ±10% of the nominal voltage. The increase of supply voltage (i.e., 770mV) modifies the PDP of both outputs (*Sum* and *Cout*) of the 3-2 adder compressor by around 10%. On the other hand, the voltage reduction (i.e., 630mV) generates an impact of around 7% if compared with nominal conditions (i.e., 700mV). When the supply voltage increases or decreases, a similar trend is observed for the delay and power metrics. The impact on power is around 20%, and the influence on delay is 11% and 15% for *Sum* and *Cout* outputs, respectively.

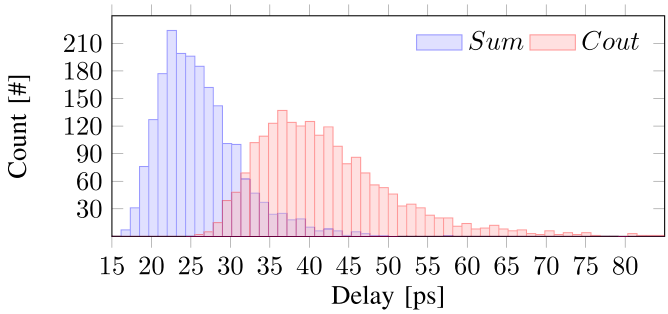

Fig. 3. Delay variability histogram for *Sum* and *Cout* worst paths of the adder compressor outputs.

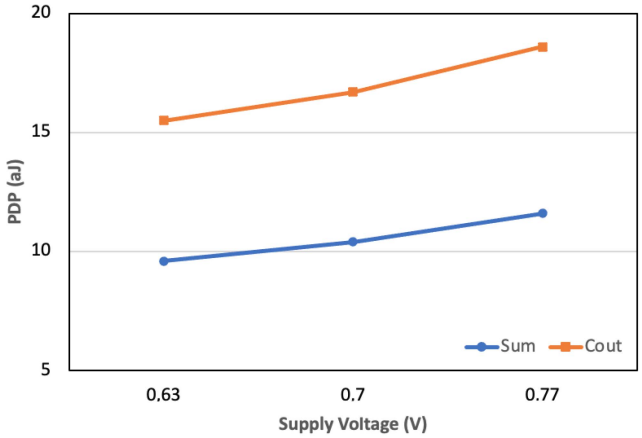

Fig. 4. Effect of voltage variations on PDP of the 3-2 AC.

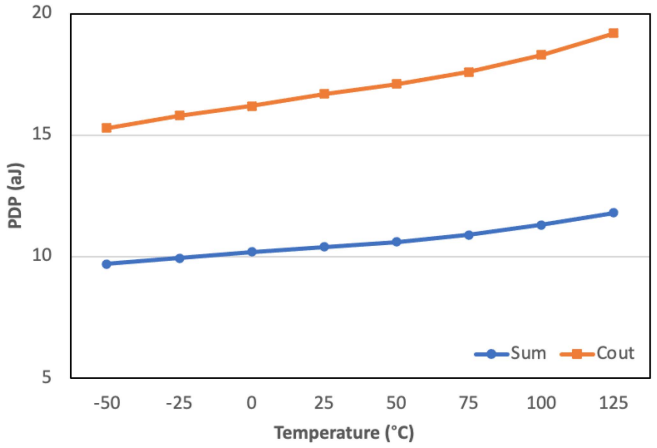

Fig. 5. Impact of temperature oscillations on PDP of the 3-2 AC.

TABLE III
INFLUENCE OF PROCESS VARIATIONS ON POWER, DELAY, AND PDP OF THE 3-2 AC AT NEAR-THRESHOLD REGIME

Metrics		Nominal	Mean	Sigma	Min	Max	σ/μ(%)
Power (nW)		92.8	84.9	40.8	10.0	979	48.06
Delay (ps)	Sum	179	262	228	27.4	993	87.02
	Cout	312	334	222	46.9	999	66.47
PDP (aJ)	Sum	16.6	22.1	16.8	42.8	73.0	76.02
	Cout	28.9	31.4	21.8	74.6	87.1	69.43

Fig. 5 presents PDP results under temperature variations. By reducing the temperature to negative values (−50°C), the impact on *Sum* and *Cout* outputs reach up to 6.7% and 8.4%, respectively. However, the impact on the PDP due to the temperature rise (125°C) is more significant than the reduction. It means that the PDP of the 3-2 adder compressor suffers an increase of up to 11.8% and 13% on *Sum* and *Cout* outputs, respectively. Unlike the behavior of process and voltage variability, the temperature deviation has a difference of around 2% on PDP between the two outputs. At 125°C, the 3-2 AC increases around 9.7% of the power consumption. The impact on power is less severe when the temperature reduces to −25°C, reaching only 3% of deviation. For *Sum* output, on average, we have an increase of 4% and 2% on delay for lower and higher temperatures, respectively. On the other hand, the *Cout* output suffers from a little more influence by the voltage variation. The impact on *Cout* is around 1.3% more if compared with *Sum* output.

V. NEAR-THRESHOLD VOLTAGE OPERATION

This section presents the results of the 3-2 adder compressor considering near-threshold voltage operation (350mV). Table III shows that near-threshold operation implies high process variability susceptibility for all metrics evaluated. Unlike the super-threshold operation, the least impacted metric by the process variation is the power, with a 48.06% deviation. The *Sum* output suffered the most significant impact due to variations for both the delay and the PDP. However, the difference between the two outputs is 20.5% for the delay and 6.6% for the PDP.

Comparing the results presented in Tables II and III, we can note that the near-threshold operation significantly reduces the total power dissipation by 77.9% for the 3-2 adder compressor evaluated, with an average delay penalty of 7.5 times in both outputs. When the 3-2 adder compressor is under the process variation effects, the total power reduction decreases to 39.8%. Moreover, the delay penalty for *Sum* and *Cout* outputs is 10x and 8x larger, respectively. This behavior emphasizes that process variability needs a careful investigation in FinFET-based circuits.

A comparison of process variability sensitivity in the 3-2 adder compressor with different threshold regimes can be seen in Fig. 6. As expected, the robustness of the 3-2 adder compressor is more significant in the near-threshold regime for all metrics. The sensitivity to process variations increases by 10% for the power in the near-threshold regime. The influence is more alarming for the delay and the PDP, reaching 56.5% and 46.4%, respectively, on average for the two outputs. The *Sum* output is more susceptible in both metrics, mainly to the delay.

Fig. 7 shows the influence of temperature variations when the 3-2 adder compressor operates at a near-threshold regime. The difference between the PDP of *Sum* and *Cout* outputs reduces as temperature increases. The 3-2 adder compressor is more robust for temperature variations above 25°C, suffering an increase of up to 35% at 125°C for both outputs. Otherwise, the temperature reduction to −50°C generates an increase of 43.5% in the PDP. When the temperature decreases

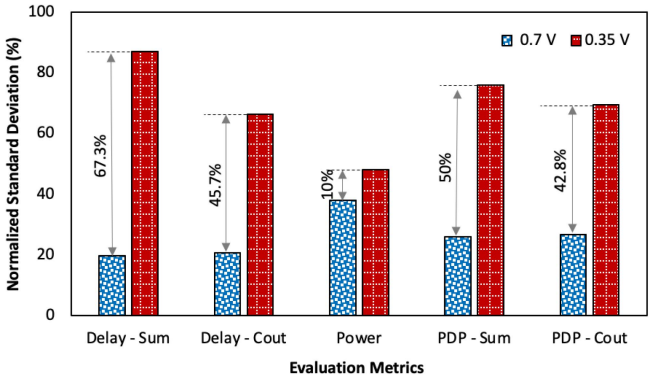

Fig. 6. Comparison of process variation effects on 3-2 adder compressor with different threshold regimes.

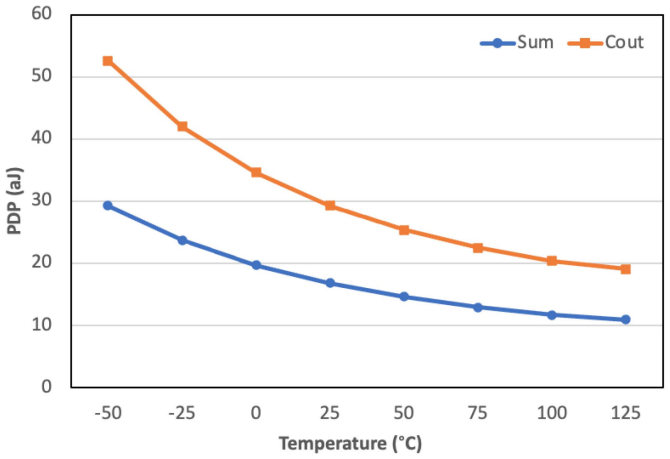

Fig. 7. Impact of temperature variations at near-threshold regime.

(−25°C), the power consumption has an insignificant impact of 2.5%. The influence is slightly greater when the temperature increases to 125°C, reaching 9% more consumption. On the other hand, the impact on delay for both outputs is significantly more severe. The delay of *Sum* and *Cout* outputs increases around 45% and 40% when the temperature is −25°C and 125°C, respectively.

VI. Conclusion

This brief investigated the process, voltage, and temperature variability analysis of the 3-2 adder compressor circuit designed in a 7nm FinFET technology. All types of variability significantly affect the expected behavior of the 3-2 adder compressor. However, process variations are the main concern in both operating regimes, presenting an even more alarming scenario in the near-threshold operation. It emphasizes the relevance of evaluating all the effects of PVT variability on very large-scale integrated circuits and the necessity of creating new design guidelines to deal with the reliability challenges imposed by current technologies.

In future works, we plan to evaluate the robustness of higher-order adder compressors, such as 4-2 and 5-2 topologies. We will also assess the influence of transient faults arising from radiation sources in all topologies investigated. Then, we will investigate circuit and layout-level mitigation techniques to reduce the impact caused by PVT variations and soft errors.

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