

D/A Conversion & A/D conversion

- D/A & A/D are two very important aspects of digital data processing.
- Digital to analog conversion involves translation of digital information to equivalent analog information.
- Output of a digital system might be changed to analog form for the purpose of driving a pen recorder.
- In this respect, a D/A converter is sometimes considered a decoding device.
- The process of changing an analog signal to an equivalent digital signal is accomplished by the use of an A/D converter.
- For example, an A/D converter is used to change the analog output signals from transducers which measure temperature, pressure etc into equivalent digital signals.
- These signals would then be in a form suitable for entry into a digital system.
- An A/D device is often called as a ~~encoding~~ device.

D/A conversion

12-1 Variable Resistor Networks

- The basic problem in converting a digital signal into an equivalent analog signal is to change n digital voltage levels into one equivalent analog voltage.
- This can be done by designing a resistive network that will change each digital level into an equivalent binary weighted voltage (or current).

Binary equivalent weight

- Consider the truth table for the 3-bit binary signal shown below:

2^2	2^1	2^0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	1	0
1	1	1

- Suppose we want to change the eight possible digital signals into equivalent analog voltages.
- The smallest number represented is $000 = 0V$
- The largest number is $111 = +7V$
- This then establishes the range of the analog signal to be developed.
- Between 000 and 111 there are seven discrete levels to be defined.
- Therefore it is convenient to divide the analog signal into seven levels.
- The smallest incremental change is represented by the LSB 2^0 .
- i.e. it is equal to $\frac{1}{7}m$ of the full scale analog output voltage.
- The resistive divider will then be designed in such a way that a 1 in 2^0 position will cause $+7 \times \frac{1}{7} = +1V$ at the output.

$$\rightarrow 2^0 = 1 \quad 2^1 = 2$$

- (4)
- A 1 in the 2¹ position must cause a change in the analog output voltage that is twice the size of LSB.
 - The resistive divider must then be constructed such that a 1 in 2¹ position will cause a change of $+7 \times \frac{2}{7} = +2V$ in the analog output voltage.
 - Similarly $+7 \times \frac{4}{7} = +4V$. for 2² bit.
 - Thus 1 LSB is given a binary equivalent weight of $\frac{1}{7}$ or 1 part of 7.
 - Notice that the sum of weights must be equal to 1 $\frac{1}{7} + \frac{2}{7} + \frac{4}{7} = \frac{7}{7} = 1$.
 - The binary weight assigned to the LSB is $\frac{1}{2^n - 1}$, where n is the number of bits.

Problem Find binary wt of each bit in a 4-bit system

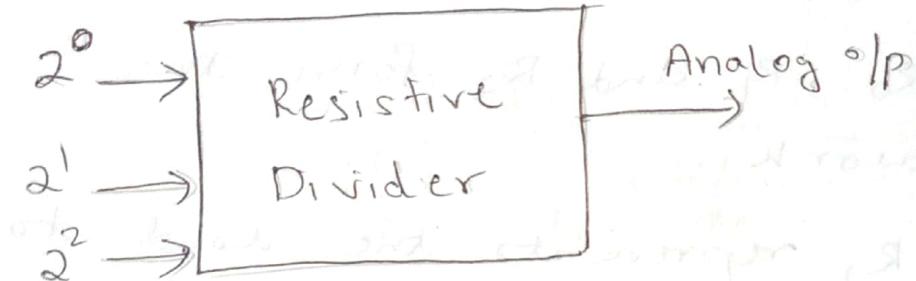
Bit	wt
2 ⁰	1/15
2 ¹	2/15

$$2^2 \left| \begin{array}{l} 4/15 \\ 8/15 \end{array} \right. = \frac{15}{15} = 1$$

(5)

Resistive divider:

- what is now desired is a resistive divider that has three digital inputs and one analog output.
- Assume that the digital input levels are $0 = 0V$ $1 = +7V$



Digital input	Analog output
000	+0V
001	+1V
010	+2V
011	+3V
100	+4V
101	+5V
110	+6V
111	+7V

→ For input 010 output = 2V

→ For input 101 output = 5V

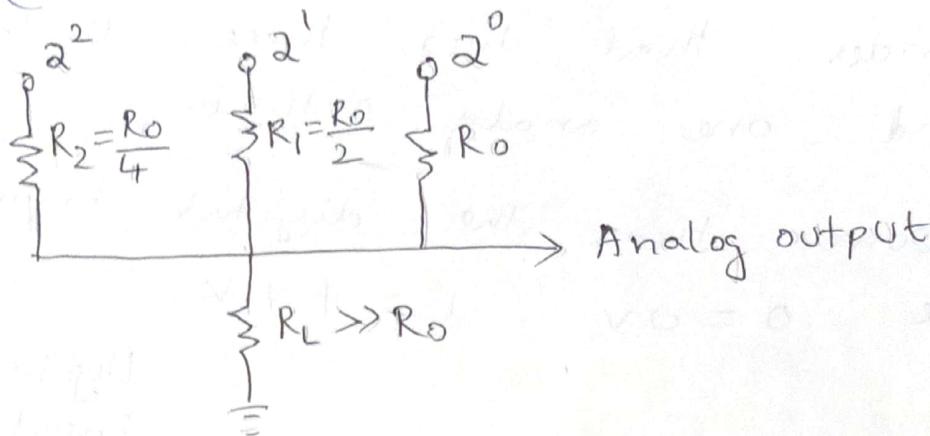
→ Thus the resistive divider must do two things in order to change the digital input into an equivalent analog voltage:

1) 2^0 must be charged to +1V, 2^1 bit must be charged to +2V, 2^2 bit must be charged to +4V

2) These three voltages representing the digital bits must be summed together to form the analog o/p v_o

(6)

→ A resistive divider that performs the above two functions is shown below.

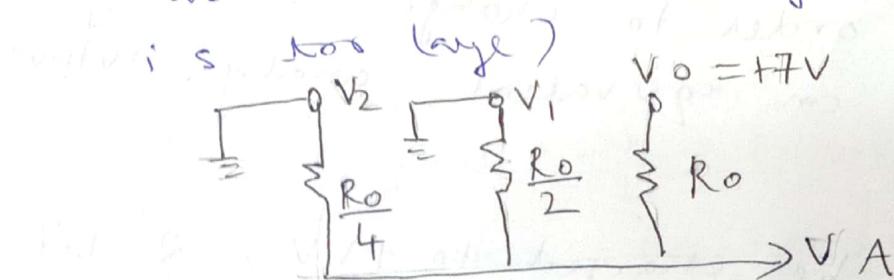


→ Resistors R_0 , R_1 and R_2 form the divider network.

→ Resistance R_L represents the load to which the divider is connected.

→ Assume the digital input signal V_2 applied to this network.

→ we can redraw the above network as shown below. (neglect R_L as it is too large)



→ The analog output voltage can be most easily found by use of Millman's theorem, which states that the voltage appearing at any node in a resistive network = summation of currents entering the node / summation of conductances connected to the node.

→ In equation form, mill mains theorem is (7)

$$V = \frac{v_1/R_1 + v_2/R_2 + v_3/R_3 + \dots}{1/R_1 + 1/R_2 + 1/R_3 + \dots}$$

$$V_A = \frac{v_0/R_0 + v_1/(R_0/2) + v_2/(R_0/4)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)}$$
$$= \frac{7/R_0}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)} = \frac{7}{7} = 1 \text{ V.}$$

→ To summarize, a resistive divider can be built to change a digital voltage into an equivalent analog voltage.

→ The following criteria can be applied to this divider

- ① There must be one input resistor for each digital bit.
- ② Beginning with the LSB, each following resistor value is one half the size of the previous resistor.
- ③ The full scale output voltage is equal to the positive voltage of the digital input signal.

$$I = +7 \text{ V for three bits}$$

④ The LSB has a weight $\frac{1}{(2^n - 1)}$

where $n \rightarrow$ no of input bits

⑤ The change in output voltage due to change in the LSB is equal to $\sqrt{\frac{V}{(2^n - 1)}}$ where V is the digital input voltage level.

⑥ The output voltage V_A can be found for any digital input signal by using the following modified form of millmann's theorem.

$$V_A = \frac{v_0 2^0 + v_1 2^1 + v_2 2^2 + \dots + v_{n-1} 2^{n-1}}{2^n - 1}$$

where,

v_0, v_1, \dots, v_{n-1} are digital input voltage levels.

$n \rightarrow$ no of input bits.



→ 12.2 Page 434.

→ Two problems with resistive divider.

① Each resistor in the nw has a different value

② Added expense becomes unattractive

case of this 3-bit system) is given a weight of $\frac{4}{7}$, which is 4 times the LSB or 4 parts in 7. Notice that the sum of the weights must equal 1. Thus $\frac{1}{7} + \frac{2}{7} + \frac{4}{7} = \frac{7}{7} = 1$. In general, the binary equivalent weight assigned to the LSB is $1/(2^n - 1)$, where n is the number of bits. The remaining weights are found by multiplying by 2, 4, 8, and so on. Remember,

$$\text{LSB weight} = \frac{1}{(2^n - 1)}$$

EXAMPLE 12.1

Find the binary equivalent weight of each bit in a 4-bit system.

Solution

The LSB has a weight of $1/(2^4 - 1) = 1/(16 - 1) = \frac{1}{15}$, or 1

part in 15. The second LSB has a weight of $2 \times \frac{1}{15} = \frac{2}{15}$.

The third LSB has a weight of $4 \times \frac{1}{15} = \frac{4}{15}$, and the MSB

has a weight of $8 \times \frac{1}{15} = \frac{8}{15}$. As a check, the sum of the

weights must equal 1. Thus $\frac{1}{15} + \frac{2}{15} + \frac{4}{15} + \frac{8}{15} = \frac{15}{15} = 1$. The binary equivalent weights for 3-bit and 4-bit systems are summarized in Fig. 12.2.

Bit	Weight	Bit	Weight
2^0	$1/7$	2^0	$1/15$
2^1	$2/7$	2^1	$2/15$
2^2	$4/7$	2^2	$4/15$
2^3	$8/7$	2^3	$8/15$
Sum	7/7	Sum	15/15

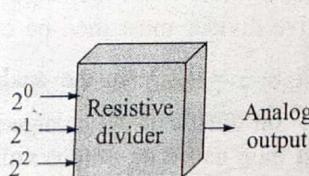
(a)

(b)

Fig. 12.2 Binary equivalent weights.

Resistive Divider

What is now desired is a resistive divider that has three digital inputs and one analog output as shown in Fig. 12.3a. Assume that the digital input levels are 0 = 0 V and 1 = +7 V. Now, for an input of 001, the output will be +1 V. Similarly, an input of 010 will provide an output of +2 V, and an input of 100 will provide an output of +4 V. The digital input 011 is seen to be a combination of the signals 001 and 010. If the +1 V from the 2^0 bit is added to the +2 V from the 2^1 bit, the desired +3 V output for the 011 input is achieved. The other desired voltage levels are shown in Fig. 12.3b; they, too, are additive combinations of voltages.



Digital input	Analog output
0 0 0	+0 V
0 0 1	+1 V
0 1 0	+2 V
0 1 1	+3 V
1 0 0	+4 V
1 0 1	+5 V
1 1 0	+6 V
1 1 1	+7 V

(a)

(b)

Fig. 12.3

6. The output voltage V_A can be found for any digital input signal by using the following modified form of Millman's theorem:

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \cdots + V_{n-1} 2^{n-1}}{2^n - 1} \quad (12)$$

where $V_0, V_1, V_2, V_3, \dots, V_{n-1}$ are the digital input voltage levels (0 or V) and n is the number of input bits.

EXAMPLE 12.2

For a 5-bit resistive divider, determine the following: (a) the weight assigned to the LSB; (b) the weights assigned to the second and third LSB; (c) the change in output voltage due to a change in the LSB, the second LSB, and the third LSB; (d) the output voltage for a digital input of 10101. Assume $0 = 0 \text{ V}$ and $1 = +10 \text{ V}$.

Solution

- (a) The LSB weight is $1/(2^5 - 1) = 1/31$.
- (b) The second LSB weight is $2/31$, and the third LSB weight is $4/31$.
- (c) The LSB causes a change in the output voltage of $10/31 \text{ V}$. The second LSB causes an output voltage change of $20/31 \text{ V}$, and the third LSB causes an output voltage change of $40/31 \text{ V}$.
- (d) The output voltage for a digital input of 10101 is

$$\begin{aligned} V_A &= \frac{10 \times 2^0 + 0 \times 2^1 + 10 \times 2^2 + 0 \times 2^3 + 10 \times 2^4}{2^5 - 1} \\ &= \frac{10(1 + 4 + 16)}{32 - 1} = \frac{210}{31} = +6.77 \text{ V} \end{aligned}$$

This resistive divider has two serious drawbacks. The first is the fact that each resistor in the network has a different value. Since these dividers are usually constructed by using precision resistor networks, added expense becomes unattractive. Moreover, the resistor used for the MSB is required to handle a much greater current than that used for the LSB resistor. For example, in a 10-bit system, the current through the MSB resistor is approximately 500 times as large as the current through the LSB resistor (see Prob. 12.5). For these reasons, a second type of resistive network, called a *ladder*, has been developed.

SELF-TEST



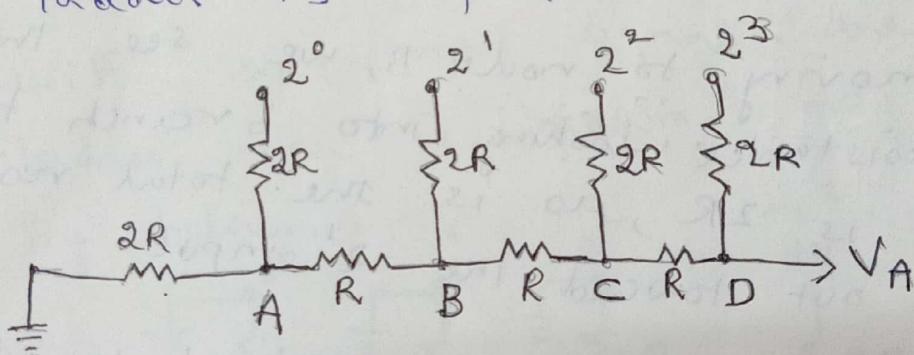
1. What is the LSB weight of a 6-bit resistive ladder?
2. What is the value of V_A in Example 12.2 if the MSB is 0?

12.2 BINARY LADDERS

The *binary ladder* is a resistive network whose output voltage is a properly weighted sum of digital inputs. Such a ladder, designed for 4 bits, is shown in Fig. 12.6. It is constructed so that the digital inputs have only two values and thus overcomes one of the objections to the resistive dividers previously discussed. The left end of the ladder is terminated in a resistance of $2R$, a

12.2 Binary Ladders :

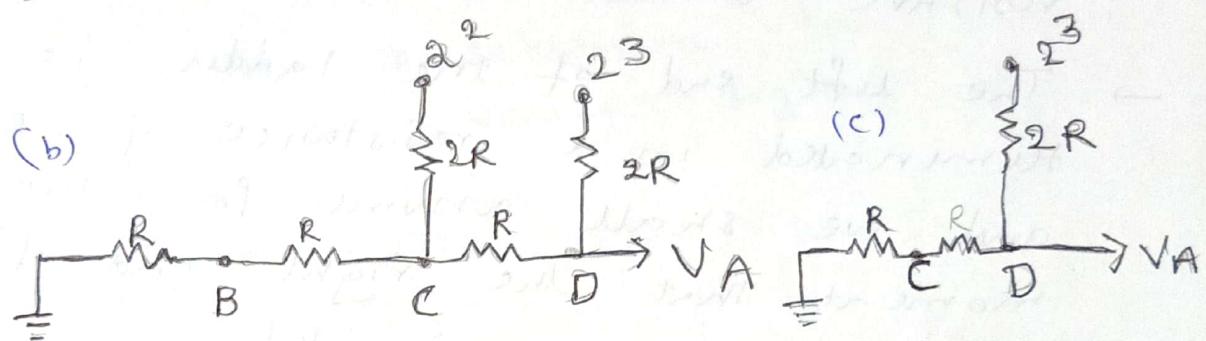
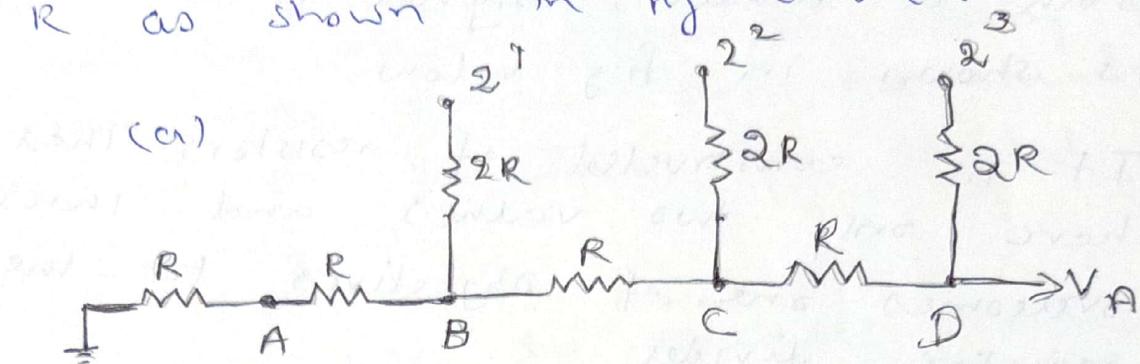
- The binary ladder is a resistive network whose output voltage is a properly weighted sum of the digital inputs.
- such a ladder, designed for 4 bits, is shown in fig below.
- It is constructed of resistors that have only two values and thus overcomes one of objectives to the resistive divider.
- The left end of the ladder is terminated in a resistance of $2R$ and we shall assume for the moment that the right end of the ladder is open circuited.



- Let us examine the resistive properties of the network, assuming that all the digital inputs are at ground.
- Beginning at node A, the total resistance looking into the terminating resistor is $2R$.

→ The total resistance looking out toward the 2^1 input is also $2R$.

→ These two resistors can be combined to form an equivalent resistor of value R as shown in fig below. (fig a)



→ Now moving to node B, we see that total resistance looking into branch towards node A is $2R$, as is the total resistance looking out toward the 2^1 input.

→ These resistors can be combined to simplify the network as shown in fig (b)

→ From fig (b) it can be seen that the total resistance looking from node C down the branch toward node B or out the branch toward the 2^2 input is still $2R$.

→ The fig reduces to fig (c)

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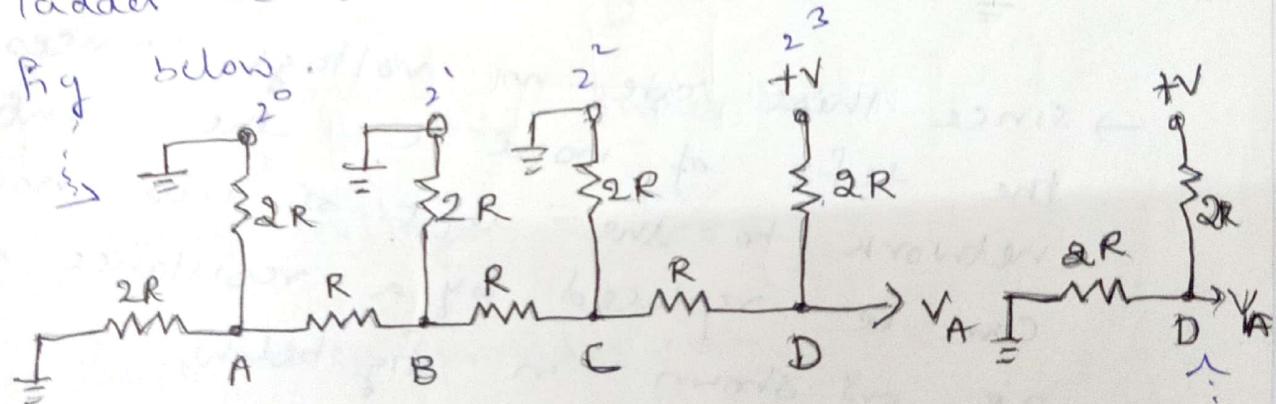
→ From this equivalent circuit, it is clear that the resistance looking back toward node C is $2R$, as is the resistance looking out toward the 2^3 input. (11)

→ From the preceding discussion, we conclude that the total resistance looking from any node back toward the terminating resistor or out toward the digital input is $s^2 R$.

→ we can use the resistance characteristics of the ladder to determine the output voltages for the various digital inputs.

→ First, assume that the digital input signal is 1000 binary

→ with this input signal, the binary ladder can be drawn as shown in



→ Since there are no voltage sources to the left of node D, the entire network to the left of this node can be replaced by a resistance of $2R$ to form the equivalent circuit shown above.

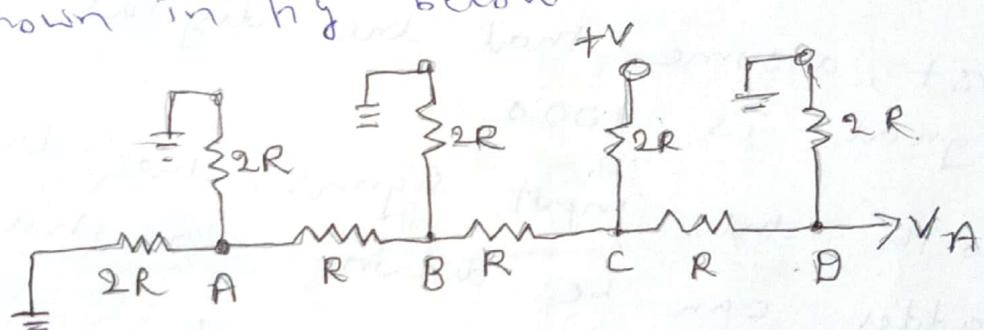
→ From this equivalent circuit, it can be easily seen that the output voltage is

$$V_A = V \times \frac{2R}{2R + 2R} = \frac{+V}{2}$$

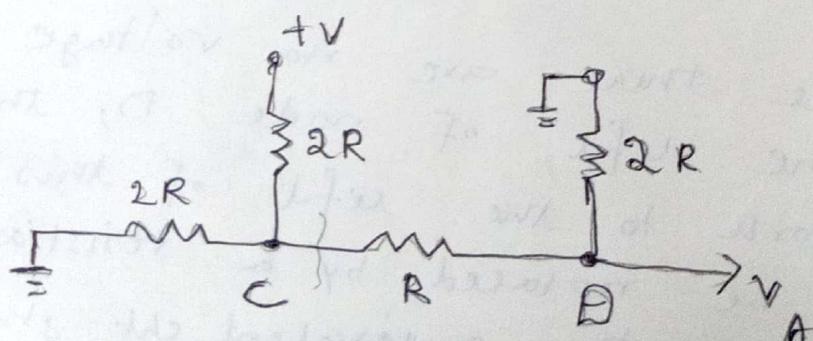
→ Thus a '1' in the MSB position will provide an output voltage $\frac{+V}{2}$

→ To determine the output voltage due to the second MSB, assume a digital input signal 0100.

→ This can be represented by the circuit shown in fig below.



→ since there are no voltage sources to the left of node C, the entire network to the left of this node can be replaced by a resistance of $2R$, as shown in fig below.



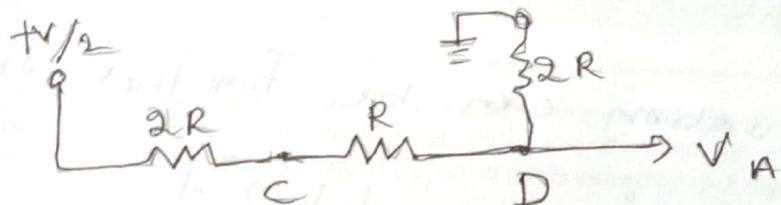
→ Replace the network to the left of node C with its Thevenin equivalent by cutting the circuit on the "}" line shown in figure

→ The Thevenin equivalent is clearly a resistance R in series with a voltage source $\frac{+V}{2}$.

→ The final equivalent circuit with the Thevenin equivalent included is shown in fig below.

→ The output voltage from this circuit is

$$V_A = \frac{+V}{2} \times \frac{2R}{R + R + 2R} = \frac{+V}{4}$$



→ similarly for the third bit

$$\text{output voltage} = \frac{+V}{8}$$

→ Fourth MSB provides an

$$\text{output voltage} = \frac{+V}{16}$$

EX 12-3

(Page 437)

- since the ladder is composed of linear resistors, it is a linear network and the principle of superposition can be used.
- The total output voltage due to a combination of input digital levels can be found by simply taking the sum of the output levels caused by each digital input individually.

- In equation form, the output voltage is given by:

$$V_A = \frac{V}{2} + \frac{V}{4} + \frac{V}{8} + \frac{V}{16} + \dots + \frac{V}{2^n}$$

$n \rightarrow$ total number of bits at the input.

- The equation can be further simplified

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + \dots + V_{n-1} 2^{n-1}}{2^n}$$

(Ex 12.4)

$$V_A = V \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \dots + \frac{1}{2^n} \right)$$

(Ex 12.5)

$$= \frac{10}{31} + \frac{20}{31} + \frac{40}{31} + \frac{80}{31} + \frac{160}{31}$$

This process can be continued, and it can be shown that the third MSB provides an output voltage of $+V/8$, the fourth MSB provides an output voltage of $+V/16$, and so on. The output voltages for the binary ladder are summarized in Fig. 12.10; notice that each digital input is transformed into a properly weighted binary output voltage.

EXAMPLE 12.3

What are the output voltages caused by each bit in a 5-bit ladder if the input levels are $0 = 0 \text{ V}$ and $1 = +10 \text{ V}$?

Solution

The output voltages can be easily calculated by using Fig. 12.10. They are

$$\text{First MSB } V_A = \frac{V}{2} = \frac{+10}{2} = +5 \text{ V}$$

$$\text{Second MSB } V_A = \frac{V}{4} = \frac{+10}{4} = +2.5 \text{ V}$$

$$\text{Third MSB } V_A = \frac{V}{8} = \frac{+10}{8} = +1.25 \text{ V}$$

$$\text{Fourth MSB } V_A = \frac{V}{16} = \frac{+10}{16} = +0.625 \text{ V}$$

$$\text{LSB = fifth MSB } V_A = \frac{V}{32} = \frac{+10}{32} = +0.3125 \text{ V}$$

Bit position	Binary weight	Output voltage
MSB	$1/2$	$V/2$
2d MSB	$1/4$	$V/4$
3d MSB	$1/8$	$V/8$
4th MSB	$1/16$	$V/16$
5th MSB	$1/32$	$V/32$
6th MSB	$1/64$	$V/64$
7th MSB	$1/128$	$V/128$
.	.	.
Nth MSB	$1/2^N$	$V/2^N$

Fig. 12.10 Binary ladder output voltages.

Since this ladder is composed of linear resistors, it is a linear network and the principle of superposition can be used. This means that the total output voltage due to a combination of input digital levels can be found by simply taking the sum of the output levels caused by each digital input individually.

In equation form, the output voltage is given by

$$V_A = \frac{V}{2} + \frac{V}{4} + \frac{V}{8} + \frac{V}{16} + \cdots + \frac{V}{2^n} \quad (12.2)$$

where n is the total number of bits at the input.

This equation can be simplified somewhat by factoring and collecting terms. The output voltage can then be given in the form

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \cdots + V_{n-1} 2^{n-1}}{2^n} \quad (12.3)$$

where $V_0, V_1, V_2, \dots, V_{n-1}$ are the digital input voltage levels. Equation (12.3) can be used to find the output voltage from the ladder for any digital input signal.

EXAMPLE 12.4

Find the output voltage from a 5-bit ladder that has a digital input of 11010. Assume that $0 = 0 \text{ V}$ and $1 = +10 \text{ V}$.

$$V_A = \frac{0 \times 2^0 + 10 \times 2^1 + 0 \times 2^2 + 10 \times 2^3 + 10 \times 2^4}{2^5}$$

$$= \frac{10(2+8+16)}{32} = \frac{10 \times 26}{32} = +8.125\text{v}$$

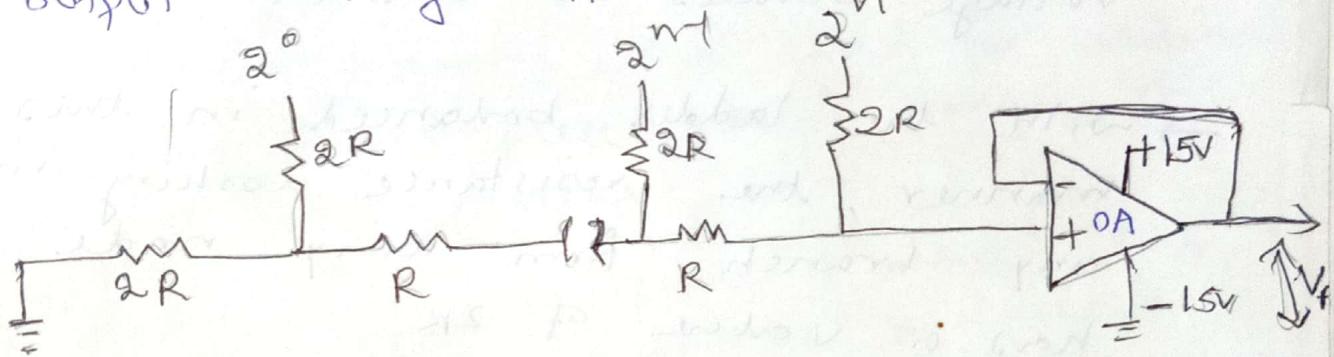
Ex: 12.5

What is the full scale output voltage of the 5 bit ladder in prev example

$$\begin{aligned} V &= 5 + 2.5 + 1.25 + 0.625 + 0.3125 \\ &= +9.6875\text{v} \end{aligned}$$

- To keep the ladder in perfect balance and to maintain symmetry, the output of the ladder should be terminated in a resistance of $2R$.
- Terminating the output of the ladder with a load of $2R$ also ensures that the input resistance to the ladder seen by each of the digital voltage sources is constant.
- with the ladder balanced in this manner, the resistance looking into any branch from any node has a value of $2R$.
- Thus the input resistance seen by any input digital source is $3R$.
- This is a definite advantage over the resistive divider, since the digital voltage sources can now all be designed for the same load.

- The operational amplifier shown in fig below is connected as a unity gain non inverting amplifier.
- In this the output voltage is equal to the input voltage.
- It is thus a good buffer amplifier.
- It will not disturb the ladder output voltage V_A .

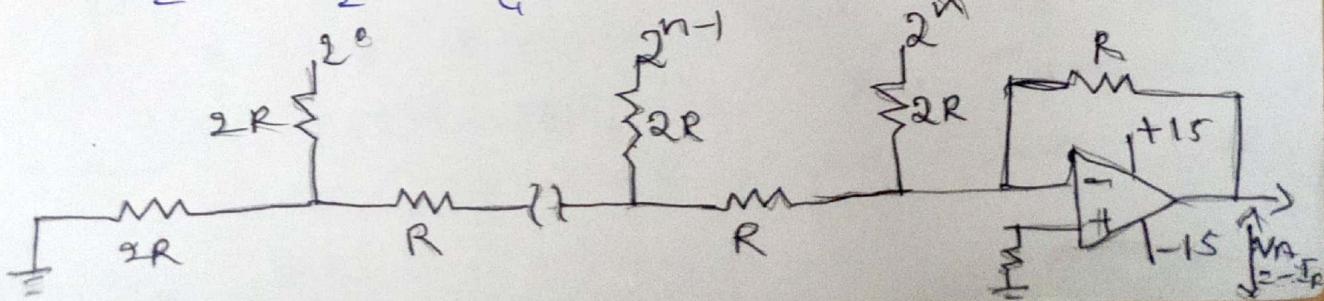


- Connecting an OA with a feedback resistor as shown below results in an amplifier that acts as an inverting current to voltage amplifier.

→ Output voltage $V_A = (-I) \times R$.

$$V_A = (-R) \left(\frac{v}{2R} + \frac{v}{4R} + \dots \right)$$

$$= -\frac{v}{2} - \frac{v}{4} - \dots$$

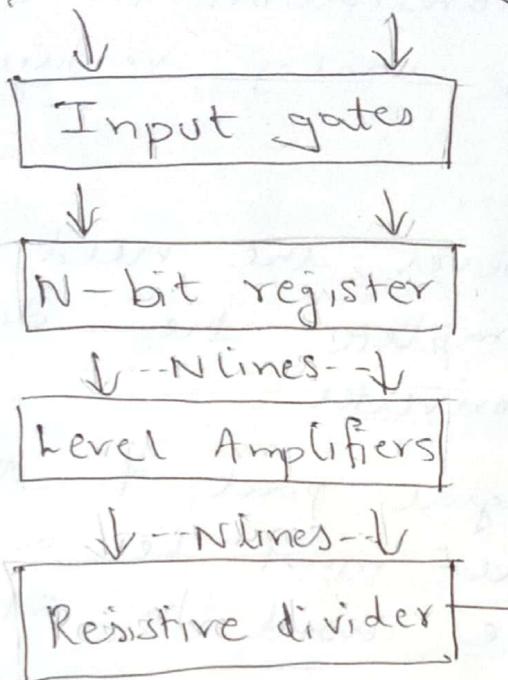


12.3 D/A converters

- Either the resistive divider or the ladder can be used as the basis for a digital to analog (D/A) converter.
- It is in the resistive network that the actual translation from a digital signal to an analog voltage takes place.
- There is however, the need for additional circuitry to complete the design of the D/A converter.
- As an integral part of the D/A converter there must be a register that can be used to store the digital information.
- This reg could be any one of the many types discussed previously.
- The simplest register is formed by use of RS flip flops, with one flip flop per bit.
- There must also be level amplifiers between the register and the resistive network to ensure that the digital signals presented to the network are all of the same level and are constant.

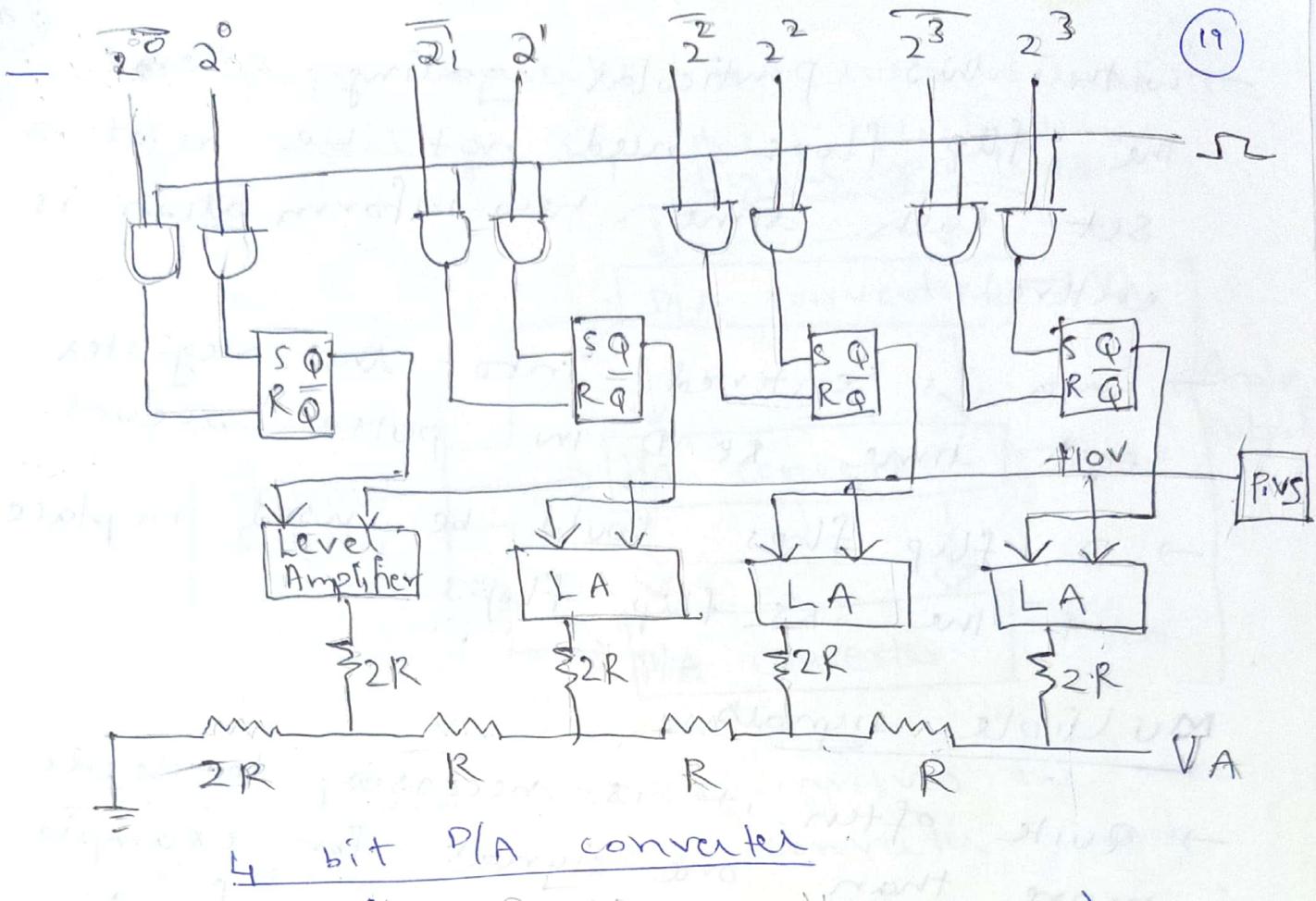
→ Finally, there must be some form of gating on the input of the register such that the flip flops can be set with proper information from the digital system. (18)

Digital input data



→ Expanding the block diagram shown above and drawing the complete schematic for a 4 bit D/A converter, we can recognize that the resistor network used is of ladder type.

→ The level amplifiers each have two inputs : one input is the +10V from the precision voltage source and the other is from a flip flop.



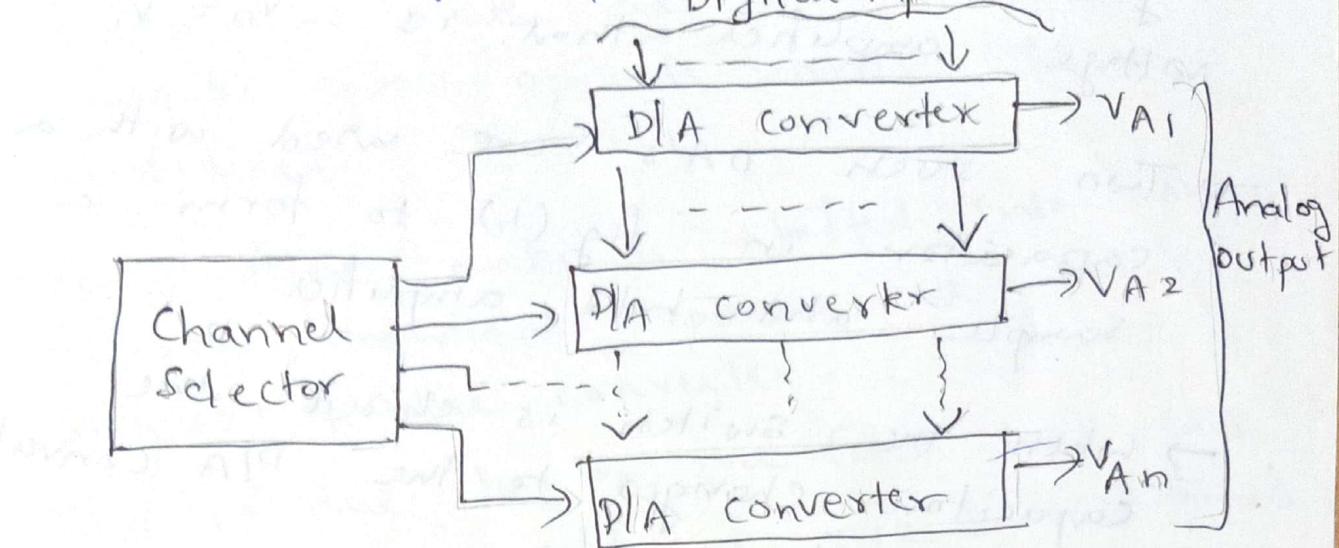
- The amplifiers work in such a way that when the input from a flip flop is high, the output of the amplifier is at +10V.
- When the input from the flip flop is low, the output is 0V.
- The four flip flops form the register necessary for storing the digital information.
- The flip flop on the right represents the msB, and the flip flop on the left represents the lsB.
- Each flip flop is a simple RS latch.

- with this particular gating scheme, the flip flops need not be reset or set each time new information is entered.
- Data is entered into the register each time READ IN pulse occurs.
- D flip flops could be used in place of the RS flip flops.

Multiple signals:

- quite often it is necessary to decode more than one signal - for example the x and y co-ordinates for a plotting board.
- In this event, there are two ways in which to decode the signals.
- The first and most obvious method is simply to use one D/A converter for each signal.
- This method has the advantage that each signal to be decoded is held in its register and the analog output voltage is then held fixed.
- The digital input lines are connected in parallel to each converter.

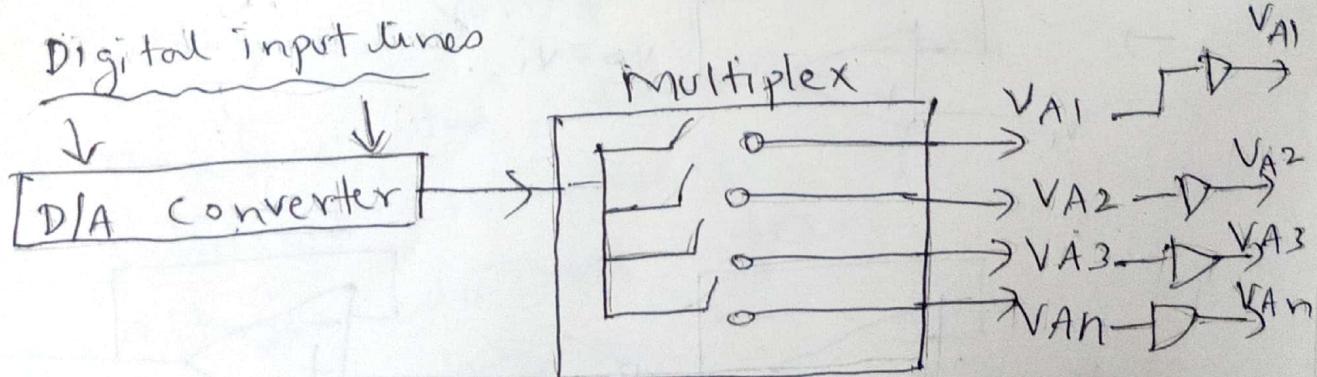
→ The proper converter is then selected for decoding by the select lines. 21



→ The second method involves the use of only one D/A converter and switching its output.

→ This is called multiplexing.

→ The disadvantage here is that the analog output signal must be held between sampling periods, and the outputs must therefore be equipped with sample and hold amplifiers.



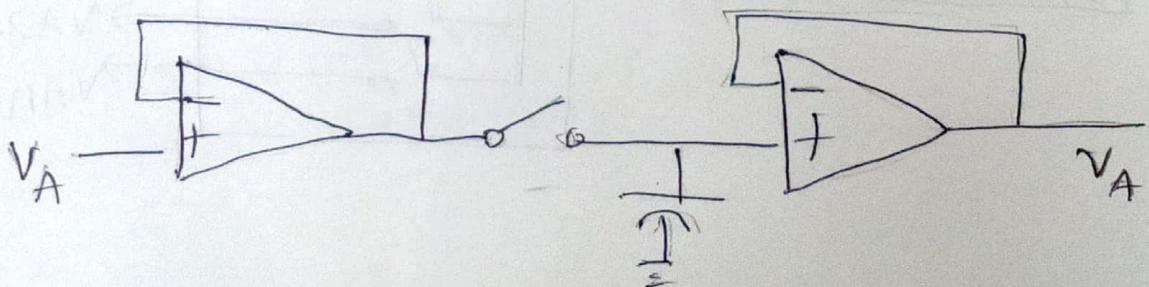
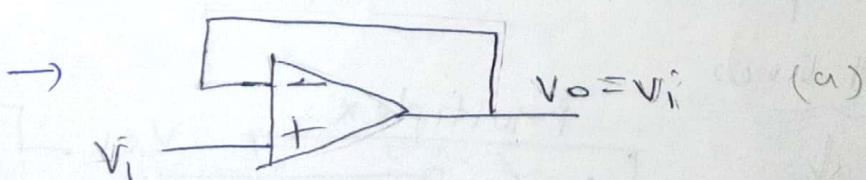
→ An operational amplifier as shown in fig(a) is a unity gain non-inverting voltage amplifier - that is $V_o = V_i$.

→ Two such OA's are used with a capacitor in fig(b) to form a sample and hold amplifier.

→ When the switch is closed, the capacitor charges to the D/A converter output voltage.

Now → When the switch is opened, the capacitor holds the voltage level until the next sampling time.

→ The operational amplifier provides a large input impedance so as not to discharge the capacitor appreciably and at the same time offers gain to drive external circuits.



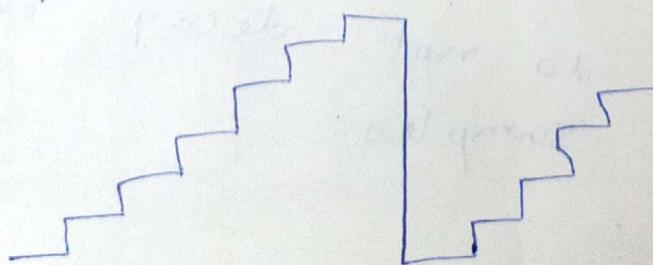
- when the D/A converter is used in conjunction with a multiplexer, the maximum rate at which the converter can operate must be considered.
- Each time data is shifted into the register, transients appear at the output of the converter.
- This is due to the fact that each flip flop has different rise & fall times.
- Thus a setting time must be allowed between shifting into the register and the time the analog voltage is read out.
- This setting time is the main factor in determining the maximum rate of multiplexing.
- The capacitors on the sample and hold amplifiers are not capable of holding a voltage indefinitely.
- Therefore the sampling rate must be sufficient to ensure that these do not decay appreciably between samples.

D/A converter testing :

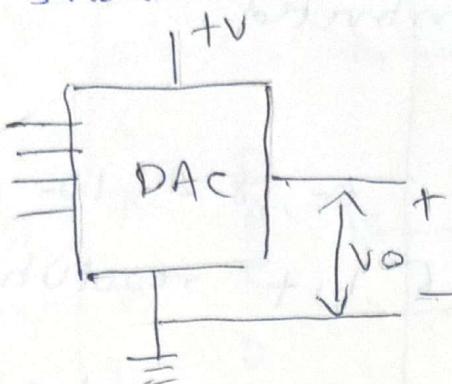
(24)

- Two simple but important tests that can be performed to check the proper operation of the D/A converter are (1) steady state accuracy test (2) monotonicity test.

- (1) Steady state accuracy test involves setting a known digital number in the input register, → measuring the analog output with an accurate meter → then comparing with theoretical value.
- (2) Monotonicity means checking that the output voltage increases regularly as the input digital signal increases.
 - This can be accomplished by using a counter as the digital input signal and observing the analog output on an oscilloscope.
 - For proper monotonicity, the output waveform should be a perfect staircase waveform as shown below.



→ A D/A converter can be regarded as (25)
a logic block having numerous digital
inputs and a single analog output.
as shown below.

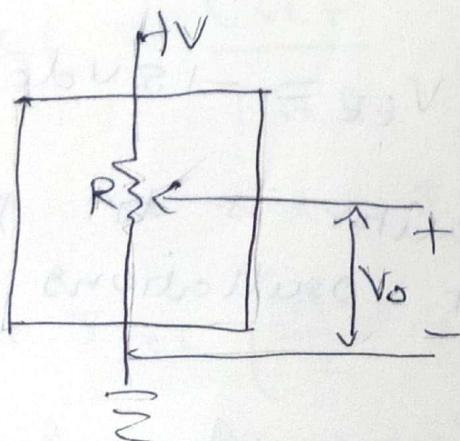


→ we can compare this logic block
with the potentiometer.

→ The analog output voltage of the D/A
converter is controlled by the digital
input signals.

→ while the analog output voltage of the
potentiometer is controlled by mechanical
rotation of the potentiometer shaft.

→ Seen in this fashion, it is easy to
see how a D/A converter could be
used to generate a voltage waveform.



Available D/A converters:

- D/A converters are readily obtainable commercial products.
- Each unit is constructed in a single package.
- Available units are 6-, 8-, 10- & 12-bit resolution up to 16 bit resolution.
- An inexpensive & very popular D/A converter is the DAC0808, an 8 bit D/A converter, from National semiconductor.
- DAC0808 is connected to provide a full scale output voltage of $V_o = +10 \text{ Vdc}$ when all 8 digital inputs are 1's
- If the 8 digital inputs are all 0's ($I_{D0} \approx 0$) the o/p $V_o = V_o = 0 \text{ Vdc}$.

Circuit details:

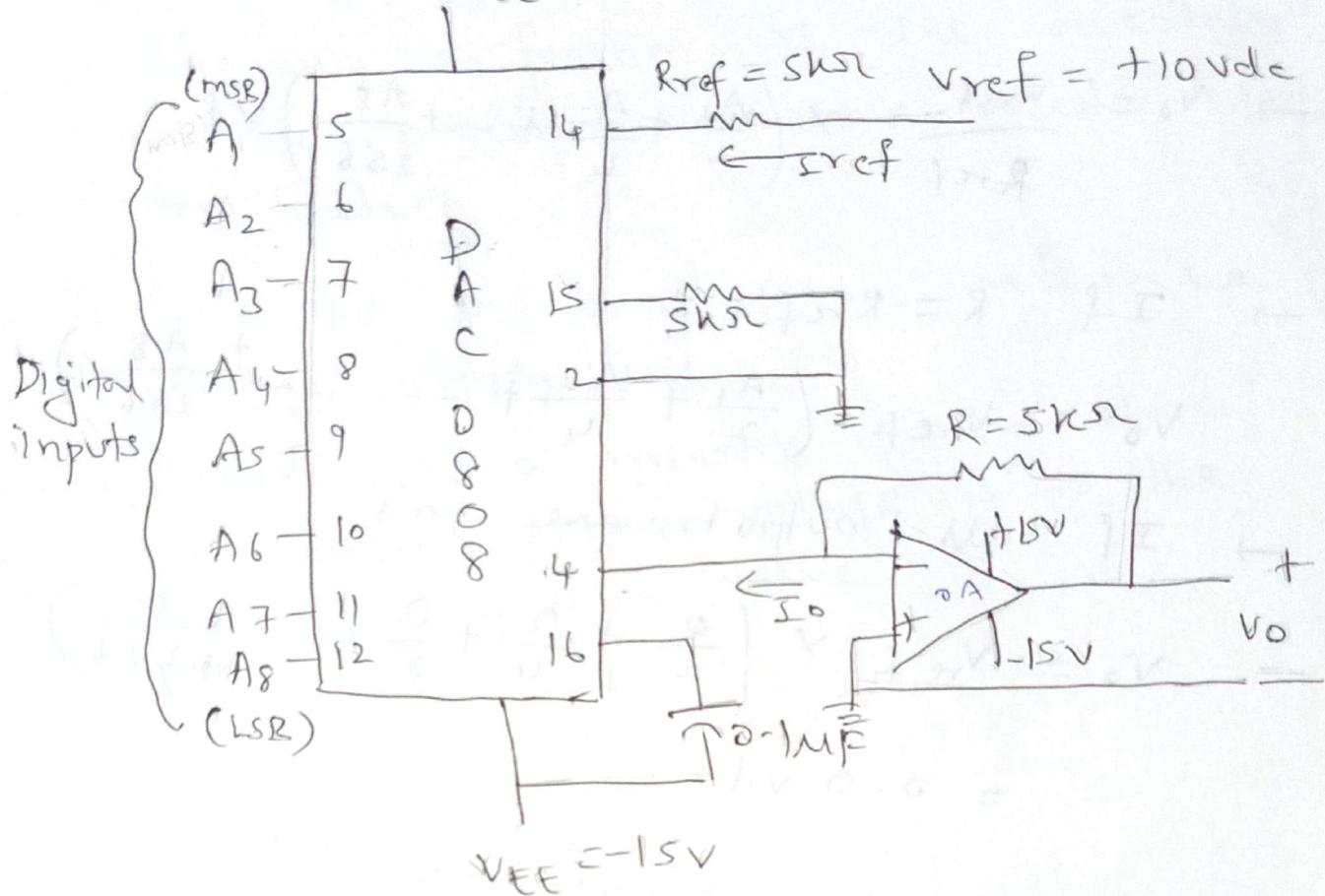
- Two dc power supply voltages are required for the DAC0808
- $V_{CC} = +5 \text{ Vdc}$ $V_{EE} = -15 \text{ Vdc}$.
- The 0.1MF capacitor is to prevent unwanted circuit oscillations

(27)

→ Pin 2 is GND

→ Pin 15 is also referenced to ground through a resistor.

$$V_{cc} = +5V_{dc}$$



→ The output of the D/A converter on pin 14 has a very limited voltage range
(+0.5 to -0.6 V).

$$\text{Output Range} = \left(\frac{V_{cc}}{2^{15}} \right) \times (V_{ee}) =$$

→ Output current = I_o .

→ min current = 0.0 mA, max current = I_{ref} .

$$I_{ref} = \frac{V_{ref}}{R_{ref}}$$

→ Output current I_o is given by

$$I_o = I_{ref} \left(\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \dots + \frac{A_8}{256} \right)$$

where $A_1 - A_8 \rightarrow$ are digital voltage levels.

→ The OA is connected as a current to voltage converter. (28)

$$V_o = I_o \times R$$

$$\rightarrow V_o = \frac{V_{ref}}{R_{ref}} \times \left(\frac{A_1}{2} + \frac{A_2}{4} + \dots + \frac{A_8}{256} \right) \times R.$$

→ If $R = R_{ref}$.

$$V_o = V_{ref} \left(\frac{A_1}{2} + \frac{A_2}{4} + \dots + \frac{A_8}{256} \right)$$

→ If all outputs are 0's

$$V_o = V_{ref} \times \left(\frac{0}{2} + \frac{0}{4} + \frac{0}{8} + \dots + \frac{0}{256} \right)$$

$$= 0.0 \text{ Vdc.}$$

→ If all the outputs are 1's

$$V_o = V_{ref} \times \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \dots + \frac{1}{256} \right)$$

$$= (V_{ref}) \times \left(\frac{255}{256} \right) = 0.996 V_{ref}.$$

→ For this ex $V_{ref} = +10V$

→ The output voltage is seen to have a range between 0.0 & +9.96.

D/A accuracy and resolution:

- Accuracy of the D/A converter is primarily a function of the accuracy of the precision resistors used in the ladder.
- and the precision of the reference voltage supply used.
- Accuracy is a measure of how close the actual output voltage is to the theoretical output value.

$$\text{Accuracy} = \frac{\text{Actual Output Voltage} - \text{Theoretical Output Voltage}}{\text{Theoretical Output Voltage}} \times 100\%$$

$$= \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\%$$

$$= \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\% = \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\%$$

$$= \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\% = \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\%$$

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$$= \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\% = \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\%$$

$$= \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\% = \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\%$$

$$= \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\% = \frac{V_{D/A} - V_{D/A, \text{ideal}}}{V_{D/A, \text{ideal}}} \times 100\%$$

→ Resolution defines the smallest increment in voltage that can be discerned → (Recognized - Recognizable increment)

→ Resolution is primarily a function of the number of bits in the digital input signal; that is the smallest increment in output voltage is determined by the LSB.

→ In a 4 bit system using a ladder, LSB weight = $\frac{1}{16}$

→ Smallest increment in $v_g = \frac{1}{16}$ of input voltage

→ if input voltage levels $\rightarrow +16V$

$$\rightarrow \frac{1}{16} \times 16 = 1V$$

→ The smallest increment = 1V

→ Voltage resolution is obtained by multiplying the weight of the LSB by full scale output voltage.

→ If full scale $v_g = +16V$
LSB weight = $\frac{1}{2^4} = \frac{1}{16}$

$$\text{Voltage resolution} = \frac{1}{16} \times 16 = 1V$$

} For
4 bits.

12.8, 12.9 & 12.10

Example 12.8

In Fig 12.16 A₁ is high
 A₂ is high
 A₅ is high
 A₇ is high.

The other digital inputs are all low.
 What is the output voltage V_o

$$V_o = 10 \times \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{32} + \frac{1}{128} \right)$$

$$= 10 \times 0.789 = 7.89 \text{ V}$$

Example 12.9 :

What is the resolution of 9 bit D/A converter which uses a ladder network?
 What is this resolution expressed as percent? If the full scale output voltage of this converter is +5V, what is the resolution in volt.

$$\rightarrow \text{LSB of 9 bit system} - \frac{1}{2^9} = \frac{1}{512}$$

Resolution = 1 part in 512.

$$\begin{aligned} \text{Resolution expressed as percent} & \frac{1}{512} \times 100 \\ & = 0.2 \text{ percent} \end{aligned}$$

$$\text{Resolution in volt} = \frac{1}{512} \times 5 = 10 \text{ mV}$$

Example 12.10 :

How many bits are required at the input of a converter if it is necessary to resolve voltages to 5mv and ladder has +10v full scale?

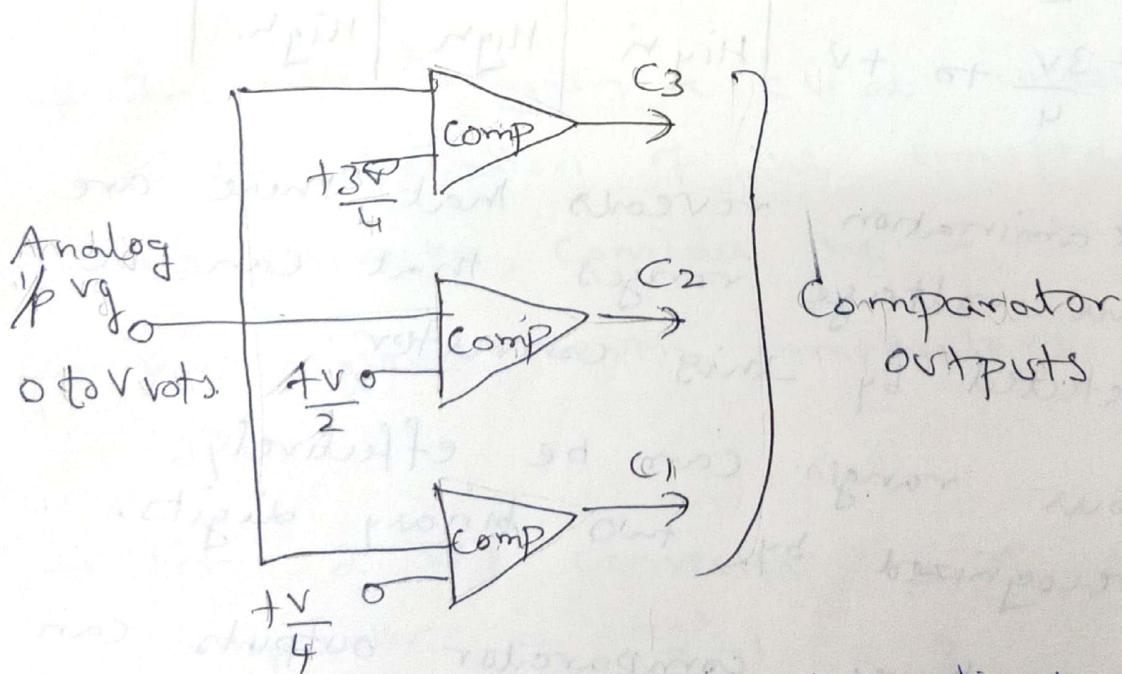
→ LSB of 11 bit system has a resolution of $\frac{1}{2048}$

This would provide a resolution at the output of $\frac{1}{2048} \times 10 = 5\text{mV}$.

(31)

12-5. A/D converter - simultaneous conversion

- The process of converting an analog v_g into an equivalent digital signal is known as analog to digital (A/D) conversion.
- This operation is more complicated than the D/A operation.
- Number of different methods have been developed.
- The simplest of which is probably the simultaneous method.
- The simultaneous method of A/D conversion is based on the use of a number of comparator circuits.
- one such system using three comparator circuits is shown below.



- The analog signal to be digitized serves as one of the inputs to each comparator.

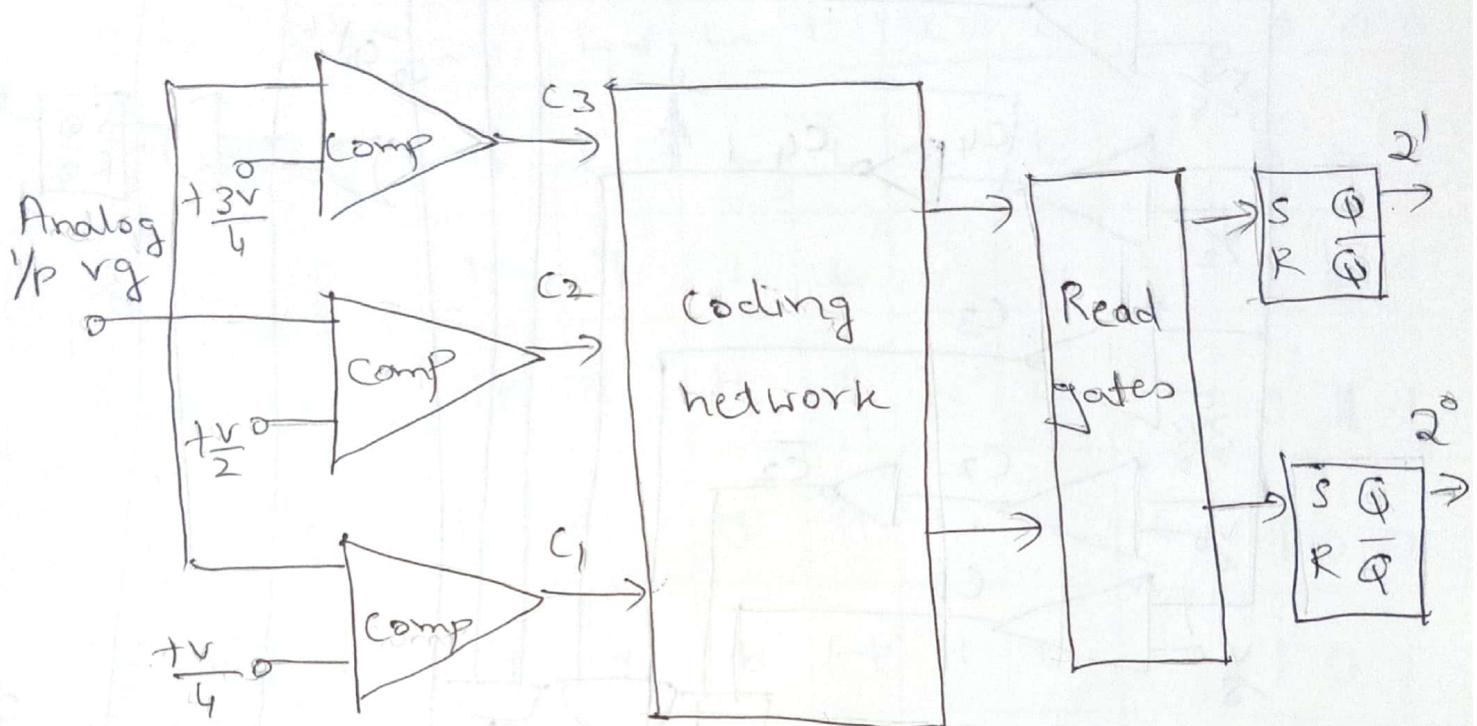
- The reference voltages used are $+ \frac{V}{4}$, $+ \frac{V}{2}$ and $+ \frac{3V}{4}$.
- The system is then capable of accepting an analog input voltage between 0 & V .
- If the analog input signal exceeds the reference voltage to any comparator, that comparator turns on.
- The Comparator output levels for the various ranges of input voltages are summarised in the table below.

Input voltage	comparator output		
	C ₁	C ₂	C ₃
0 to $+ \frac{V}{4}$	Low	Low	Low
$+ \frac{V}{4}$ to $+ \frac{V}{2}$	High	Low	Low
$+ \frac{V}{2}$ to $+ \frac{3V}{4}$	High	High	Low
$+ \frac{3V}{4}$ to $+ V$	High	High	High

- Examination reveals that there are four voltage ranges that can be detected by this converter.
- Four ranges can be effectively recognized by two binary digits.
- The three comparator outputs can then be fed into a coding network to provide 2 bits which are equivalent to the input analog voltage.

→ The bits of the coding network can then be entered into a flip flop register for storage.

→ The complete block diagram for such an A/D converter is shown below



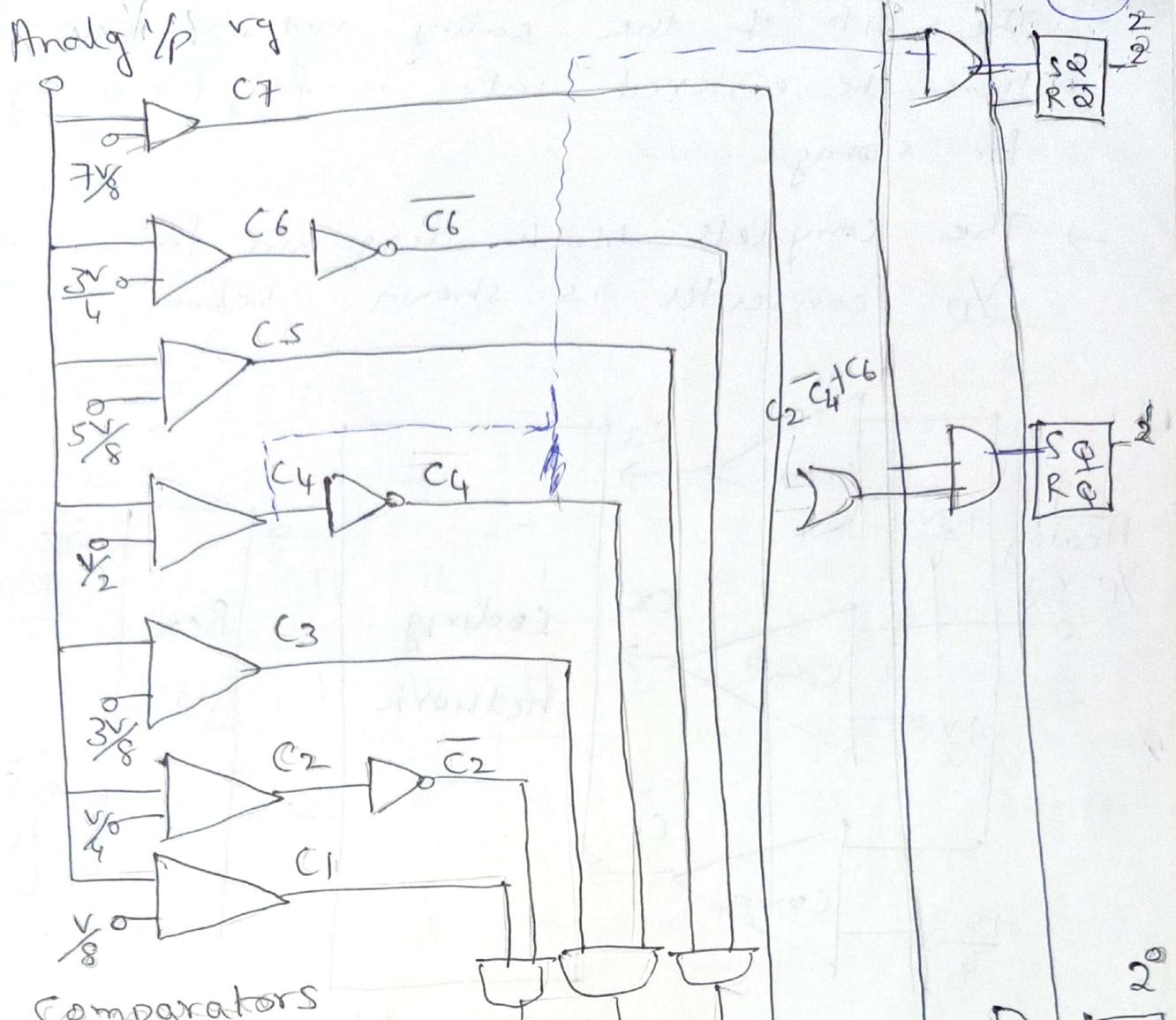
2-bit simultaneous A/D converter

→ In order to gain a clear understanding of the operation of the simultaneous A/D converter, consider the 3 bit converter.
→ we require seven comparators.

$$2^n - 1$$

→ For 2 bit converter no. of comparators = $2^2 - 1 = 3$

→ For 3 bit no of comparators = $2^3 - 1 = 7$



→ The encoding matrix must accept seven input levels & encode them into 3 bit binary numbers.

→ The 2^2 bit is easiest to determine since it must be high whenever C_4 is high. $2^2 = C_4 \oplus$

$$\rightarrow 2^1 = C_2 \bar{C}_4 + C_6$$

$$\rightarrow 2^0 = C_1 \bar{C}_2 + C_3 \bar{C}_4 + C_5 \bar{C}_6 + C_7$$

→ the operation of the encoding matrix can be most easily understood by examination of the table of outputs.

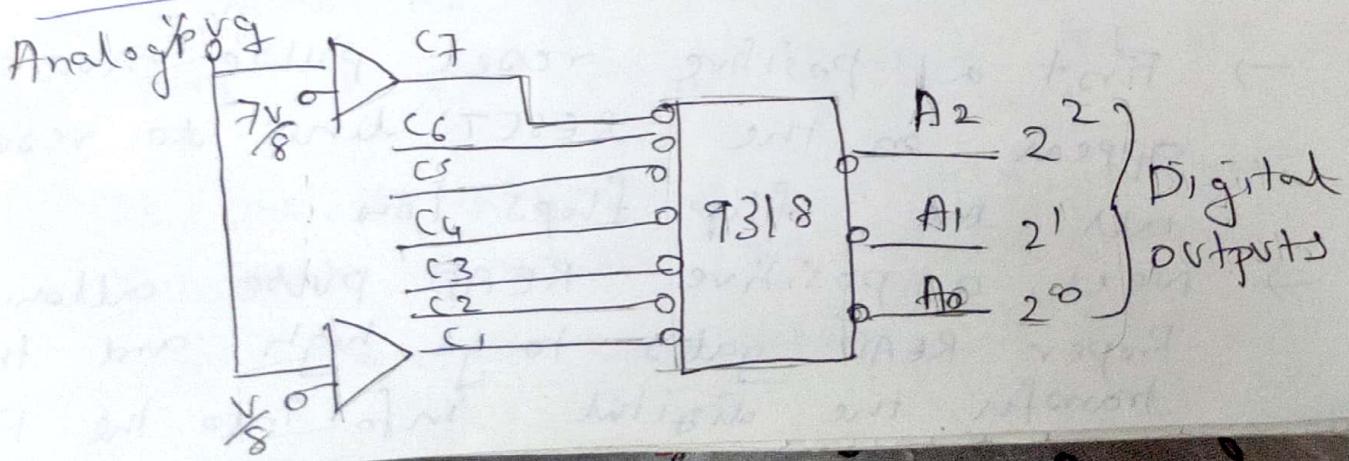
Input voltage	comparator o/p							Binary output 2 2 1 2 0
	$c_1 \cdot c_2$	c_3	$c_4 \cdot c_5$	$c_6 \cdot c_7$	$c_1 \cdot c_2$	c_3	$c_4 \cdot c_5$	
0 to $\frac{V}{8}$	H	H	L	L	L	L	L	0 0 0
$\frac{V}{8}$ to $\frac{V}{4}$	H	L	L	L	L	L	L	0 0 1
$\frac{V}{4}$ to $\frac{3V}{8}$	H	H	L	L	L	L	L	0 1 0
$\frac{3V}{8}$ to $\frac{V}{2}$	H	H	H	L	L	L	L	0 1 1
$\frac{V}{2}$ to $\frac{5V}{8}$	H	H	H	H	L	L	L	1 0 0
$\frac{5V}{8}$ to $\frac{3V}{4}$	H	H	H	H	H	L	L	1 0 1
$\frac{3V}{4}$ to $\frac{7V}{8}$	H	H	H	H	H	H	L	1 1 0
$\frac{7V}{8}$ to V	H	H	H	H	H	H	H	1 1 1

- The transfer of data from the encoding matrix into the register must be carried out in two steps.
- First a positive reset pulse must appear on the RESET line to reset all the flip flops low.
- Next, a positive READ pulse allows the proper READ gates to go high and thus transfer the digital info into the FF.

→ A convenient application for a 9318 priority encoder is to use it to replace all the digital logic.

- The inputs $c_1, c_2 \dots c_7$ must be TTL compatible. (diagram below)
- Because of its speed it is also called as a flash converter.
- The Motorola MC10318 is an example of an 8 bit flash A/D converter.
- The input has 256 parallel comparators.
- The input has 256 parallel comparators connected to a precision voltage divider.
- The flash A/D converter is capable of operation with a 25 MHz clock.
- Possible applications include radar, signal processing, video displays, high speed instrumentation, television broadcasting.

9318 priority encoder



12-10 A/D accuracy & resolution

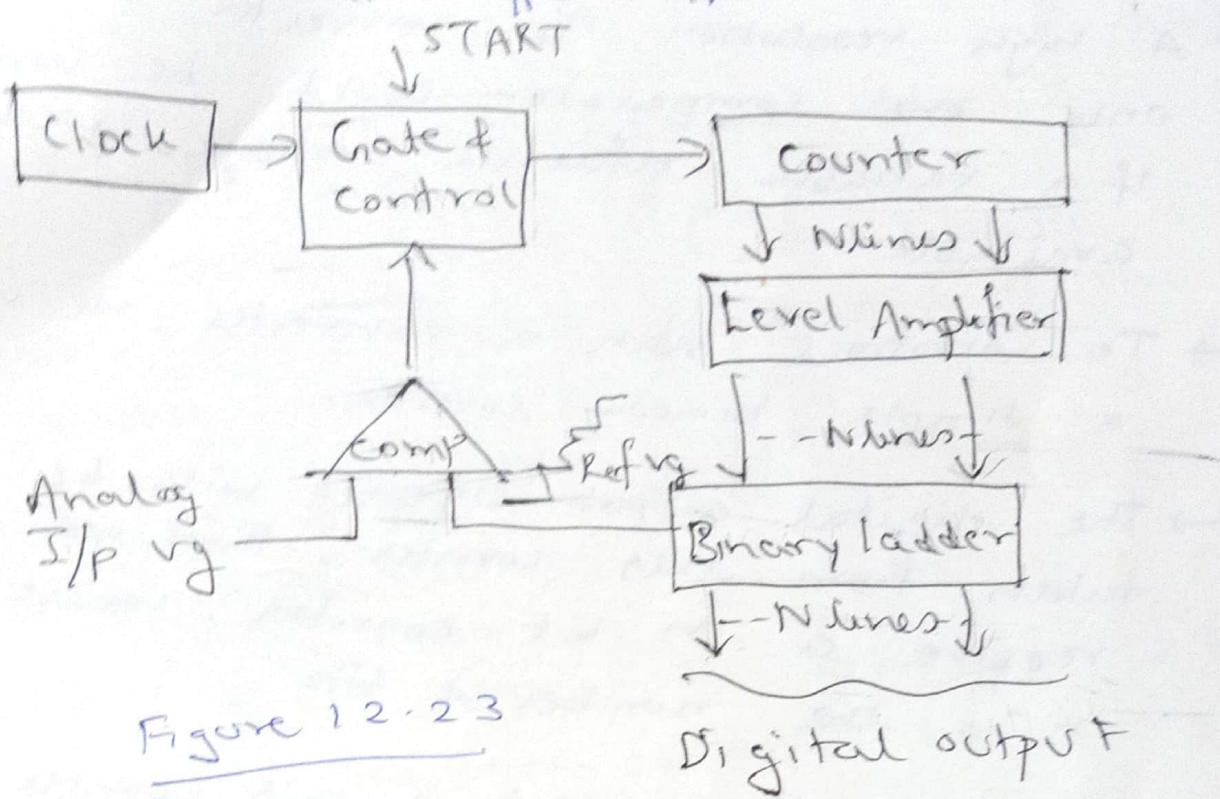
- since A/D converter is a closed loop system involving both analog & digital systems, the overall accuracy must include errors from both the analog & digital positions.
- In determining the overall accuracy it is easiest to separate the two sources of error.
- If we assume that all the components are operating properly, the source of digital error is simply determined by the resolution of the system.
- In digitizing an analog v_g , we are trying to represent a continuous analog v_g by an equivalent set of digital numbers.
- The simple fact that the ladder voltage leads to digital error in the system.
- This error is often called quantization error and it can be commonly ± 1 bit.
- If the comparator is centred, as with continuous converters, the quantization error can be ~~can~~ made $\pm \frac{1}{2}$ LSB.

- The main source of analog error is in the comparator.
- The error in the comparator is centred around variations in the dc switching point.
- The dc switching point is the difference between the input voltage levels that cause the output to change state.
- Variations in switching are due primarily to offset, gain and linearity of the amplifier used in the comparator.
- These parameters usually vary slightly with input voltage levels & quite often with temperature.
- It is these changes which give rise to the analog error in the system.
- An important measure of converter performance is given by differential nonlinearity, which is a measure of the variation in voltage step size that causes the converter to change from one state to next.
- It is usually expressed as a percent of the average step size.

12.6 A/D converter - counter method

- A high resolution A/D converter using only one comparator could be constructed if a variable reference voltage were available.
- To construct such a converter, we use a simple binary counter.
- The digital output signals will be taken from this counter, thus we require a n bit counter, where n is the number of bits.
- Connect the output of this counter to a standard binary ladder to form a simple D/A converter.
- If a clock is now applied to the input of the counter, the output of the binary ladder is the familiar staircase waveform.
- This waveform is exactly the reference voltage signal we would like to have for the comparator.
- With a minimum of gating and control circuitry, this simple D/A converter can be changed into the desired A/D converter.

→ The figure below shows one block diagram for a counter type A/D converter. (38)



→ The operation of the counter is as follows.

→ First the counter is reset to all 0's.

→ Then when a convert signal appears on the START line, the gate opens and clock pulses are allowed to pass through to the input of the counter.

→ The counter advances through its normal binary count sequence, and the staircase waveform is generated at the output of the ladder.

→ This waveform is applied to one side of the comparator, and the analog input V_g is applied to the other side.

→ When the reference voltage equals (or exceeds) the input analog voltage, the gate is closed, the counter stops and the conversion is complete.

(39)

→ The number stored in the counter is now the digital equivalent of the analog input voltage.

→ This can be considered as a closed loop system.

→ An error signal is generated at the output of the comparator by taking the difference between the analog input signal and the feedback signal.

→ The error is detected by the control circuit, and the clock is allowed to advance the counter.

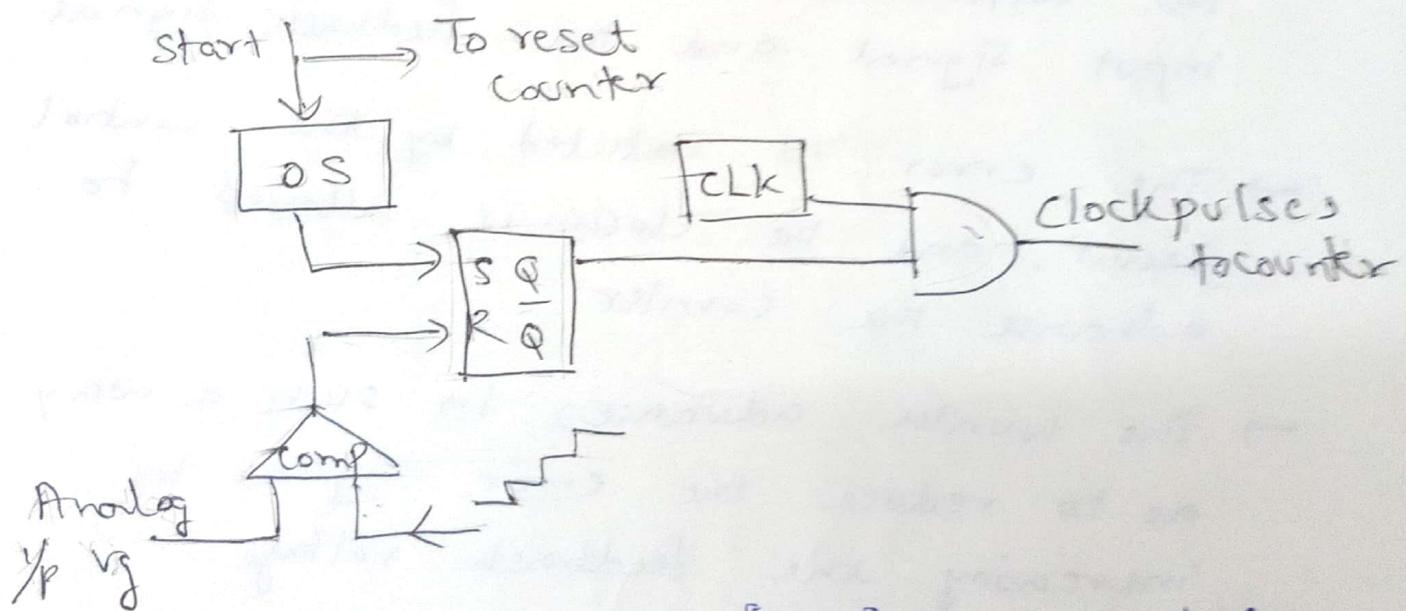
→ The counter advances in such a way as to reduce the error signal by increasing the feedback voltage.

→ When the error is reduced to zero, the feedback voltage is equal to the analog input signal, the control circuitry stops the clock from advancing the counter, and the system comes to rest.

(60)

→ Figure below shows one method of implementing the control circuitry for the converter.

- A conversion is initiated by the receipt of a START signal.
- The positive edge of the START pulse is used to reset all the flip flops in the counter & to trigger the one shot.
- The output of one shot sets one control flip flop, which makes the AND gate true & allows clock pulses to advance the counter.



→ with the control flip flop set, the counter advances through its normal count sequence until the staircase voltage from the ladder is equal to the analog input voltage.

Example 12.11

Suppose that the converter shown in figure 12.23 (page 38) is an 8 bit converter driven by 500 kHz clock.

Find (a) the maximum conversion time

(b) the average conversion time

(c) the maximum conversion rate.

→ (a) 8 bit converter $- 2^8 = 256$ counts.

→ with a 500 kHz clock, the counter advances at the rate of 1 count each 2 ms.

→ To advance 256 counts requires

$$256 \times 2 \times 10^{-6} = 512 \times 10^{-6} = 512 \text{ ms.}$$

(b) Average conversion time is one half the maximum conversion time.

$$\frac{1}{2} \times 0.512 \times 10^{-3} = 0.256 \text{ ms.}$$

(c) The maximum conversion rate is determined by the longest conversion time. since the converter has a maximum conversion time of 0.512 ms.

→ It is capable of making at least

$$\frac{1}{(0.512 \times 10^{-3})} = 1953 \text{ conversions per second.}$$

→ At this time, the comparator "P" changed state, generating a positive pulse which resets the control flip flop.

→ Thus the AND gate is closed and counting ceases.

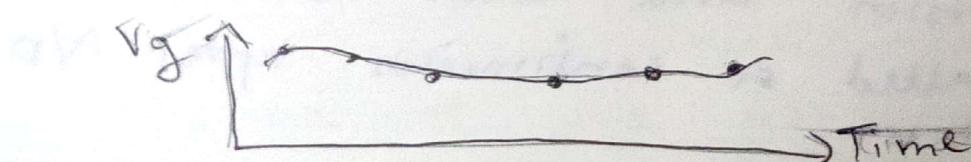
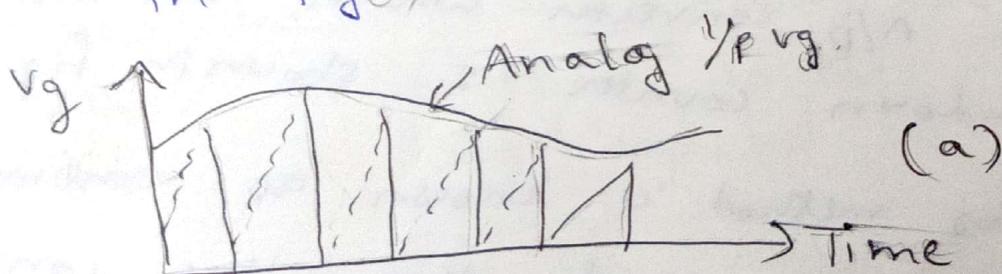
→ The counter now holds a digital number which is equivalent to the analog input voltage.

→ The converter remains in this state until another conversion signal is received.

→ The converter can be used to digitize the signal as shown in fig(a).

→ The analog input signal can be reconstructed from the digital information by drawing straight lines from each digitized point to the next.

→ Such a reconstruction is shown in fig(b) below.

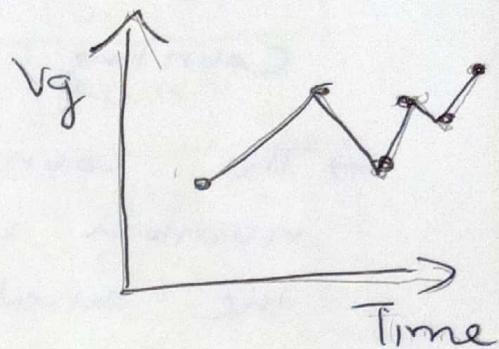
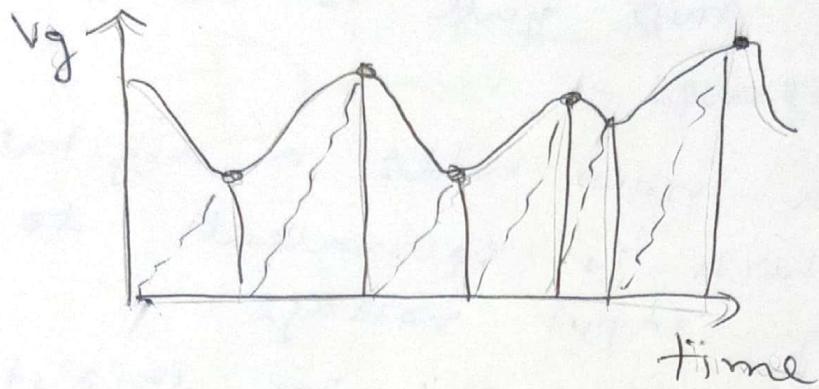


(b)

Problem
12-11

12.7 Continuous A/D conversion

→ An obvious method for speeding up the conversion of the signal is shown below.



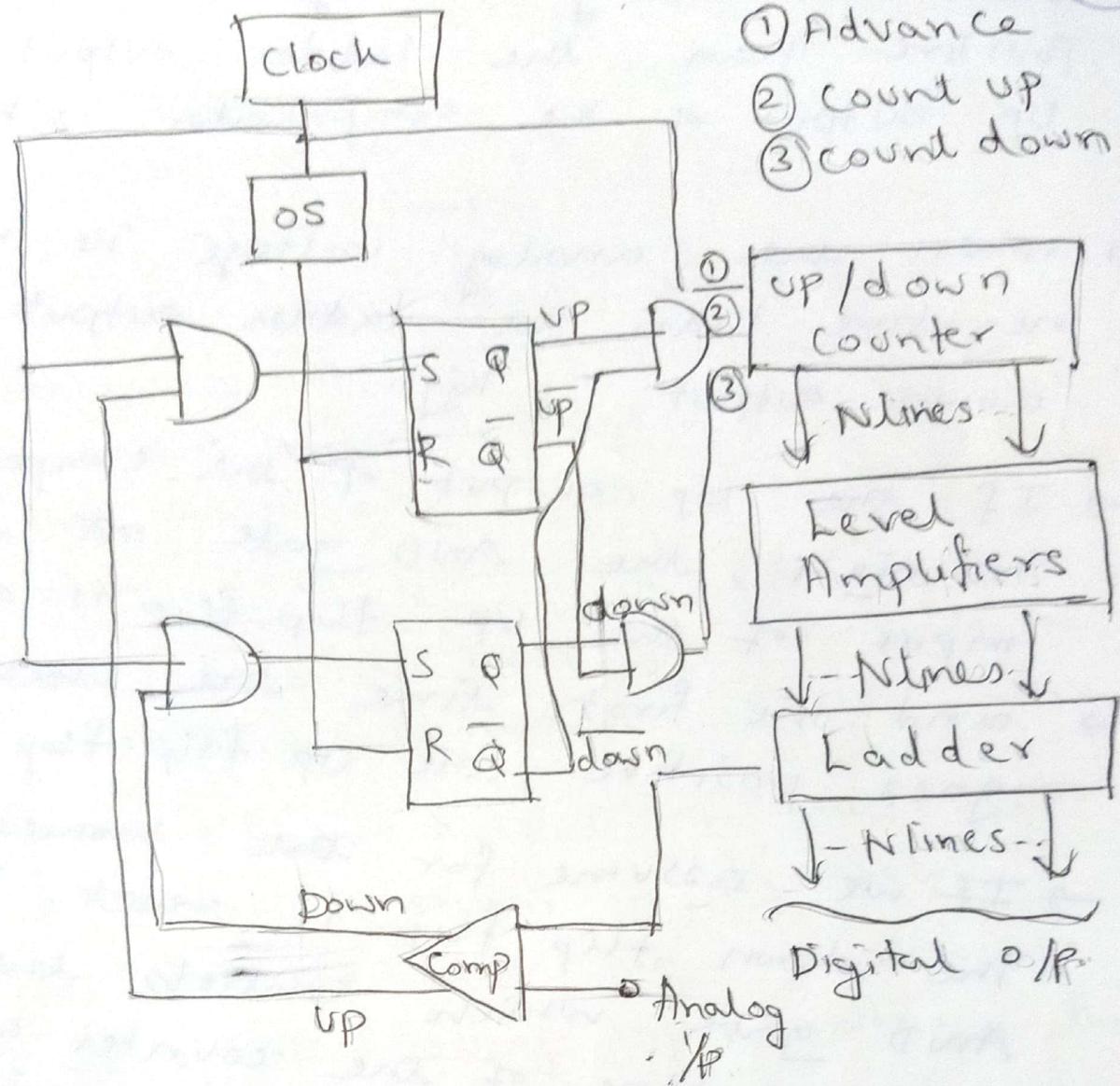
→ we need to eliminate the need for resetting the counter each time a conversion is made.

→ counter has to be capable of counting either up or down.

→ There is however the need for additional circuitry, since we must decide whether to count up or down by examining the output of the comparator.

→ An A/D converter which uses an up-down counter is shown in fig.

→ This method is known as continuous conversion and thus the converter is called a continuous type A/D converter.



- The D/A portion of this converter is the same as that discussed previously.
- only exception being the counter.
- It is an up-down counter and has the up and down count control lines in addition to the advance line at its input.
- The output of the ladder is fed into a comparator which has two o/p's instead of one as before.

→ when the analog voltage is more positive than the ladder output, the up output of the comparator is high. (44)

→ when the analog voltage is more negative than the ladder output, the down output is high.

→ If the up output of the comparator is high, the AND gate at the input of the up flip flop is open

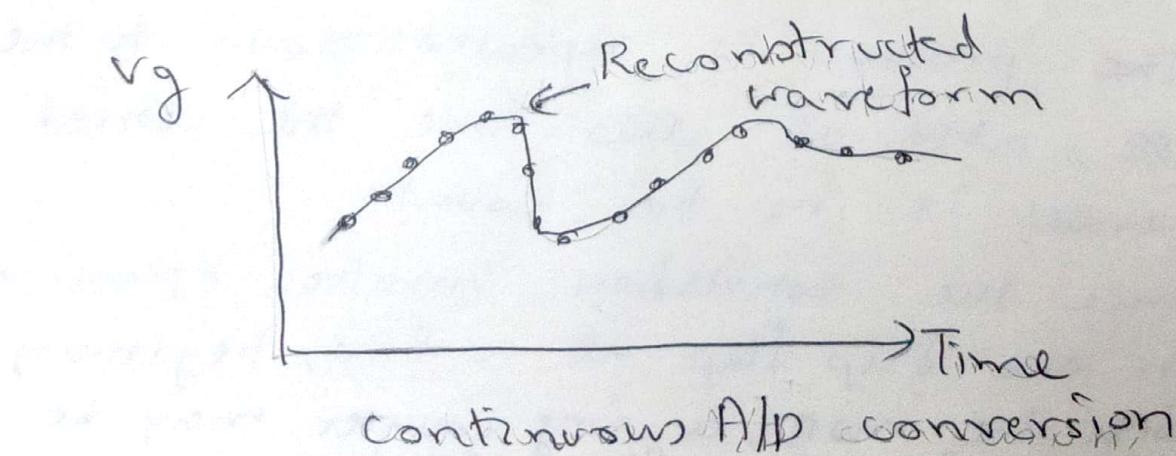
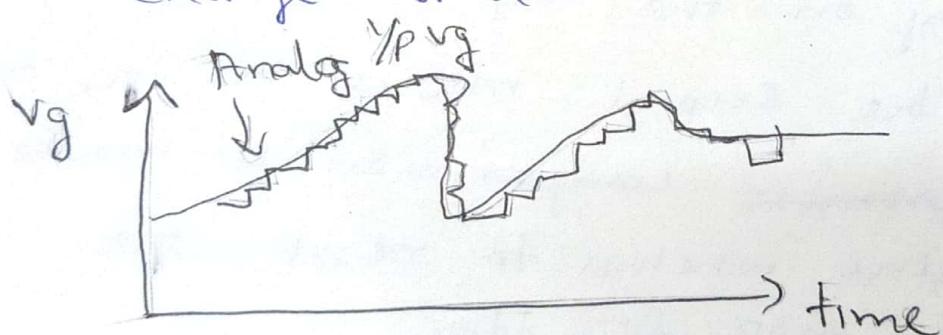
→ and the first time the clock goes positive, the up flip flop is set.

→ If we assume for the moment that the down flip flop is reset, the AND gate which controls the count up line of the counter will be true and the counter will advance one count.

→ The counter can advance only one count since the output of the one shot resets both the up and down flip flops just after the clock goes low.

→ This can be considered as one count up conversion cycle.

- (4.5)
- As long as the up line out of the comparator is high, the converter continues to operate one conversion cycle at a time.
 - At the point where the ladder voltage becomes more positive than the analog input voltage, the up line of the comparator goes low and the down line goes high.
 - The converter then goes through a count down conversion cycle.
 - A waveform typical of this type of converter is shown in fig below.
 - we can see that the converter is capable of following input voltages that change at a much faster rate.



12.8 A/p Techniques :

- There are a variety of methods for digitizing analog signals
- successive approximation :
- If multiplexing is required, the successive-approximation converter is most useful.
- The block diagram for this type of converter is shown in Fig below.
- The converter operates by successively dividing the voltage ranges in half.
- The counter is first reset to all 0's and the msB is then set.
- The msB is then left in or taken out depending on the output of the comparator.
- Then the second msB is set in, and a compromise comparison is made to determine whether to reset the second msB flip flop.
- The process is repeated down to the LSB, and at this time the desired number is in the counter.
- Since the conversion involves operating on one flip flop at a time, beginning with the msB, a ring counter may be used for flip flop selection.