Part - B Asynchronous Sequential circuit

→ Asynchronous sequential circuit also called event driven circuit does not have any clock to trigger change of state.

→ state changes are triggered by change in input signal.

11-8 Analysis of asynchronous sequential circuit.

→ memory is the most important element in Sequential circuit.

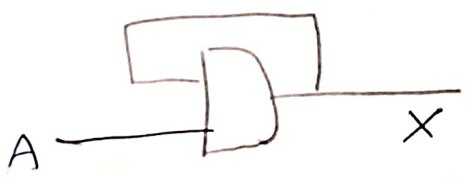
→ In synchronous system we use clock driven flip flops which we cannot use here

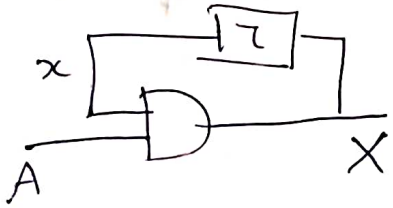
→ This is done through feedback similar to basic latch portion of a flip flop.

→ First we discuss how a two input AND gate and two input NAND gate behave with output fed back to one of the input.

AND Gate:

→ The two input AND gate with output fed back as one input is shown below





x \ A	0	1
0	0	0
1	0	1

$X = x \cdot A$

→ The circuit can be redrawn that includes the effect of propagation delay of the gate (τ)

→ τ → Finite time after which is a gate reacts to its input.

→ If x is current output obtained following logic relation & x is the feedback output we write

$$x = X(t - \tau).$$

→ The truth table is also called state table and each location in k map a state of asynchronous sequential ckt.

→ The encircled states indicate stable condition of the circuit.

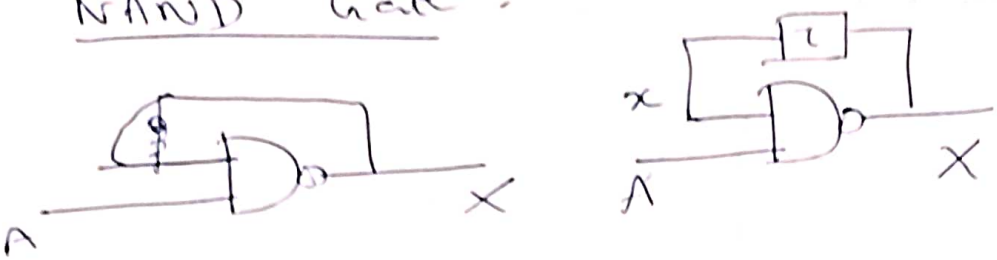
→ $A = 0 \quad x = 0$ then $X = x \cdot A = 0 \cdot 0 = 0$

→ After time $t = \tau$ x takes the value of X

→ $A = 0, \; x = 0$ represents a stable state and is encircled.

→ similarly $x = 0, \; A = 1$ / $x = \phi \quad A = 1$ → stable state

NAND Gate :



x \ A	0	1
0	1	1
1	1	0

$X = \overline{x \cdot A}$

$x = 0 \quad A = 0 \quad X = 1$

$x = 1 \quad A = 0$

→ For $A = 1$ there is no stable state

→ $x = X'$ for both $x = 0$ & $x = 1$

→ Thus there is oscillation between

$x = 0 \quad A = 1$ & $x = 1 \quad A = 1$ state

$x = 0 \quad A = 1 \quad X = 1$

$x = 1 \quad A = 1 \quad X = 0$

11 → 0

nand

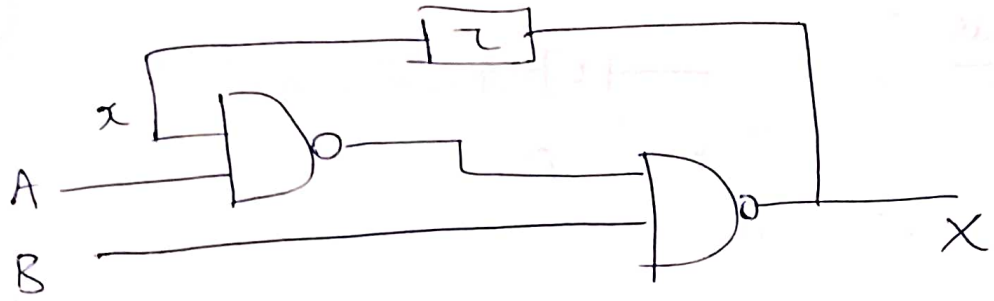
Two input NAND latch :

→ In analysis of sequential circuit there is an important constraint to be followed.

→ Though there can be more than one input feeding the circuit, at a time only one input variable can change.

→ The other input can change only when the circuit is stabilized following the previous input change.

→ If there are two or more output variables only one output variable can change



x \ AB	00	01	11	10
0	1	0	0	1
1	1	0	1	1

→ If $X = x$ the circuit is stable.

→ Arrows show the movements from transient states

→ let us see how input changes effect the output.

Input AB change from 00 to 01 :

→ The circuit moves from $xAB = 100$, a stable position to $xAB = 101$, which is unstable and then moves to $xAB = 001$

→ This is a stable state that has the output 0.

→ Therefore $00 \rightarrow 01$ transition in AB has output X making $1 \rightarrow 0$ transition.

Input AB Changes from 00 to 10 :

→ The circuit moves from stable position $x AB = 100$, to $x AB = 110$.

→ Therefore a $00 \rightarrow 10$ transition in AB does not alter the value of output $x = 1$

→ AB cannot change from 00 to 11 as there will be a finite delay.

→ Thus the transition path of AB is either $00 \rightarrow 01 \rightarrow 11$ or $00 \rightarrow 10 \rightarrow 11$ depending on which of A or B changes earlier.

input AB	state (xAB) transition	output x
$00 \rightarrow 01$	$100 \rightarrow 101 \rightarrow 001$	$1 \rightarrow 0 \rightarrow 0$
$00 \rightarrow 10$	$100 \rightarrow 110$	$1 \rightarrow 1$
$01 \rightarrow 00$	$001 \rightarrow 000 \rightarrow 100$	$0 \rightarrow 1 \rightarrow 1$
$01 \rightarrow 11$	$001 \rightarrow 011$	$0 \rightarrow 0$
$10 \rightarrow 00$	$110 \rightarrow 100$	$1 \rightarrow 1$
$10 \rightarrow 11$	$110 \rightarrow 111$	$1 \rightarrow 1$
$11 \rightarrow 01$	$011 \rightarrow 001$, $111 \rightarrow 101 \rightarrow 001$	$0 \rightarrow 0$, $1 \rightarrow 0 \rightarrow 0$
$11 \rightarrow 10$	$011 \rightarrow 010 \rightarrow 101$, $111 \rightarrow 110$	$0 \rightarrow 1 \rightarrow 1$, $1 \rightarrow 1$

Problems with Async seq ckts:

→ Before we go for the design of asynchronous sequential circuit we will look at a few design related issues.

→ There are non issues in sync ckt.

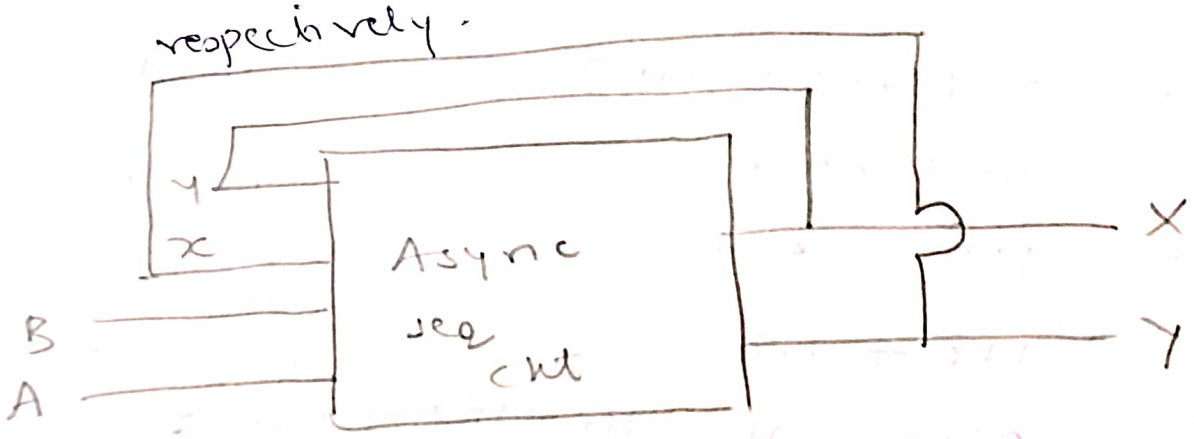
→ Async ckt responds to all the transient values and problems like oscillation, critical race, hazards can cause major problem.

→ Ex :- ckt with two inputs A, B and two outputs x, y.

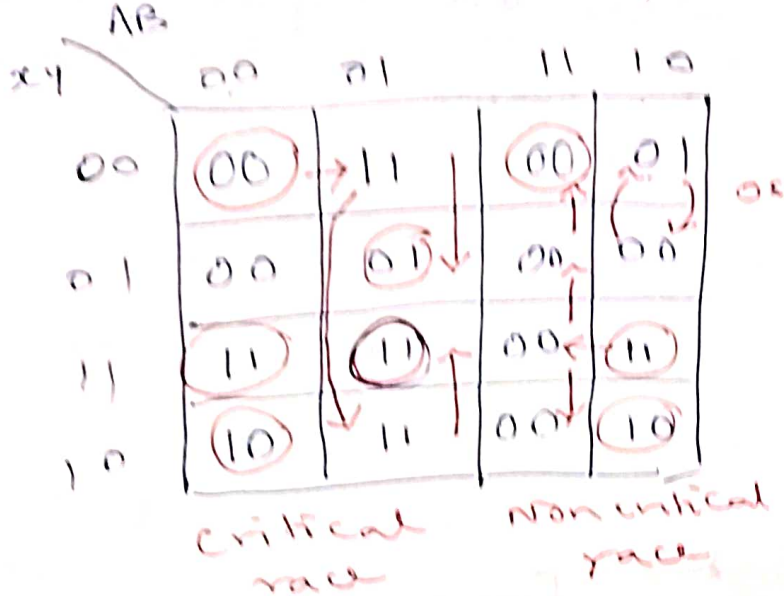
→ Both the outputs are fedback to the input side in the form of x & y but with different prop delays.

→ Thus x, y cannot change simultaneously

→ They change with time delays τ_1 & τ_2 respectively.



→ Truth table → k-map.



Oscillation:

→ $xyAB = 0000$ $x = X$ $y = Y$.

→ AB → 00 to 10. $xyAB = 0010$ $\because XY = 01$

→ This is a transient state because $xy \neq XY$

→ After time t_2 the circuit goes to $xyAB = 0010$.

→ Thus the circuit oscillates between state. 0010 & 0110.

→ output Y oscillates between 0 & 1 with a time gap t_2.

→ In asynchronous sequential circuits for any given input, transitions between two unstable states like these are to be avoided

Critical race:

→ This occurs when an input change tries to modify more than one output.

→ Consider the stable state $xyAB = 0000$.

→ AB changes to 01 ckt moves to $xyAB = 0001$ where $XY = 11$

→ Now depending which of Y_1 and Y_2 is lower. xy moves from 00 to either 01 or 10.

→ Y_1 - lower:

x changes earlier ckt goes to $xyAB = 1001$.

$XY = 11$.

→ Y_2 - lower:

y changes earlier ckt goes to $xyAB = 0101$.

$XY = 01$.

→ Thus depending on prop delays in feedback path, the circuit settles at two different states, generating two different outputs.

→ such a situation is called critical race condition and is to be avoided in asyn seq ckt.

→ Race can be non critical, in which case its presence does not pose any problem for the circuit

→ Stable state $xyAB = 1110$.

→ If AB changes to 11, the circuit goes to $xyAB = 1111$ where output $xy = 00$.

→ Again depending on propogation delays xy becomes either 01 or 10.

→ In both cases the final state is 0011 and output = 00. ~~since~~

→ since the race condition does not lead to two different state it is termed as non-critical race.

Hazards :

→ static & dynamic hazards causes malfunctioning of asyn seq ckt.

→ In circuit with feedback even when these hazards are adequately covered there can be another problem called essential hazard.

→ This occurs when change in input does not reach one part of the circuit while from other part one output fed back to the input side

→ Essential hazard can be avoided by adding delay, may be in the form of additional gates that does not change the logic level.

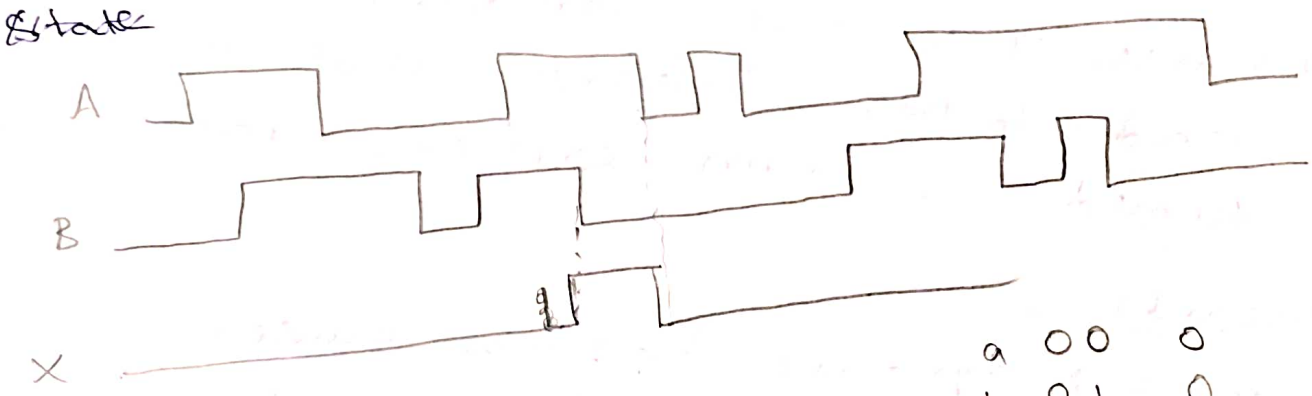
Design of asynchronous sequential ckt:

The problem:

→ Two inputs A & B, one output x

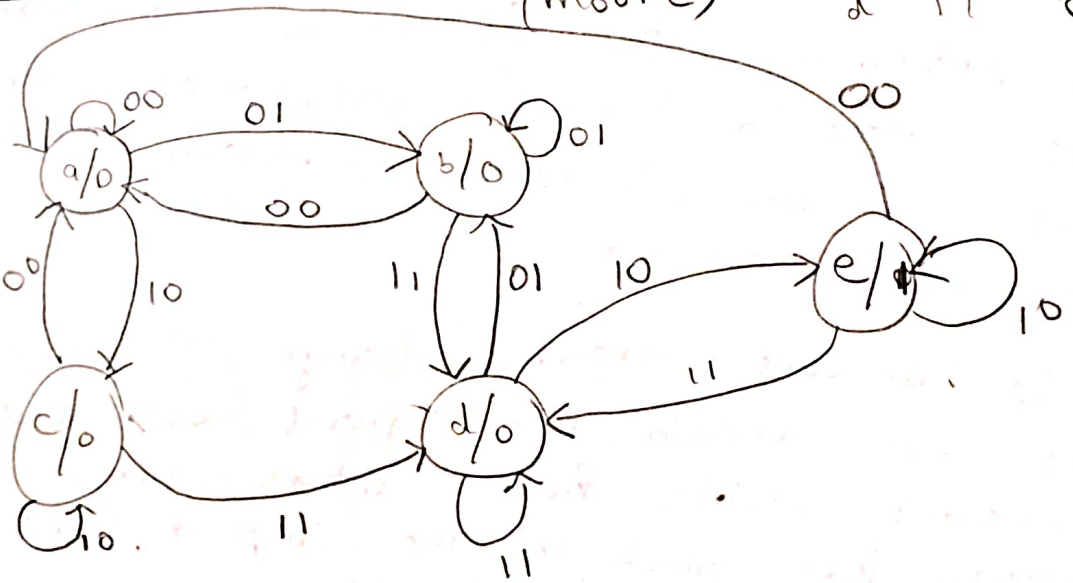
→ x goes high if A = 1 B makes tranition 1 → 0.

→ x remains high as long as this A = 1 B = 0 are maintained



a	00	0
b	01	0
c	10	1
d	11	0

State transition diagram: (moore)



Primitive table :

→ Next step is to form state table from state transition diagram.

→ In this table if all the rows representing a state has only one stable state for all possible input combinations it is termed as primitive table or primitive flow table.

→ Each row in this table has one dont care state

→ The dont care state in each row comes to a condition which asks both input to change at the same time

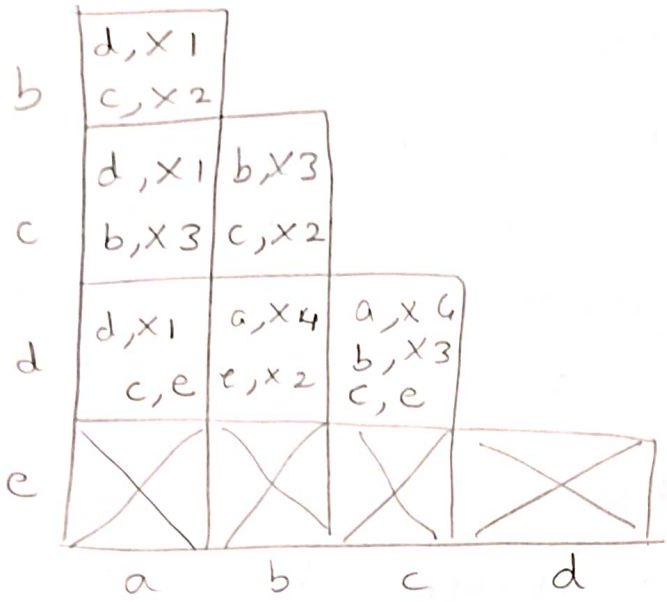
→ This condition is not allowed in an asynchronous sequential logic.

→ The suffix like 1, 2 are given (not compulsory)

→ This will be useful when we check state redundancy.

	AB: 00	01	11	10	X
a	(a)	b	x1	c	0
b	a	(b)	d	x2	0
c	a	x3	d	(c)	0
d	x4	b	(d)	e	0
e	a	x5	d	(e)	1

State reduction



→ c column → c, e condition is not satisfied
∴ e cannot be equal to a, b, c, d.

→ b column → b with d → not possible
∴ e, X_2 → not possible

→ b column → b, X_3
c, X_2
→ possible if → $X_3 = b$, $X_2 = c$

(bc) → Partition group.

→ a column → a with d → not possible
∴ c, e → not possible.

→ a column. → let $X_1 = d$, $X_2 = c$, $X_3 = b$

d, X_1 ⟹ d, d ⟹ (ab) can be grouped
c, X_2 c, c

→ a column → Let $X_1 = d$, $X_2 = c$, $X_3 = b$

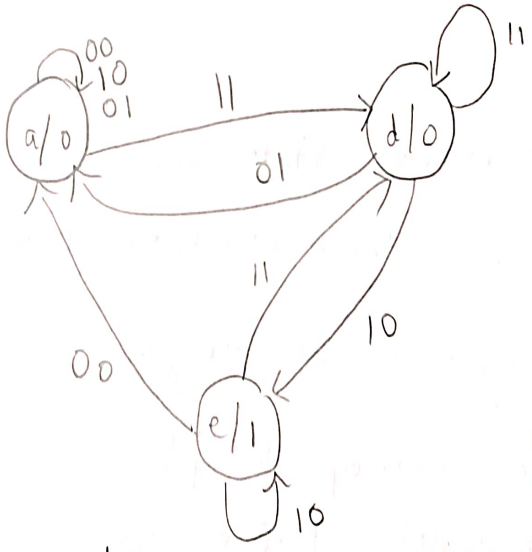
d, X_1 ⟹ d, d ⟹ (bc) can be grouped
b, X_3 b, b

Partition groups are

$$P = (abc)(d)(e)$$

Reduced state table

	AB: 00	01	11	10	X
a	(a)	(a)	d	(a)	0
d	X4	a	(d)	e	0
e	a	X5	d	(e)	1



State assignment:

→ suppose {a, d, e} is represented by {00, 01, 10} it occurs twice for d→e e→d transition.

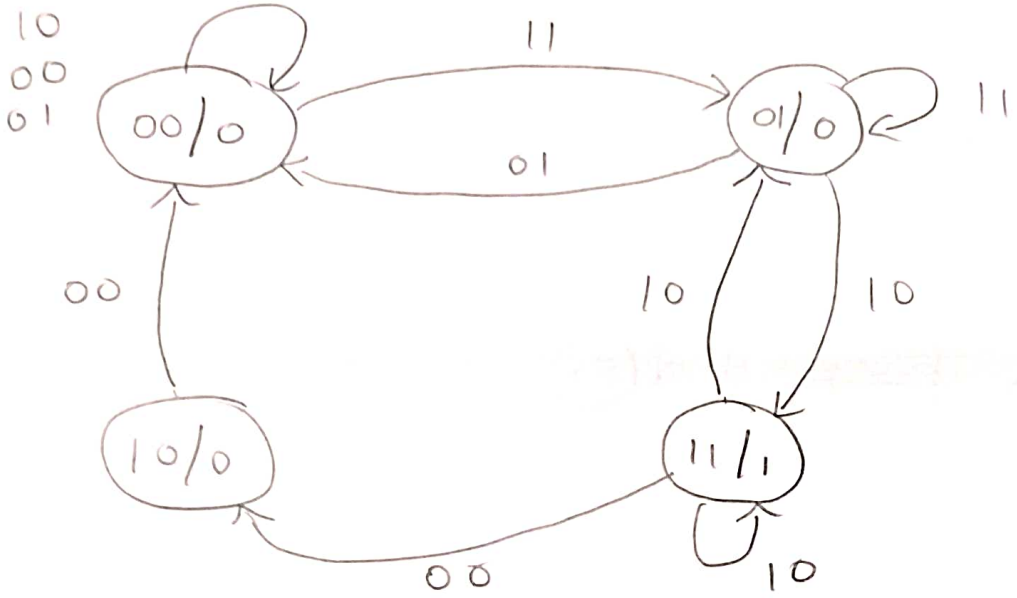
→ There arises a critical race problem for 01 to 10 transition

→ we can solve this by changing the representation {00, 01, 11}

→ Here e→a transition cause problem

→ Hence we introduce a dummy variable ϕ between e & a.

a : 00 d : 01 e : 11 ϕ = 10



→ we represent state variables by P & Q, feedback variables p & q.

Design eqns & ckt diagram :-

→ we use k-map to get expression of state variables P & Q as function of input A, B & p & q.

→ A, B → input variables → 00, 01, 11, 10

→ p, q → states, a, d, e, ϕ → 00, 01, 11, 10

→ Inside kmap fill up the next states. PQ

→ Prepare two kmaps to derive equation for P & equation for Q.

PQ \ AB	00	01	11	10
a ← 00	00	00	01	00
d ← 01	X	00	01	11
e ← 11	10	X	01	11
φ ← 10	00	X	X	X

PQ

eqn for P

PQ \ AB	00	01	11	10
00	0	0	0	0
01	X	0	0	1
11	1	X	0	1
10	0	X	X	X

$P = q\bar{B}$

eqn for Q

PQ \ AB	00	01	11	10
00	0	0	1	0
01	X	0	1	1
11	0	X	1	1
10	0	X	X	X

$Q = q\bar{A} + AB$

PQ	o/p
00 →	0
01 →	0
10 →	0
11 →	1

P \ q	0	1
0	0	0
1	0	1

$X = PQ$