12.8 A/D Techniques :

→ There are a variety of methods for digitizing analog signals

Successive approximation :

→ If multiplexing is required, the successive-approximation converter is most useful.

→ The block diagram for this type of converter is shown in fig below.

→ The converter operates by successively dividing the voltage ranges in half.

→ The counter is first reset to all 0s and the MSB is then set.

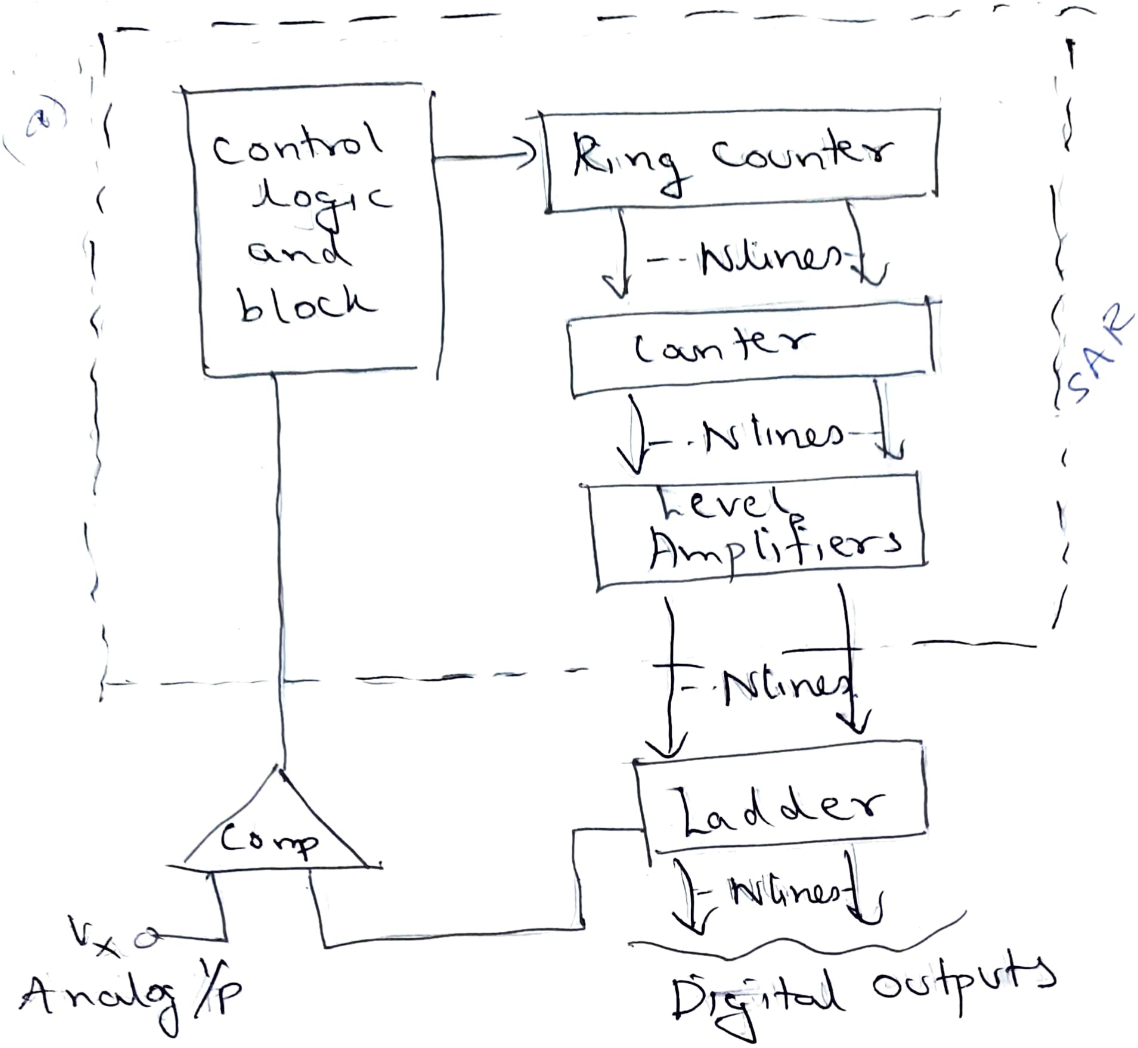
→ The MSB is then left in or taken out depending on the output of the comparator.

→ Then the second MSB is set in, and a ~~compromise~~ comparision is made to determine whether to reset the second MSB flip flop.

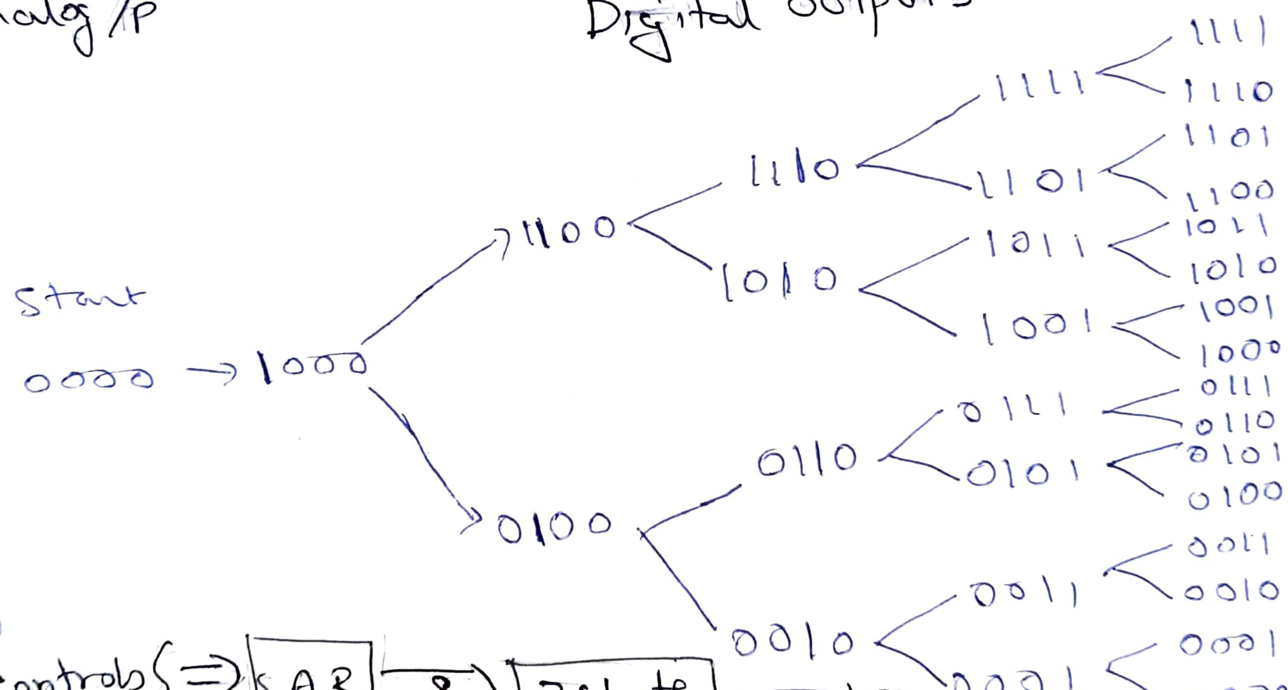
→ The process is repeated down to the LSB, and at this time the desired number is in the counter.

→ Since the conversion involves operating on one flip flop at a time, beginning with the MSB, a ring counter may be used for flip flop selection.

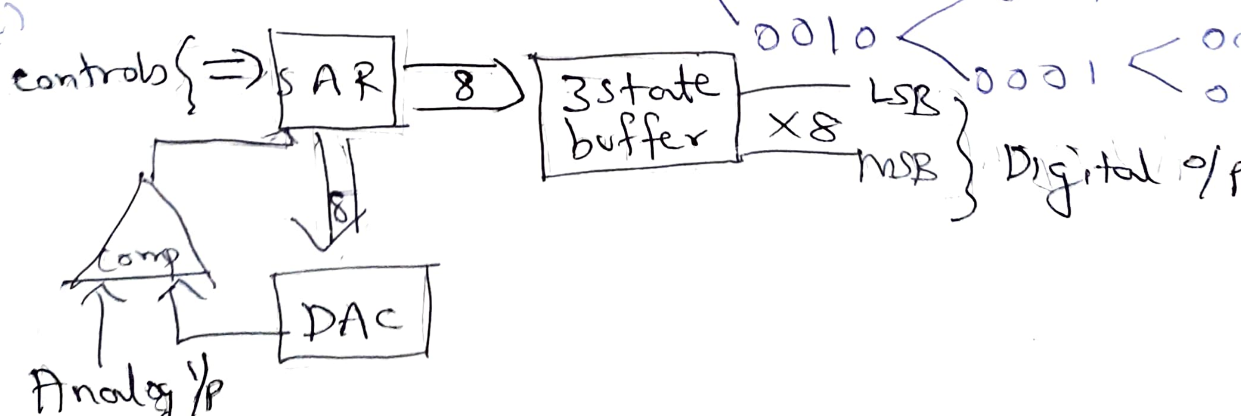
(a)


Control logic and block
Ring counter
N lines
Counter
N lines
Level Amplifiers
N lines
Ladder
N lines
Digital outputs
SAR
Comp
V_x
Analog I/P

(b)


Start
0000
1000
1100
0100
1110
1010
0110
0010
1111
1101
1011
1001
0111
0101
0011
0001
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
0010
0001
0000

(c)


controls
SAR
8
3state buffer
LSB
X8
MSB
Digital o/p
8
Comp
DAC
Analog I/P

→ The successive approximation method thus is the process of approximating the analog voltage by trying 1 bit at a time beginning with the MSB.

→ The operation is shown in diagram form in (b).

→ It can be seen from this diagram that each conversion takes the same time and requires one conversion cycle for each bit.

→ Thus the total conversion time is equal to the number of bits, n times the time required for one conversion cycle.

→ one conversion cycle normally requires one cycle of the clock.

→ All the logic blocks inside the dashed line are frequently constructed on a single MSI chip, this chip is called a successive approximation register (SAR). fig (a)

→ Fig (C) is an 8 bit μp compatible A/D converter that includes an SAR, D/A conversion capabilites, control logic and buffered digital outputs in a 28 pin DIP.

The ADC 0804 :-

→ ADC0804 is a very popular & inexpensive A/D converter which is available from a number of different manufacturers, including National semiconductor.

→ It is an 8 bit CMOS microprocessor compatible successive-approximation A/D converter that is supplied in a 20pin DIP.

→ It is capable of digitizing an analog input voltage within the range 0 to +5vdc.

→ It has a single dc supply voltage usually +5vdc.

→ The controls are wired such that the converter operates continuously.

→ This is the so called free-running mode.

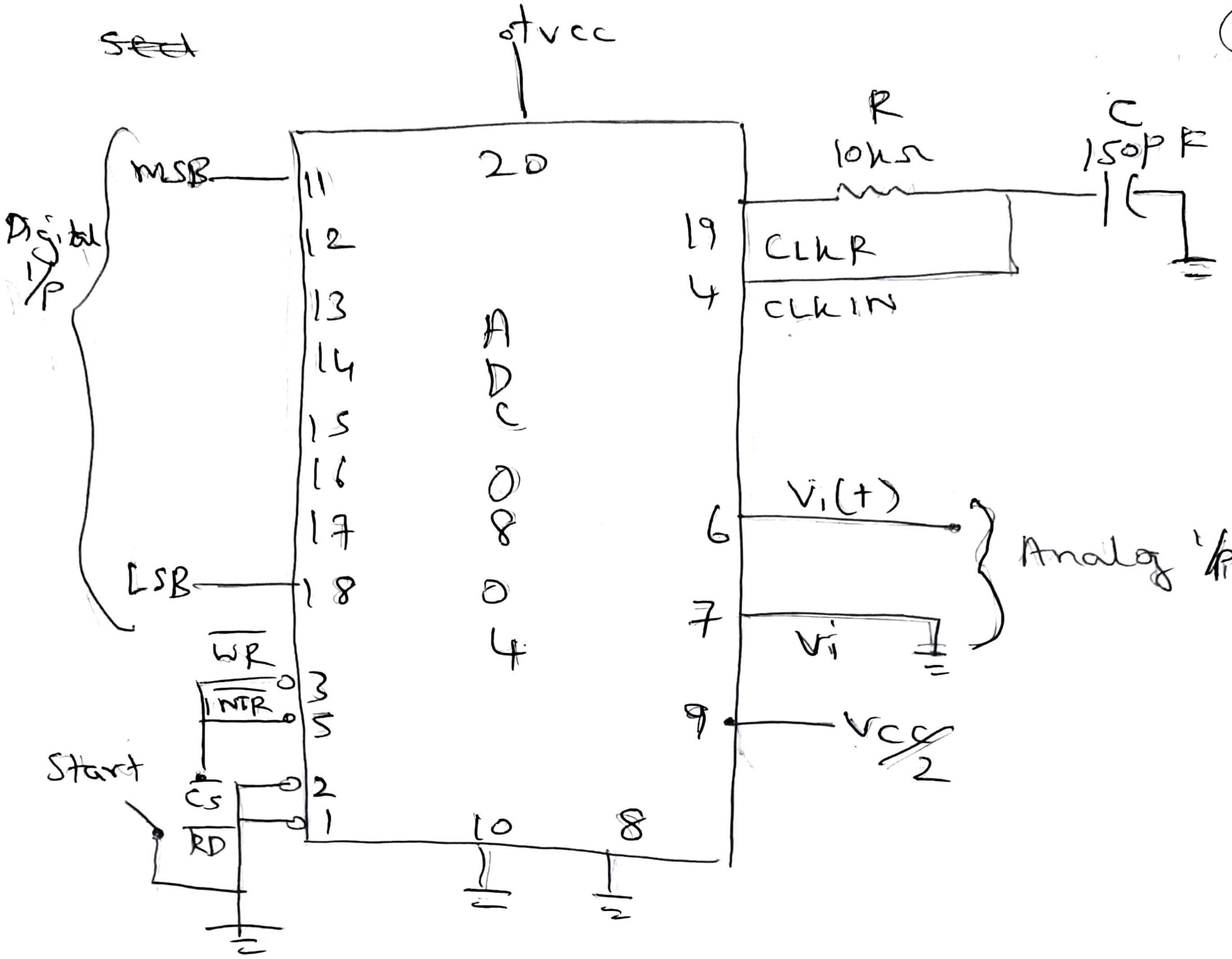
→ The frequency of operation according to

$$f = \frac{1}{1.1(RC)} = \frac{1}{1.1 \times (10k\Omega \times 150pF)}$$

$$= 607 \text{ kHz}$$

→ A momentarily activation of the START switch is necessary to begin operation.

~~Sect~~



Section counters :

→ Another method for reducing the total conversion time of a simple counter converter is to divide the counter into sections.

→ Such a configuration is called a section counter.

→ Assume that we have a standard 8 bit counter

→ If the counter is divided into two equal counters of 4 bits each, we have a section converter.

→ The converter operates by setting the section containing the four LSBs to all 1s and then advancing the other sections until the ladder voltage exceeds the input voltage.

→ At this point the four LSBs are all reset, and this section of the counter is then advanced until the ladder voltage equals the input voltage.

→ Notice that a maximum of $2^4 = 16$ counts is required for each section to count full scale.

→ Thus this method requires only $2 \times 2^4 = 2^5 = 32$ counts to reach fullscale.

→ This is a considerable reduction over the $2^8 = 256$ counts required for the straight 8 bit counter.

→ This type of converter is quite often used for digital voltmeters, since it is very convinient to divide the counters by counts of 10.

→ Each counter is then used to represent one of the digits of the decimal no.

12-10 A/D accuracy & resolution

→ Since A/D converter is a closed loop system involving both analog & digital systems, the overall accuracy must include errors from both the analog & digital positions

→ In determining the overall accuracy it is easiest to seperate the two sources of error.

→ If we assume that all the components are operating properly, the source of digital error is simply determined by the resolution of the system.

→ In digitizing an analog vg, we are trying to represent a continuous analog vg by an equivalent set of digital numbers.

→ The simple fact that the ladder voltage leads to digital error in the system.

→ This error is often called quantization error. and it can be commonly ±1 bit.

→ If the comparator is centred, as with continuous converter, the quantization error can be ~~can~~ made ±½ LSB.

→ The main source of analog error is in the comparator.

→ The error in the comparator is centred around variations in the dc switching point.

→ The dc switching point is the difference between the input voltage levels that cause the output to change state

→ variations in switching are due to primarily offset, gain and linearity of the amplifier used in the comparator.

→ These parameters usually vary slightly with input voltage levels & quite often with temperature.

→ It is these changes which give rise to the <u>analog error</u> in the system.

→ An important measure of converter performance is given by <u>differential linearity</u>, which is a measure of the variation in voltage step size that causes the converter to change from one state to next

→ It is usually expressed as a percent of the average step size.

→ In general, it is considered good practice to construct converters having analog and digital errors of approximately the same magnitudes.

→ There are many arguments for and against this and any final argument would have to depend on the situation.

→ As an example, an 8 bit converter would have a quantization error of $1/256 = 0.4$ percent.

→ It would then seem reasonable to construct this converter to an accuracy of 0.5 percent in an effort to achieve an overall accuracy of 1.0 percent.

→ This might mean constructing the ladder to an accuracy of 0.1 percent, the comparator to an accuracy of 0.2 percent and so on, since these errors are all accumulative.

Example 12.13

What overall accuracy could one reasonably expect from the construction of a 10 bit A/D converter?

→ A 10 bit converter has a quantization error of $\frac{1}{1024}$ = 0.1 percent.

If the analog portion can be constructed to an accuracy of 0.1 percent, it would seem reasonable to strive for an overall accuracy of 0.2 percent.