

7th semester
Open-lab Report 2021

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Lock in amplifier simulation using Multisim

Abstract

Lock-in amplifiers have become daily basis need in life for demodulation of signals as the stability of output in lock-ins is very assuring and the extraction the weak signal from the attenuated noisy signal makes the signal processing very simple. Lock-ins work under the principle of phase sensitive detection, this technique allows the user to extract the test signal with the help of a reference signal which has the same frequency as of the test signal. In this experiment we have tried to perform the experimental in the simulation software Multisim. Multisim is an electronic schematic capture and simulation program which helps to make electronic circuits for better understanding. In this experiment we have calculated the amplification factor(μ) in a lock-in amplifier and the phase of the detected test signal by simulating through single phase and dual phase lock-in amplifiers.

Aim of the experiment:

- Making single-phase and dual phase lock-in amplifier
- Calculating the amplification factor amplified signal.
- Calculating the phase shift of the original signal.
- Calculating the signal to noise ratio

Theory:

Introduction:

The lock-in amplifier is a device, which can measure very small AC voltages in the presence of noise. It uses the principle of phase sensitive detection. It produces a maximum DC output when the signal to be measured is in phase with a reference signal at the same frequency. (NISER)

The whole process of lock-in amplifier can be shown in the figure 1.

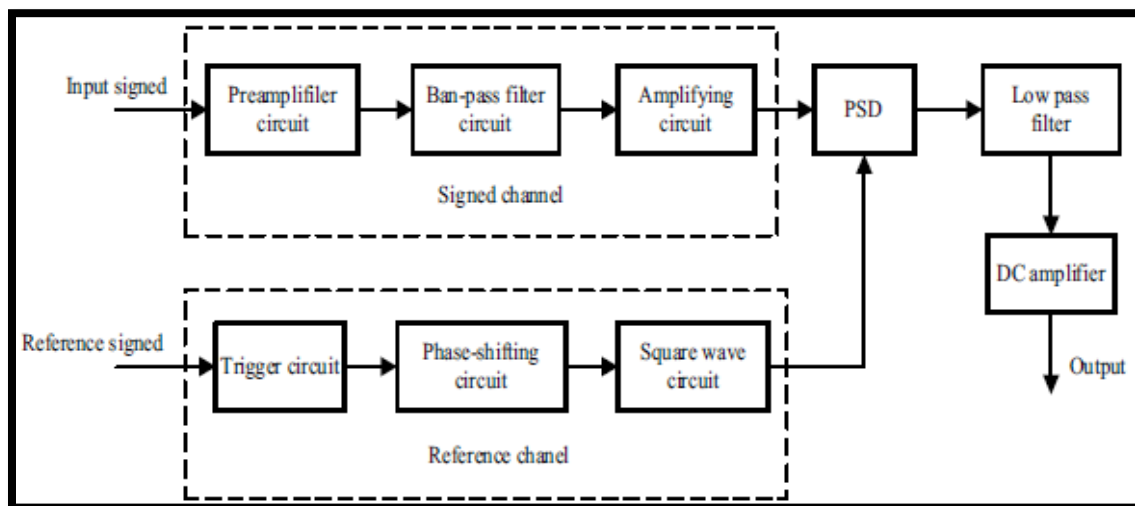


Fig.1: Lock-in internal frame diagram

Preamplifier:

Preamplifier is an electronic device which is used for amplifying weak signals, since weak signals are more prone to getting mixed with the noise. So, having an amplification of weak signals makes it more tolerant towards the noise. The amplified signal can be sent for further amplification or to a loudspeaker.

Preamplifier circuit with low noise, high gain, dynamic range of features. This design uses two integrated operational amplifiers, this circuit has a peripheral circuit is simple, high input impedance, can effectively suppress common mode interference characteristics. A well schematic circuit is show in figure 2.

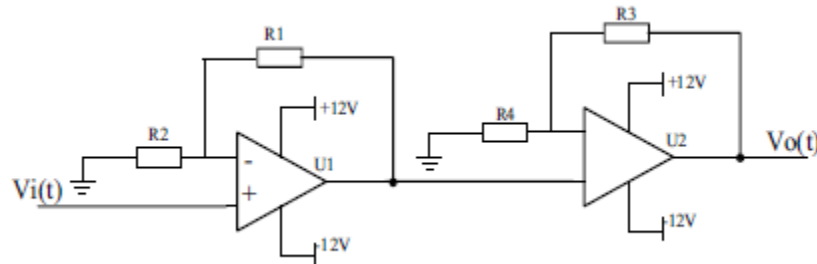


Fig.2 : Preamplifier circuit

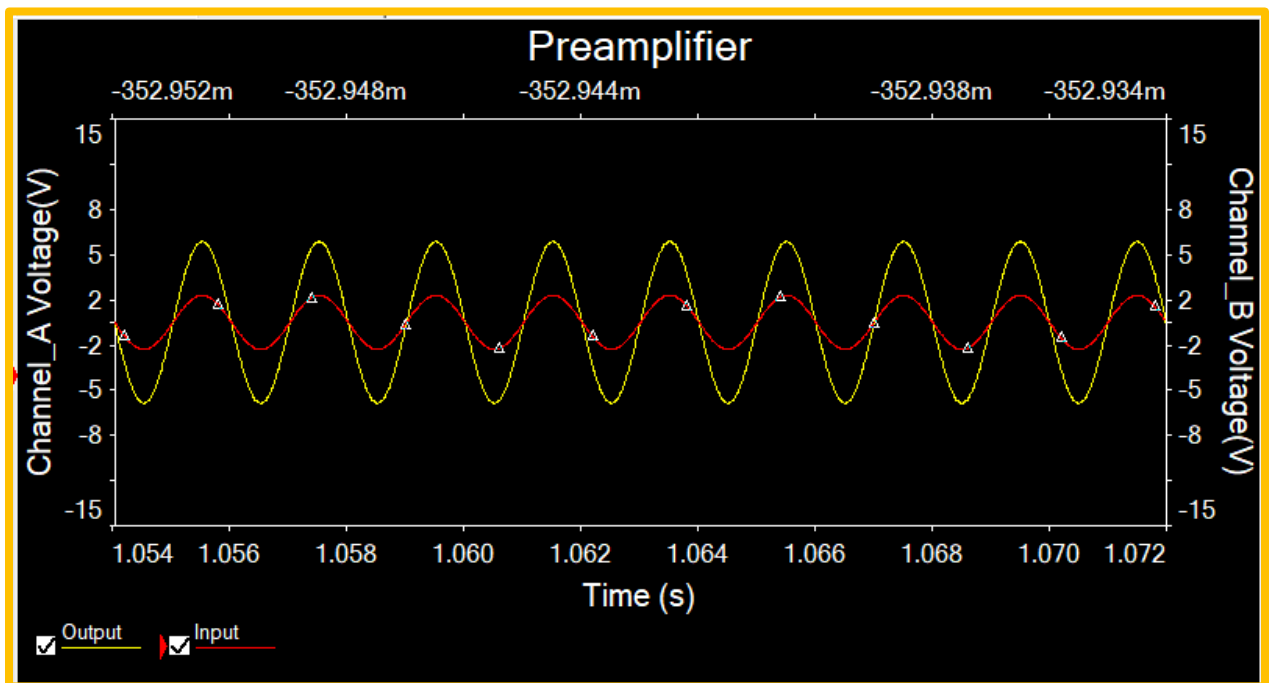


Fig.3: Preamplifier output

Band-pass Filter:

A band-pass filter is used for separating the signal from both lower and higher frequencies, it comprises of both a low pass filter and a high pass filter. Figure 4 shows the schematic circuit of an active band pass filter. Active band pass filter has a benefit over passive band pass filters

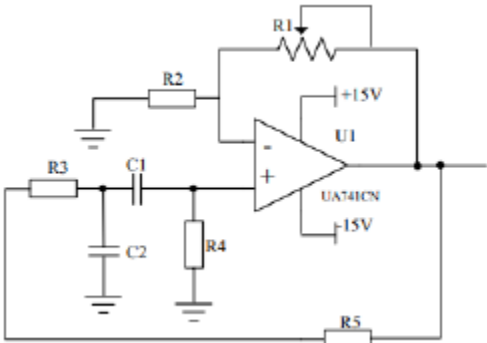


Fig.4: Active Band pass filter circuit

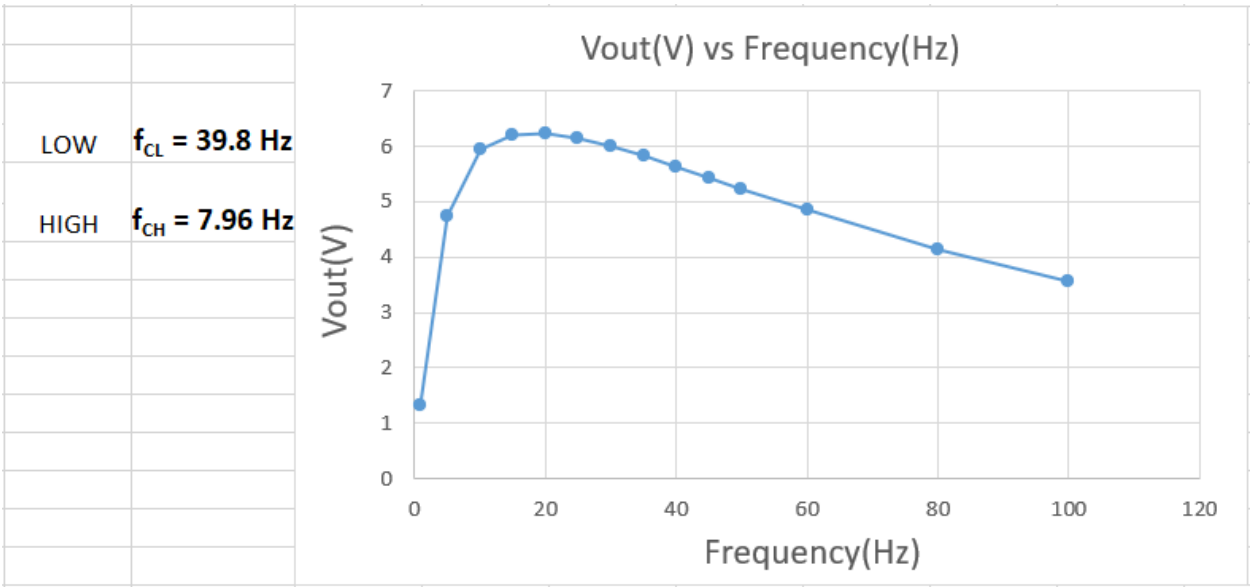


Fig.5 : Band pass filter V_{out} (V) vs Frequency (Hz)

AD630 IC:

The AD630 is a high precision balanced modulator/demodulator that combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. A network of onboard applications resistors provides precision closed-loop gains of ± 1 and ± 2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of 1, 2, 3, or 4. External feedback enables high gain or complex switched feedback topologies.

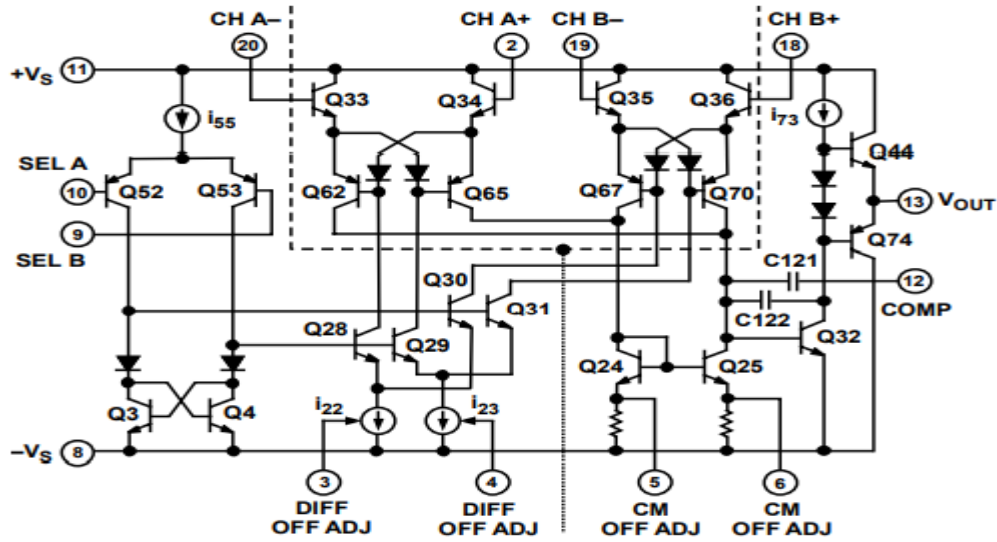


Fig.6: AD630 Simplified Schematic

How AD630 works?

The basic mode of operation of the AD630 may be easier to recognize as two fixed gain stages, which can be inserted into the signal path under the control of a sensitive voltage comparator. When the circuit is switched between inverting and noninverting gain, it provides the basic modulation/demodulation function. The AD630 is unique in that it includes laser wafer trimmed thin-film feedback resistors on the monolithic chip. The configuration shown in Figure-7 yields a gain of ± 2 and can be easily changed to ± 1 by shifting R_B from its ground connection to the output.

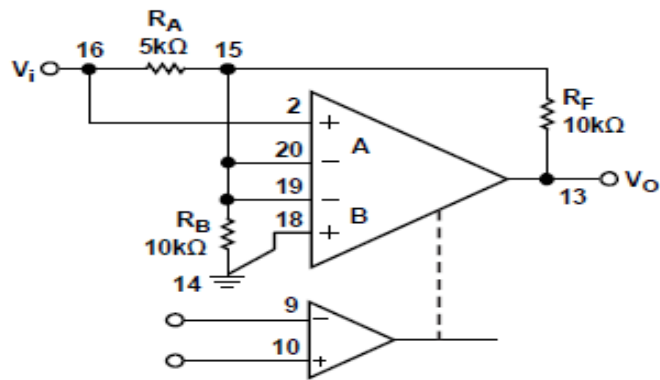


Fig.7:AD630 symmetric gain

When Channel B is selected, the R_A and R_F resistors are connected for inverting feedback as shown in the inverting gain configuration diagram in Figure-8-a. The amplifier has sufficient loop gain to minimize the loading effect of R_B at the virtual ground produced by the feedback connection.

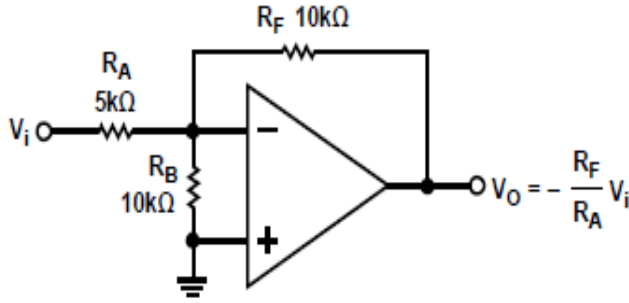


Fig.8(a): Inverting Gain Configuration

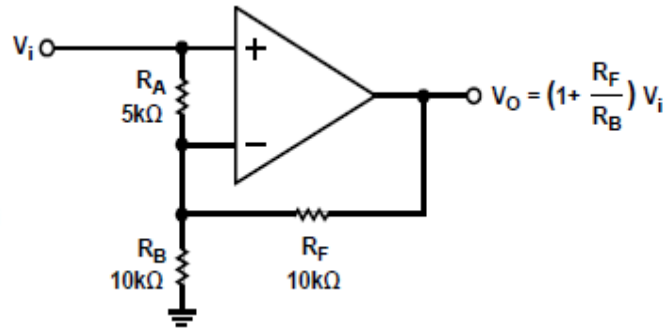


Fig.8(b): Non-inverting Gain Configuration

When the sign of the comparator input is reversed, Input B is deselected and Input A is selected. The new equivalent circuit is the non-inverting gain configuration shown in Figure-8-b. In this case, R_A appears across the op amp input terminals, but because the amplifier drives this difference voltage to zero, the closed-loop gain is unaffected.

Phase-sensitive detection:

Phase sensitive detection requires the use of the AD630 IC, here the input signal and the reference signal are fed into the IC and the output received is in the form of full wave rectifier output (i.e., oscillating from 0 to +a value.)

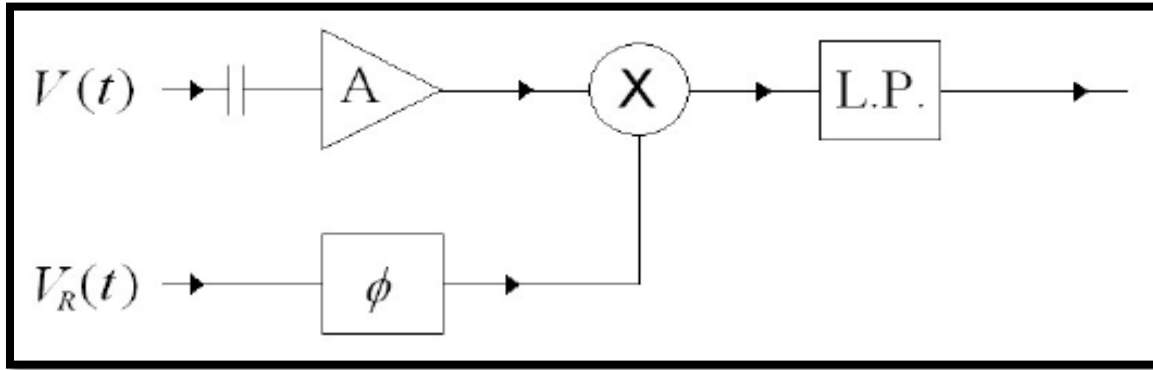


Fig.9: Block diagram of phase-sensitive detection

The AD630 IC receives the amplified signal and the reference signal as input and it matches the signal frequency with the reference frequency such that the wave which has the reference frequency remains in the signal and the remaining all frequency waves are cancelled out.

Mathematically the filtering of the signal can be given as follows:

Let's consider a sinusoidal input signal:

$$V_S(t) = V_o \sin(\omega t + \phi)$$

Let our reference signal be:

$$V_R(t) = \sin(\Omega t)$$

Now the product of these two frequencies will give us:

$$V_S(t)V_R(t) = \frac{V_o}{2} \{ \cos[(\omega - \Omega)t + \phi] - \cos[(\omega + \Omega)t + \phi] \}$$

Now when $\omega \neq \Omega$ the average value of the oscillation within a time period goes to zero. However, when $\omega = \Omega$ we get a sinusoidal output and with a DC offset.

$$V_S(t)V_R(t) = \frac{V_0}{2} \{\cos[\phi] - \cos[2\Omega t + \phi]\}$$

On adjusting the DC offset and by determining the ϕ we can get the direct measurement of the signal amplitude V_0 . Now in the above signal we can see the two frequency terms, the higher frequency term can be removed by using a low pass filter.

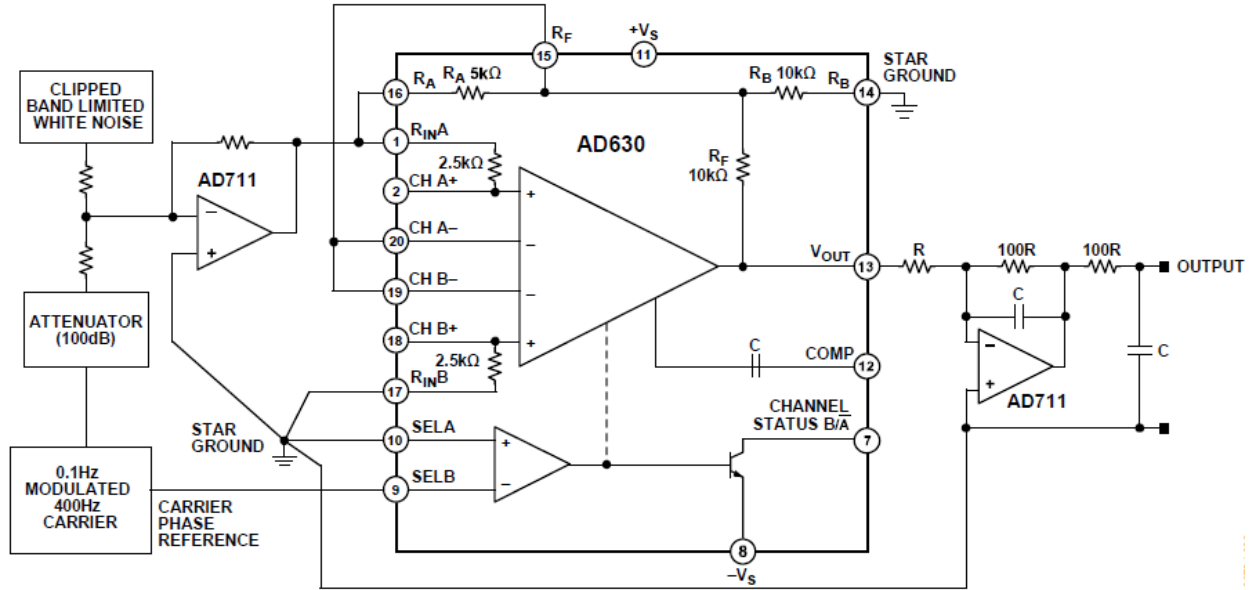


Fig.10: AD630 circuit connections in a lock in amplifier

Low pass filter:

The low pass filter only allows low frequency signals to pass and stops the high frequency signal waves, the cut-off frequency of the low pass filter can be given as:

$$f_c = \frac{1}{2\pi RC}$$

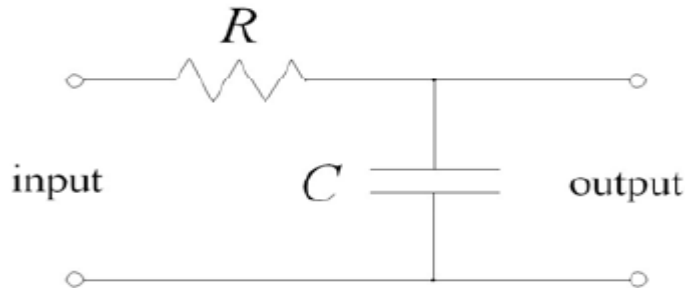


Fig.11: A first order passive low pass filter

The below figure shows the frequency response of an ideal and a normal passive low pass filter, the cut-off frequency is also given as -3dB frequency or when the output of the low pass filter lags by a phase of 45° and the slope for 1st order low pass filter is -20 dB/decade

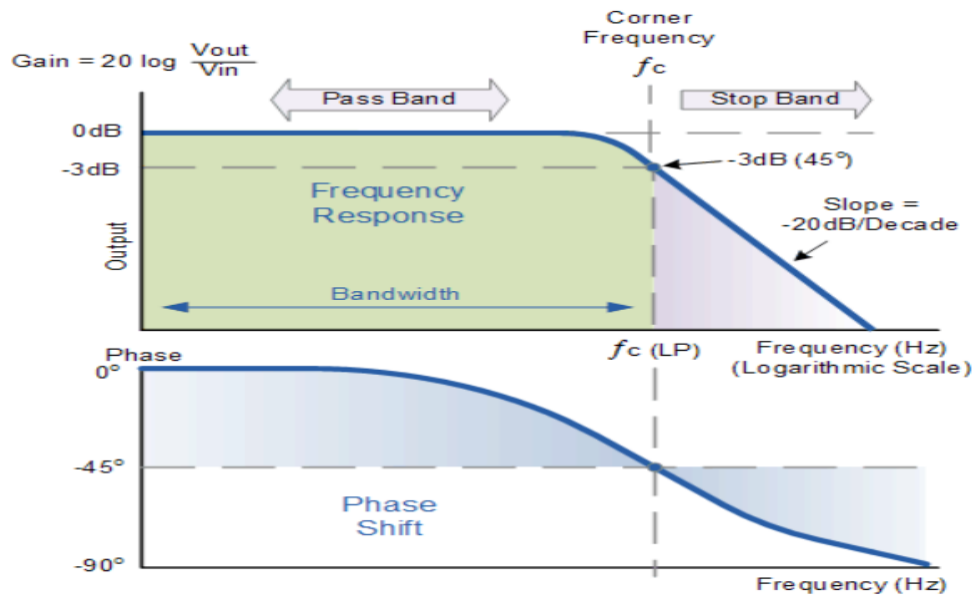


Fig.12: Frequency response of a low pass filter.

Active low pass filters work same with the same principle as the passive filters with an additional property of gain (i.e., in passive low pass filter the output voltage will always be less than the input voltage, except at zero frequency or DC input)

Lock-in amplifier functioning and its applications:

The main purpose of lock-in amplifier is to demodulate (separate) the incoming from the carrier wave and the attenuated noise with it. By knowing the frequency of the original signal, the same signal can be retrieved from the attenuated signal by feeding with reference signal of same frequency of original signal and performing the demodulation.

The figure-13 shows the different stage of the signal, starting from unattenuated signal to attenuated signal plus noise and the last is the lock-in output stage.

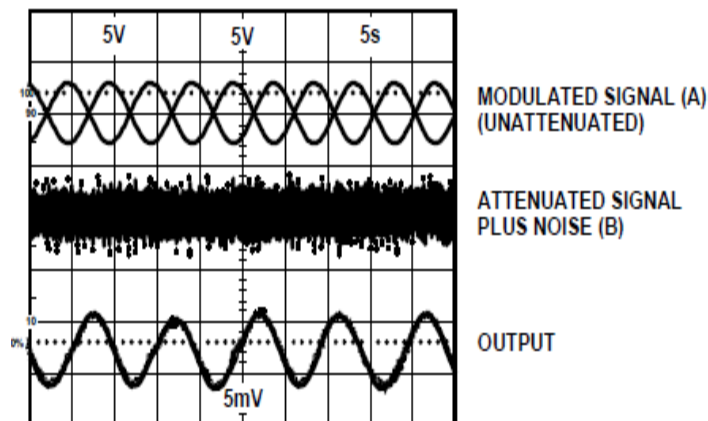


Fig.13: Lock-in amplifier waveform

Working formula:

1. Amplification factor:

Amplification factor is given as the ration of the output signal voltage to the input signal voltage, it is a dimension less quantity. On plotting the graph between the V_{Output} vs V_{Input} the slope gives the amplification factor and the error in amplification factor is given by the standard deviation.

$$\mu = \frac{\text{Output voltage in } V}{\text{Input voltage in } V}$$

2. Phase of the input signal:

In order to calculate the phase of the input signal we made a dual-phase lock-in amplifier, it is made via consecutively attaching the single-phase lock-in amplifier, here the second reference signal is always 90° phase to the first reference.

Therefore, the calculated phase of the lock-in amplifier can be given as:

$$\phi = \tan^{-1}\left(\frac{X \text{ lock} - \text{in output in } V}{Y \text{ lock} - \text{in output in } V}\right)$$

Circuit diagrams:

All the circuits shown here are made up with the help of Multisim software:

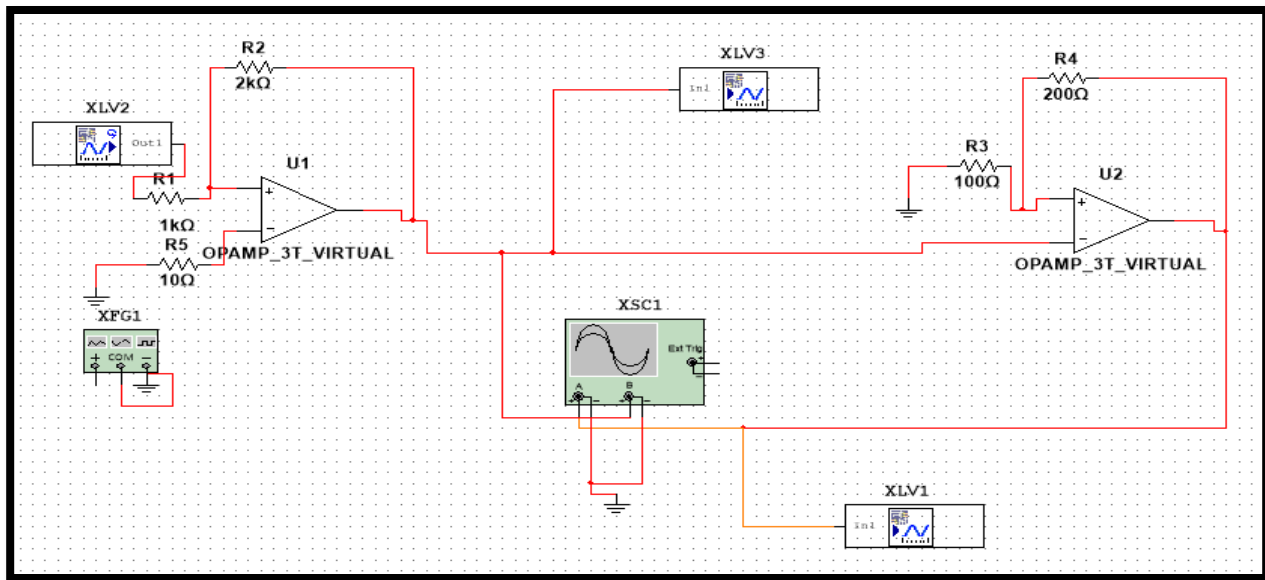


Fig.14:Preamplifier circuit

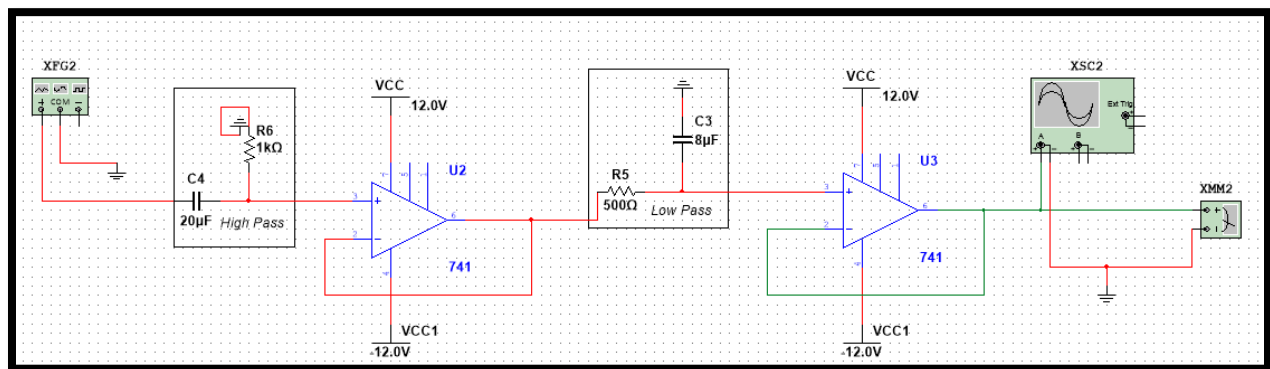


Fig.15: Band-pass filter circuit

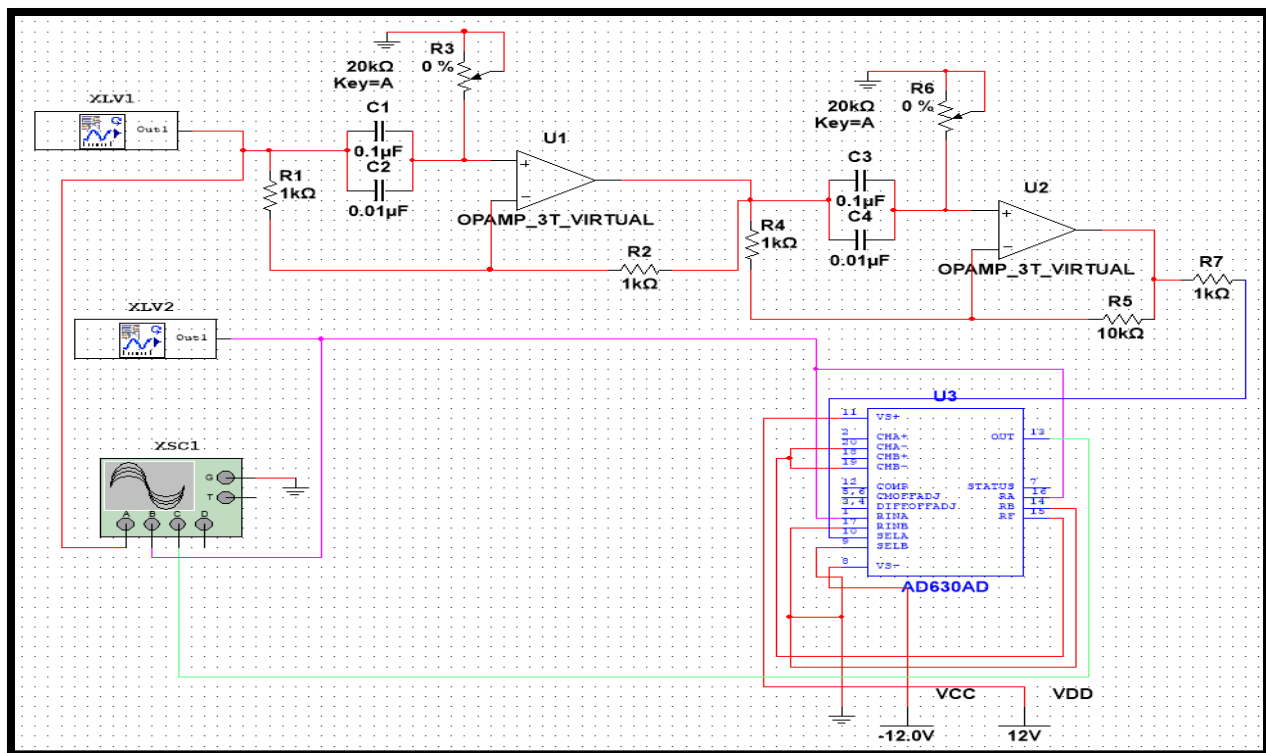


Fig.16: AD630 circuit

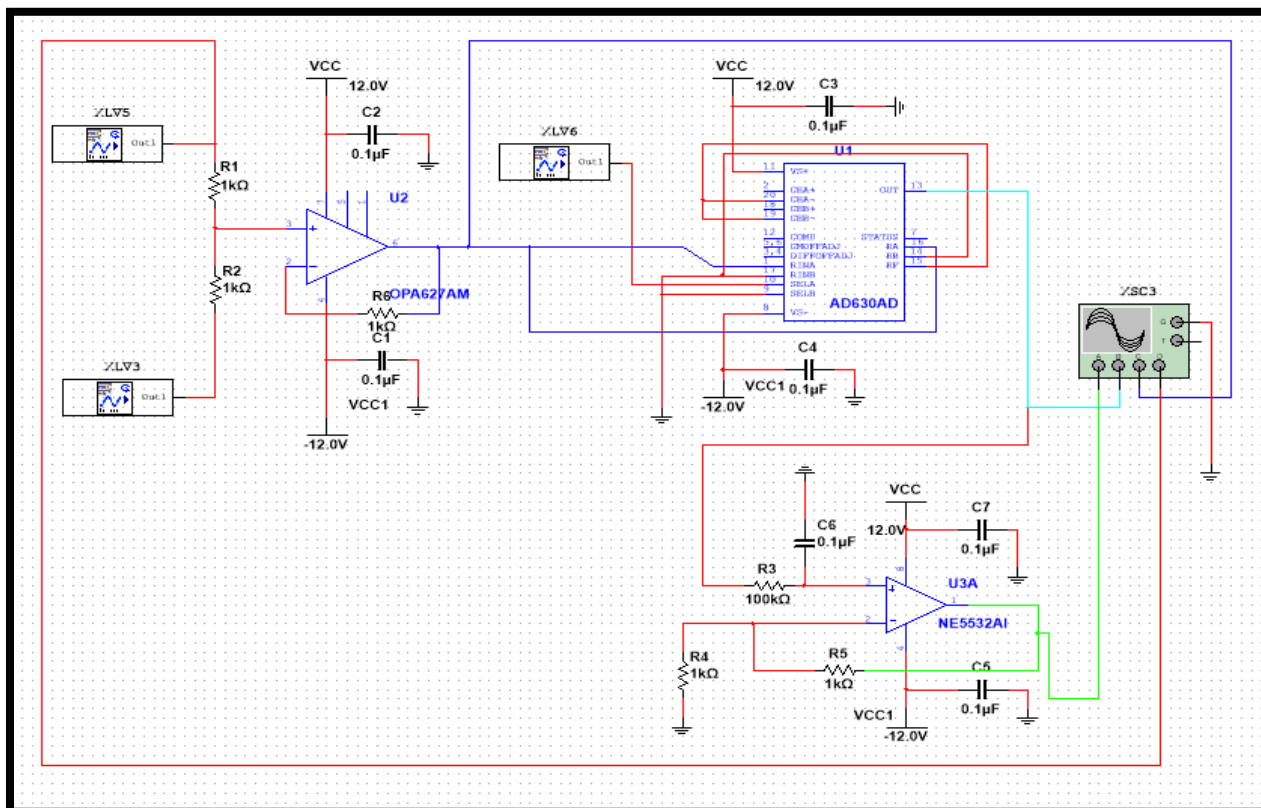


Fig.17: Single-phase lock-in amplifier

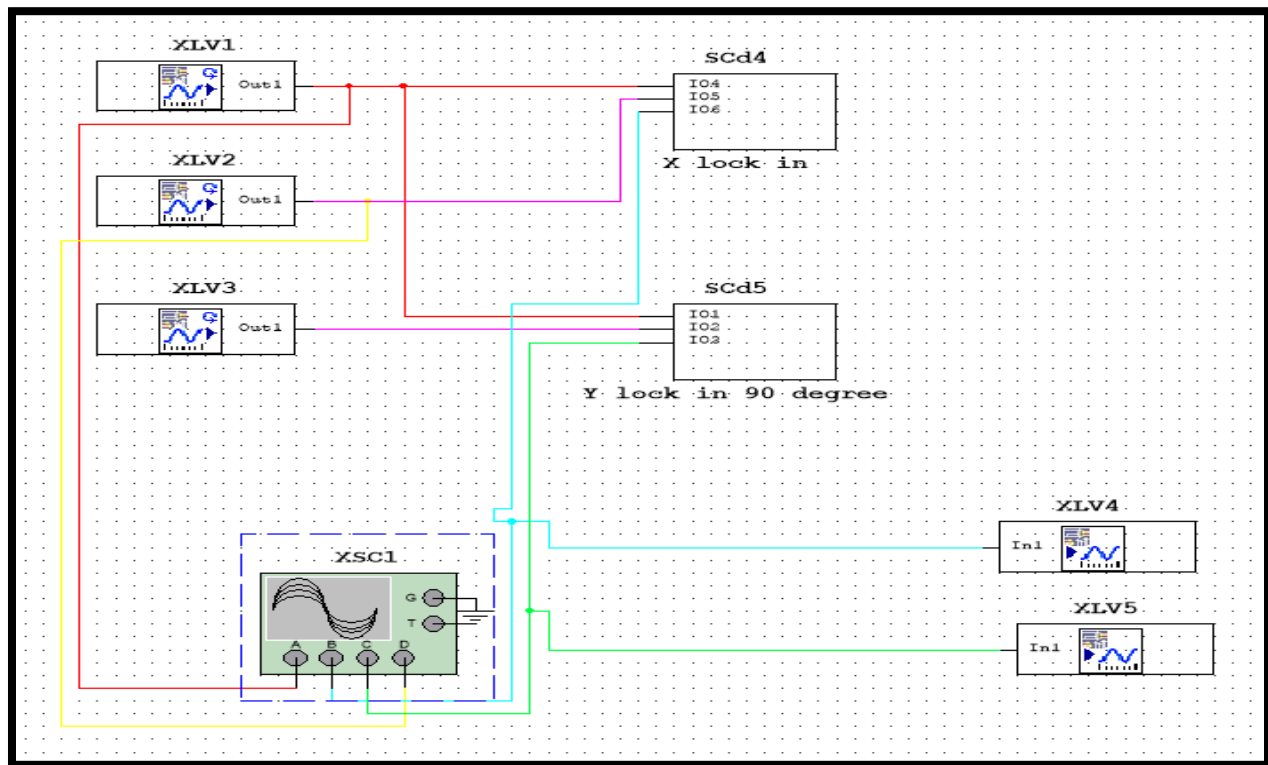
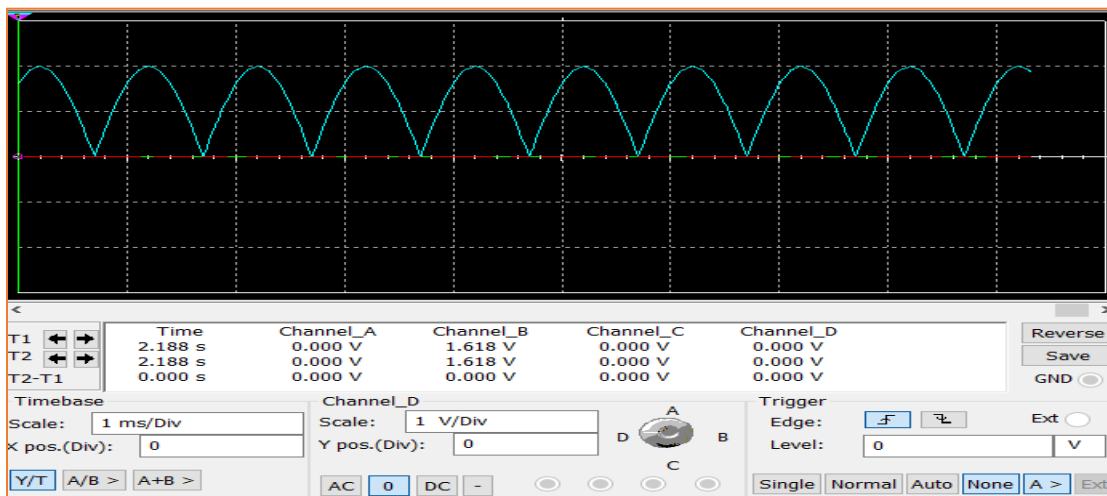


Fig.18: Dual-phase lock-in amplifier (here X & Y are single phase lock-in amplifier)

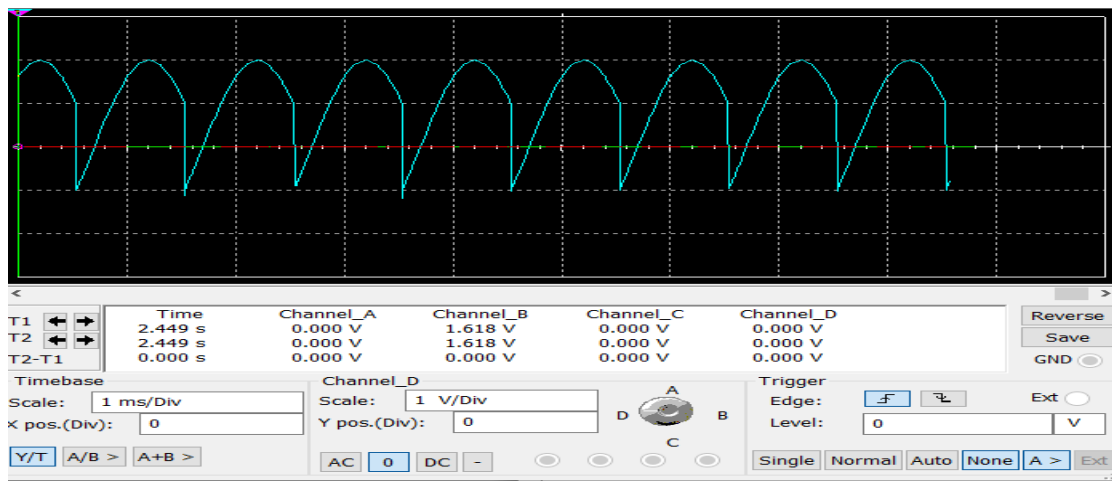
Observations:

a) AD630 output behaviour with changing phase:

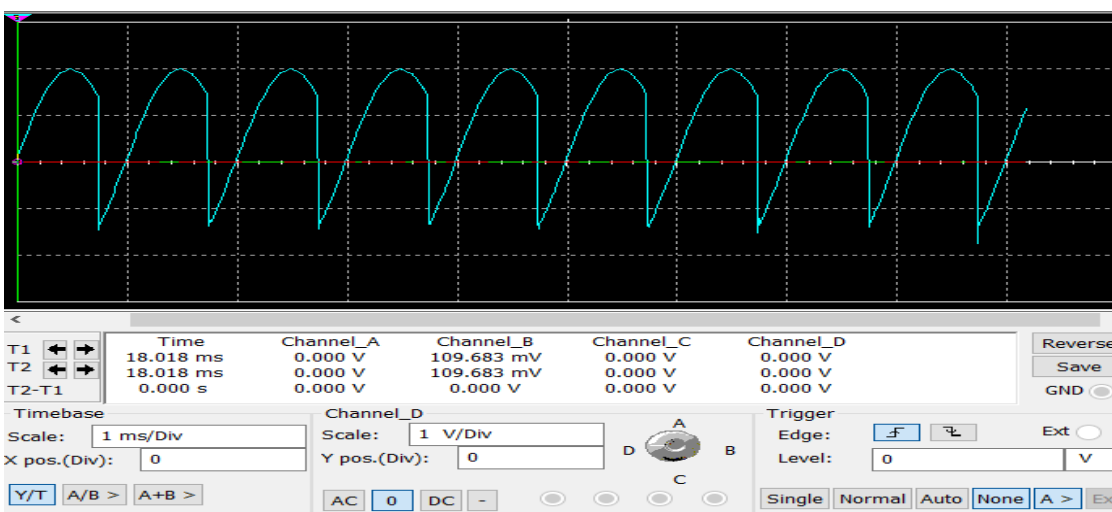
(I) Phase = 0°



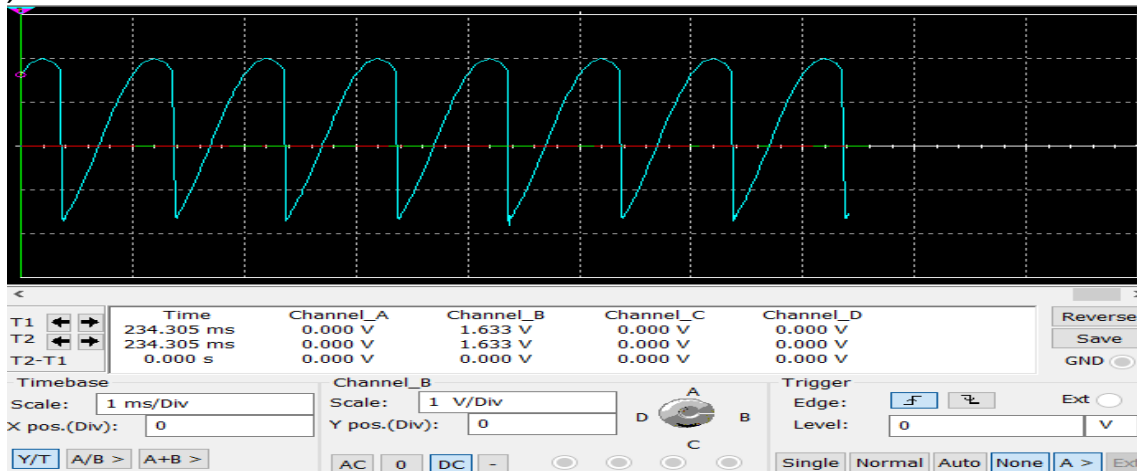
(II) Phase = 30°



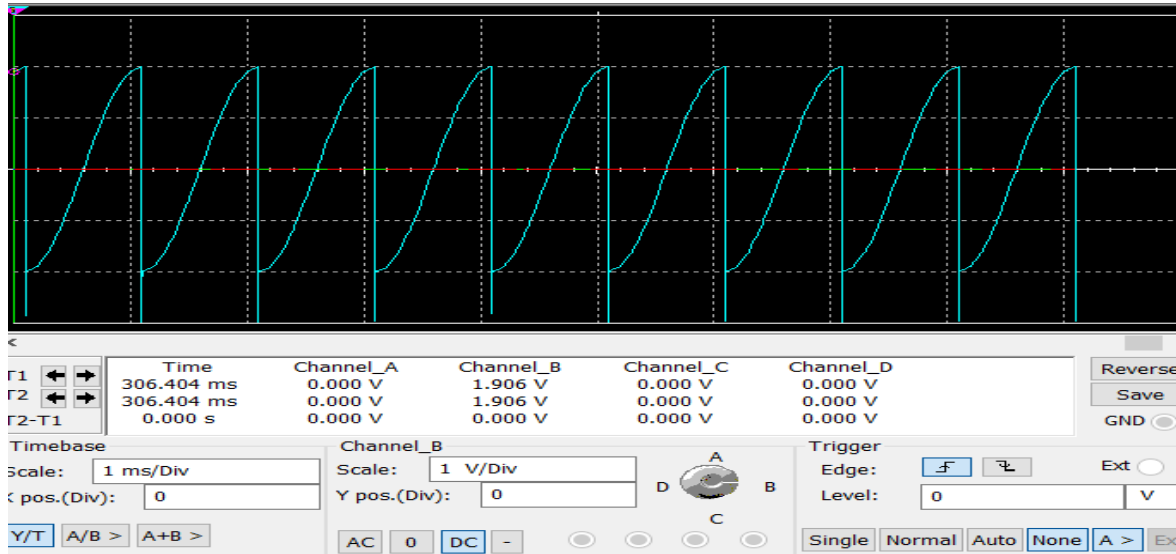
(III) Phase = 45°



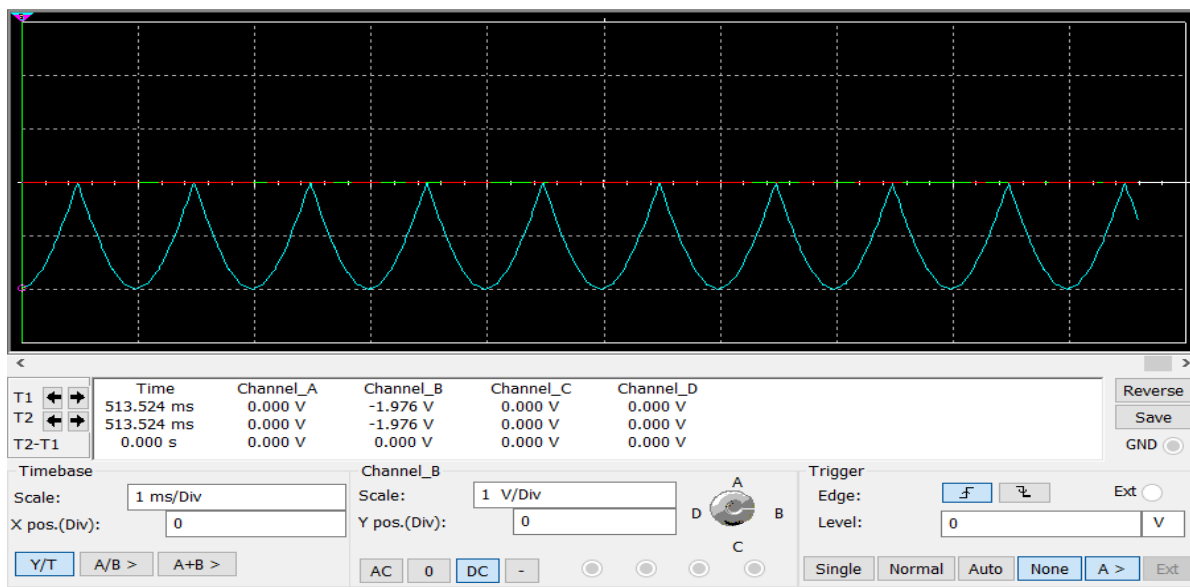
(IV) Phase = 60°



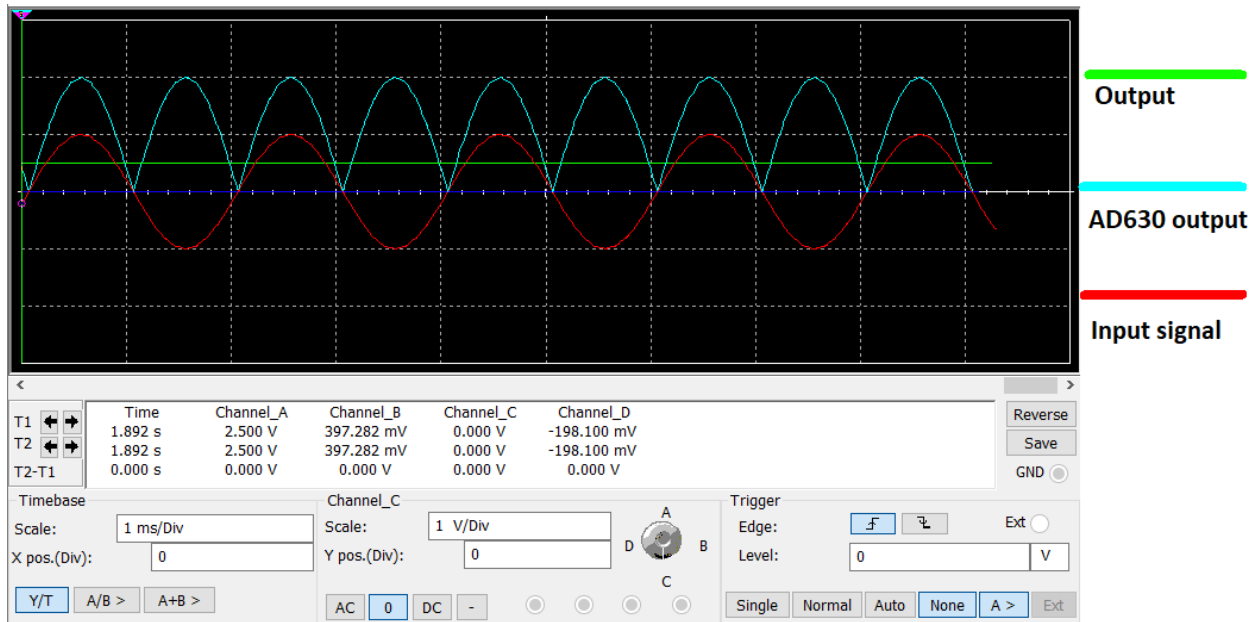
(V) Phase = 90°



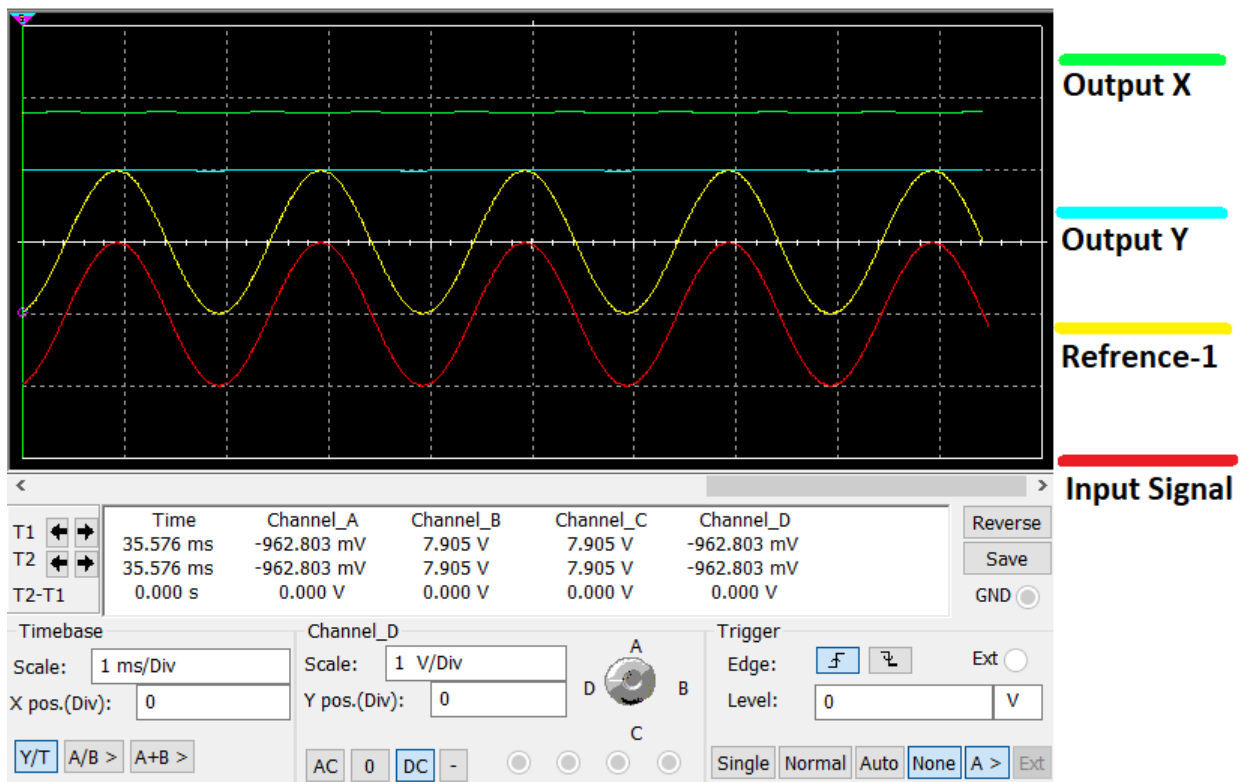
(VI) Phase = 180°



(b) Single phase lock-in amplifier:



(C) Dual-Phase lock-in:



Data:

(I) Single phase lock-in:

Frequency=500 Hz			
$V_{p-p}(V)$	$V_{input}(rms)(V)$	$V_{dc} (V) (output)$	V_{signal}
0.1	0.070	0.216	0.10079
0.2	0.140	0.460	0.197156
0.3	0.211	0.712	0.296682
0.4	0.281	0.960	0.394629
0.6	0.421	1.488	0.60316
0.8	0.561	1.974	0.795103
1.0	0.701	2.511	1.007188
1.2	0.842	3.023	1.2094
1.5	1.050	3.765	1.502449
2.0	1.400	5.024	1.999684
2.5	1.750	6.291	2.500079
3.0	2.100	7.460	2.961769

(II) Single phase lock-in with noise:

Noise frequency = 500			
$V_{input} (V)$	$V_{dc} (V)$	$V_{signal} (V)$	% Error
0.1	0.214	0.1	0.00
0.3	0.72	0.299842	0.05
0.5	1.22	0.497314	0.54
0.8	1.99	0.801422	0.18
1	2.49	0.998894	0.11
1.5	3.76	1.500474	0.03
2	5.02	1.998104	0.09

(III) Dual phase lock-in (constant input):

Frequency = 500Hz					
V _{input} (V)	Input Phase (ϕ°)	X _{output} (V) DC	Y _{output} (V) DC	Cal. phase (ϕ°)	R
1	1	8.018	0.28	2.000037615	8.02288751
1	10	7.902	1.262	9.073874216	8.002140214
1	20	7.483	2.343	17.38584521	7.841233194
1	30	6.693	3.742	29.20918846	7.668038406
1	45	5.226	4.949	43.44058851	7.197477127
1	60	3.321	6.132	61.56068357	6.973554689
1	90	0.178	8.073	88.73690121	8.074962105

Here ‘R’ is the total magnitude of the signal combined i.e., $R = \sqrt{X^2 + Y^2}$

(IV) Dual phase lock-in (constant phase):

Frequency=500 Hz & Θ=60°				
V _{in} (V)	X _{output} (V) DC	Y _{output} (V) DC	R	V _{signal} (V)
0.1	0.088	0.179	0.19946	0.101305772
0.3	0.340	0.616	0.70360	0.300681073
0.5	0.596	1.050	1.20736	0.49990473
0.8	0.982	1.700	1.96324	0.798838581
1.0	1.230	2.140	2.46830	0.998575896
1.5	1.870	3.230	3.73226	1.498443695
1.7	2.130	3.670	4.24332	1.700555315
2.0	2.510	4.330	5.00490	2.001739145

(V) Dual phase lock-in with noise:

Noise frequency = 500 Hz						
Input (ϕ°)	V_{in} (V)	X_{output} (V)	Y_{output} (V)	R	V_{signal} (V)	Phase (ϕ°)
20	0.50	1.150	0.392	1.214975	0.502917	19.8227
55	0.75	1.050	1.510	1.839185	0.749776	55.7866
30	1.00	2.150	1.230	2.476974	1.002007	29.5736
75	1.50	0.951	3.610	3.733162	1.498799	75.3416
60	2.00	2.490	4.330	4.994897	1.997784	60.2986
10	2.50	6.180	1.050	6.268564	2.501489	9.6526

Graphs:

(I) Single phase lock-in: V_{out} vs V_{input}

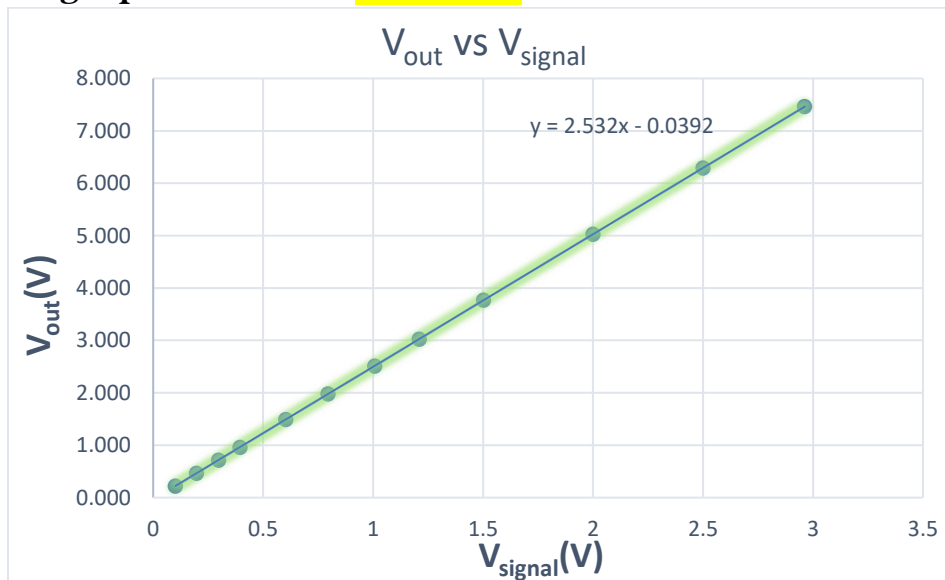


Fig.19: V_{out} vs V_{signal}

The above graph has a slope of **2.5159** and an intercept of **- 0.0277**, where our slope represents the amplification factor (μ)

(II) Dual phase lock-in: (i) **R vs V_{in}**

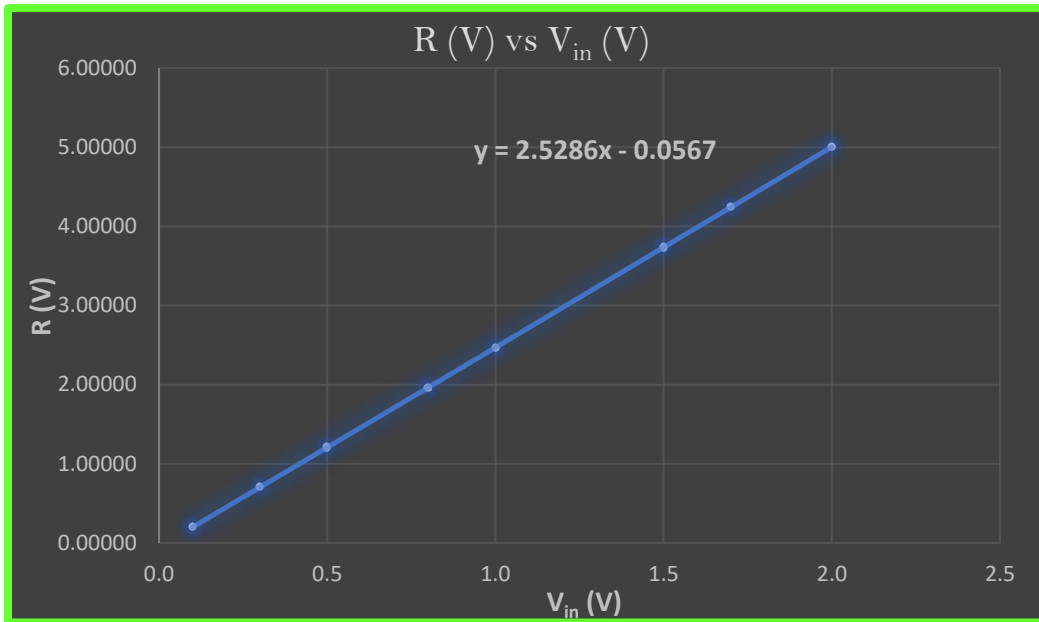


Fig.20: R (Volts) vs V_{in} (Volts)

(ii) **ϕ (calculated) vs ϕ (input):** (only for verification purpose)

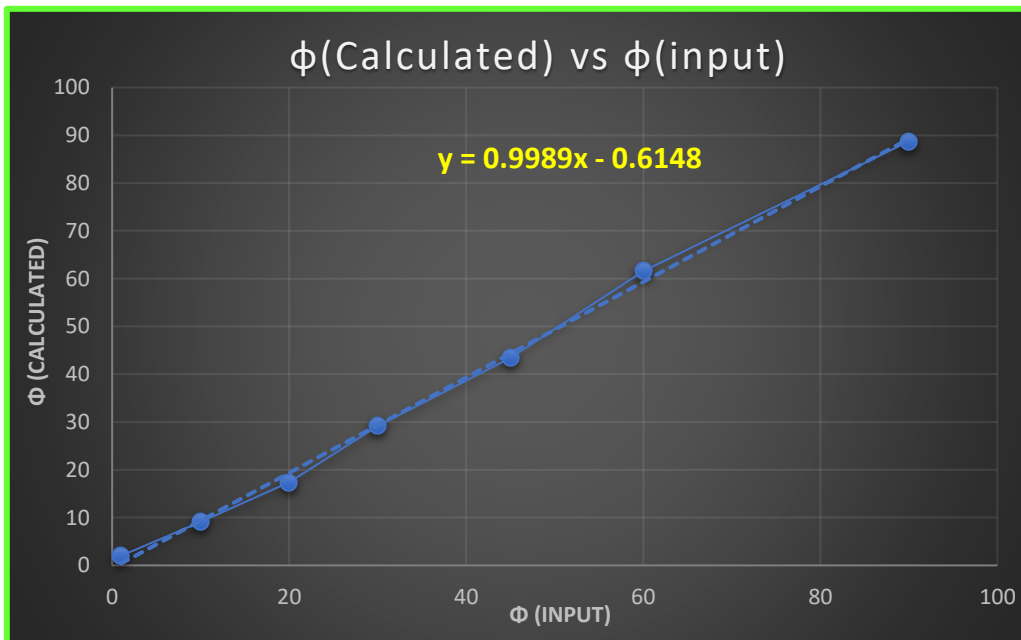


Fig.21: Calculated phase vs Input phase

In the figure-21 the slope is closer to 1 and which confirms that the calculated phase from dual phase lock-in amplifier is same as the phase of input signal.

Results and Discussion:

In the experiment Lock-in amplifier simulation we have tried to calculate the amplification factor (μ) and the phase of the incoming signal, we have also tried to verify the phase detection by the keeping the known phase values of the input signal.

- (i) Amplification factor(μ):

The amplification factor of the lock-in amplifier from the graph(figure-19) has been found to be:

$$\text{Amplification factor } (\mu) = 2.5159 \pm 0.0277$$

- (ii) The single phase and dual phase lock-in amplifiers have been successfully simulated and phase detection has been verified.

The amplification factor found is only twice that of the input signal, the reason for such low amplification maybe due to the wrong choice of combinations of feedback resistor and capacitors.

The AD630 IC used in the lock-in amplifier circuit is capable of both modulating and demodulating the signal but, for our purpose we have used it for demodulation purpose only.

Conclusion:

In this experiment, through the Multisim simulation software the design of signal channel, reference channel, phase sensitive detector and the low pass filter were combined simulated as the design of the lock-in amplifier. From the figure-13 it can be seen that lock in amplifier is very capable of separating the required frequency from the noisy and weak signal and this property is very useful in telecommunications, radio FMs and television cables, i.e., different channels can be sent in single signal by modulating their frequency and phase. The lock-in system helps in conserving the required energy and resources. On looking into these many benefits of lock-in in future it might be useful in other fields such as optics, electromagnetism, etc.

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2. **Mingxin Song and Fangfang Liu. Mingxin song and fangfang liu. International Journal of SignalProcessing, (1),2015.doi:10.14257/ijcip.2015.8.5.24. URL http://article.nadiapub.com/IJSIP/vol8_no5/24.pdf**
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