COMPUTER ENGINEERING

DLCA ODD SEM 2021-22/EXPERIMENT 2

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Experiment No - 2

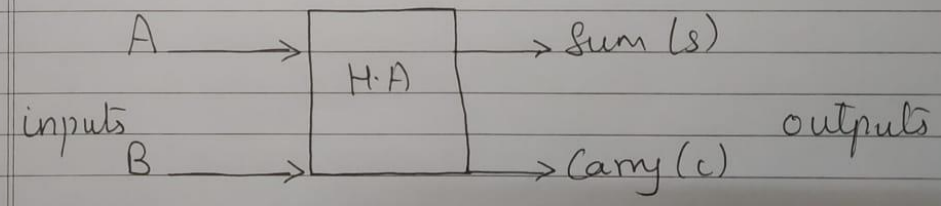
Aim:- Implement To design and Verify Half Adder Circuit

Software used: Virtual labs

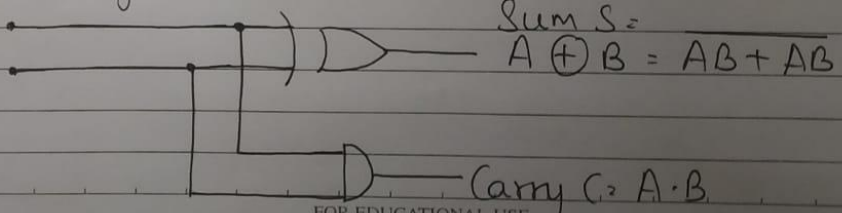
Theory:

Half Adder:

Half Adder is a Combinational logic circuit with two inputs and two outputs which carries out addition of two "single" bit numbers. The circuit has two outputs namely "sum" and "carry" The block diagram is shown below. The half adder circuit is suppose to add two single bit binary numbers A and B



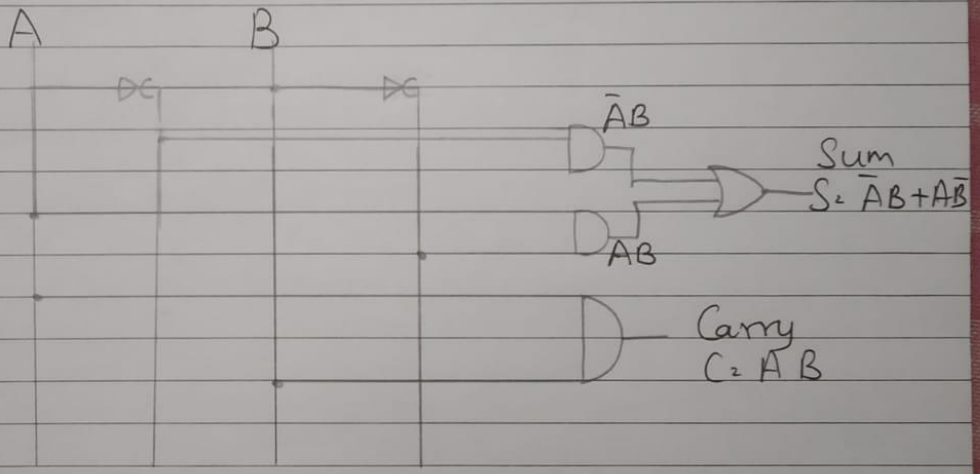
logic diagram



Truth table:

Input		Output	
A	B	Sum	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half adder using basic gates



Conclusion: Hence we have verified the truth table of Half Adder and proved the results.

OUPUT:

Half Adder