COMPUTER ENGINEERING

DLCA ODD SEM 2021-22/EXPERIMENT 3

NAME:- GAURAV AMARNANI (D7A, 67)

Experiment No: 3

Aim: To design and verify full Adder Circuit

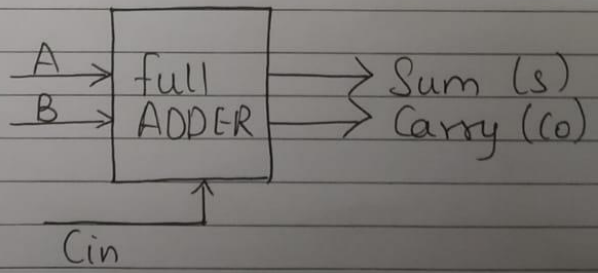
Software used: Virtual labs

Theory:

Full Adder

Full Adder is a three input two output combination logic circuit which can add three single bits applied at its inputs to produce sum and carry outputs. It can add two one-bit numbers A and B and carry Cin. The full adder is a three input and two output combinational circuit. To overcome the drawback of half adder circuit a single bit adder circuit called full adder is developed. It can add two one bit numbers A and B and Carry Cin

Block diagram



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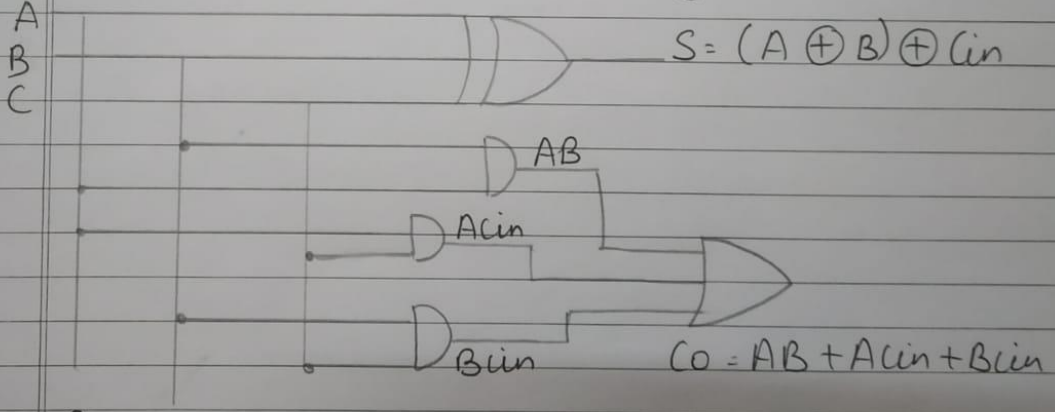
Truth table

Input			Output	
A	B	Cin	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder with basic gates



Conclusion: Hence we have the truth table of Full Adder and proved the result

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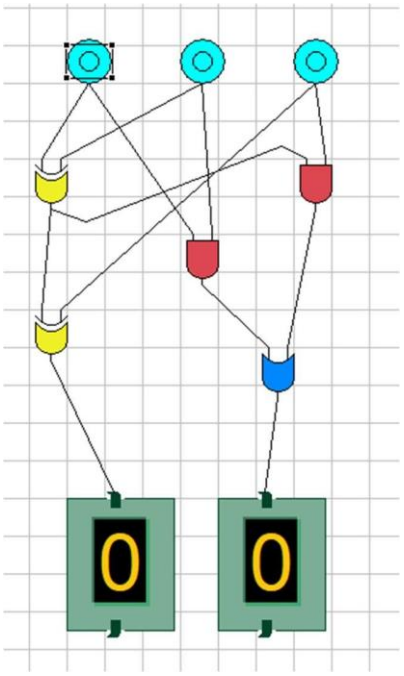
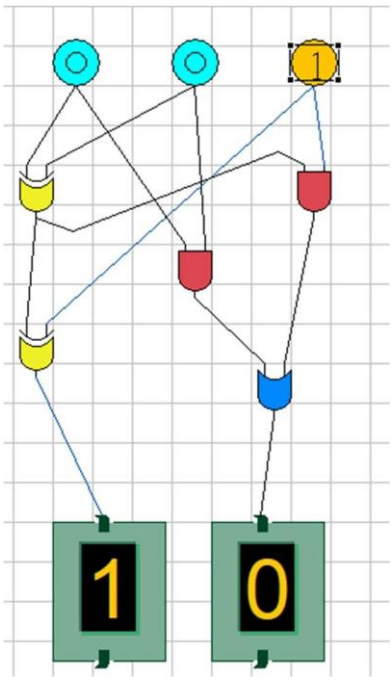
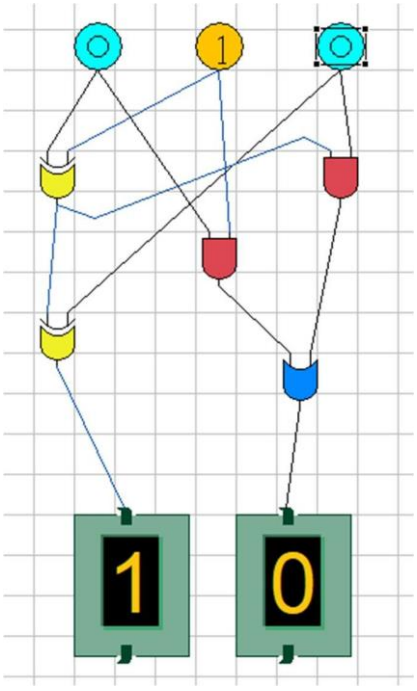
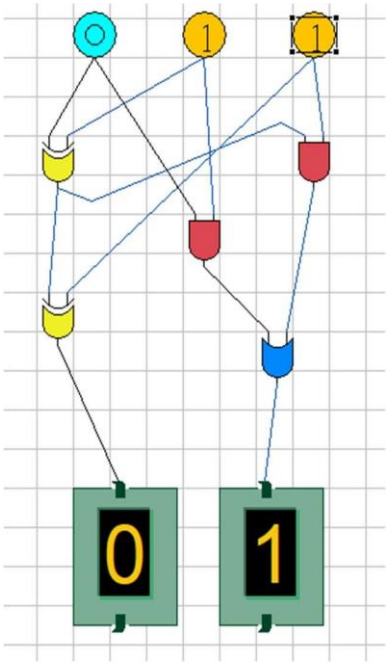
OUPUT:

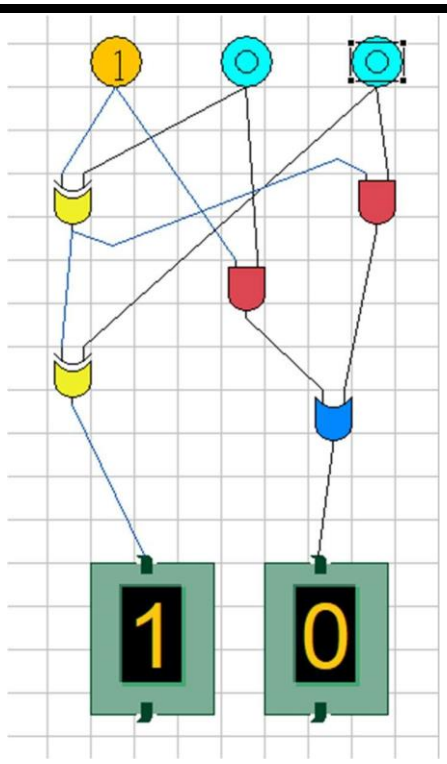
Full Adder:







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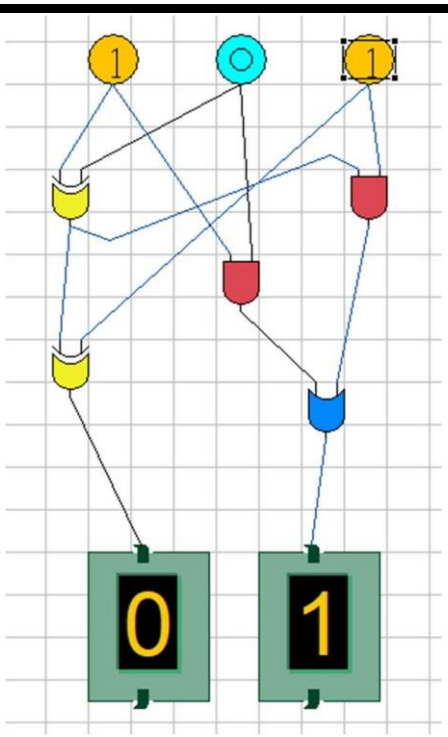
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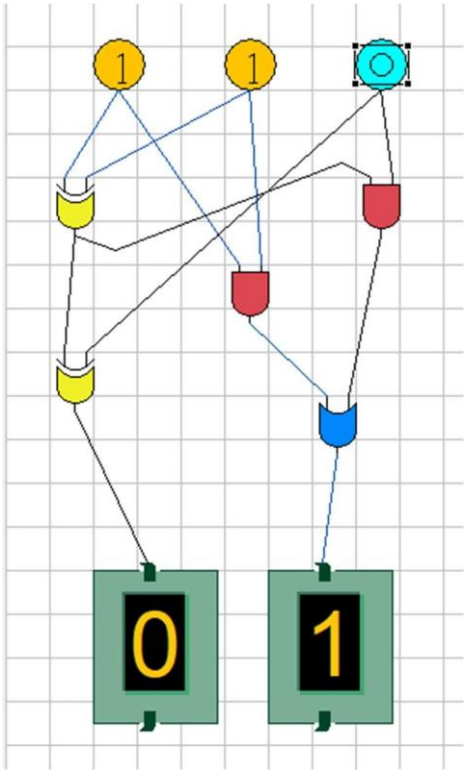
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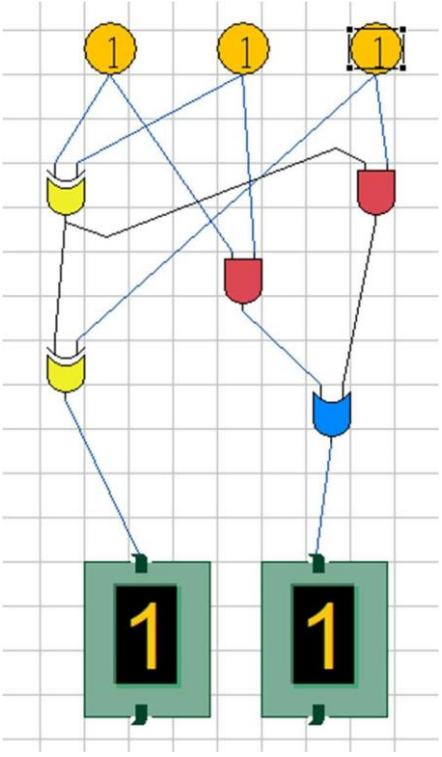
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