COMPUTER ENGINEERING

DLCA ODD SEM 2021-22/EXPERIMENT 1

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DLCOA Experiment 1.

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Date
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Aim : To study and verify the truth table of various logic gates using IC

Theory : To study and verify the truth table of various logic gates using IC.

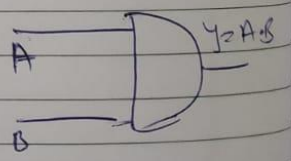
1) AND Gate :

The AND gate performs logical multiplication. The output is high when all input is high and low if any one of the input is low logical AND function.

$Y = A \cdot B$

Truth Table

A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1



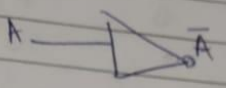
2) NOT Gate

The NOT gate performs inverting or complementing operation. It is thus also inverter. Then output is high when input is low and vice versa.
Logical NOT operation :

$Y = A = \overline{A}$

Truth Table

A	$Y = \bar{A}$
0	1
1	0



3) OR Gate:

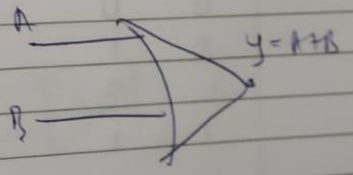
An OR gate with N inputs and one output. The OR operation is defined as the output of an OR gate is 1 if and only if one or more inputs are 1.

logical operation:

$Y = A + B$

Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

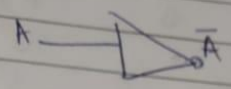


4) NOR Gate

The NOR gate is a OR gate with input inverted where the OR gate allows the output to be true if any one or more of its inputs are true the NOR inverts this and forces the output to logic 0 when any input is true.

Truth Table

A	$Y = \bar{A}$
0	1
1	0



3) OR Gate:

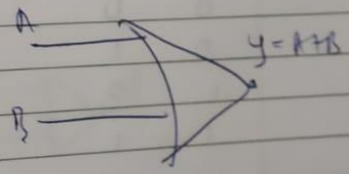
An OR gate with N inputs and one output. The OR operation is defined as the output of an OR gate is 1 if and only if one or more inputs are 1.

logical operation:

$Y = A + B$

Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

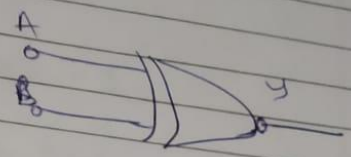


4) NOR Gate

The NOR gate is a OR gate with inverted output where the OR gate allows the output to be true if any one or more of its inputs are true the NOR inverts this and forces the output to logic 0 when any input is true.

Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

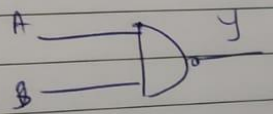


5) NAND gate :

The NOT AND operation is known as the NAND operation. The gate has n input AND gate followed by Not gate. The NAND is a AND gate with the compliment of the output

Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

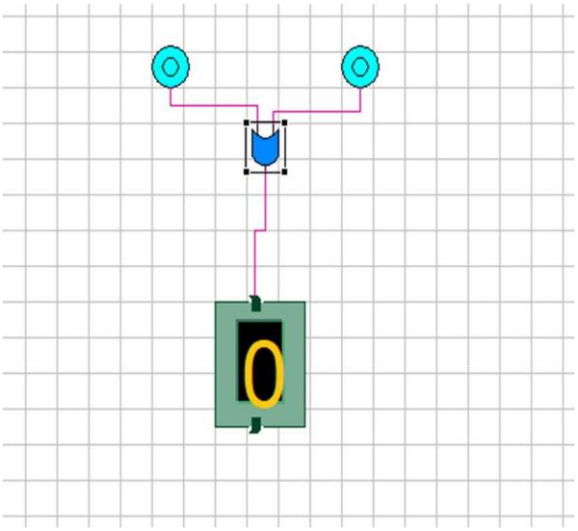


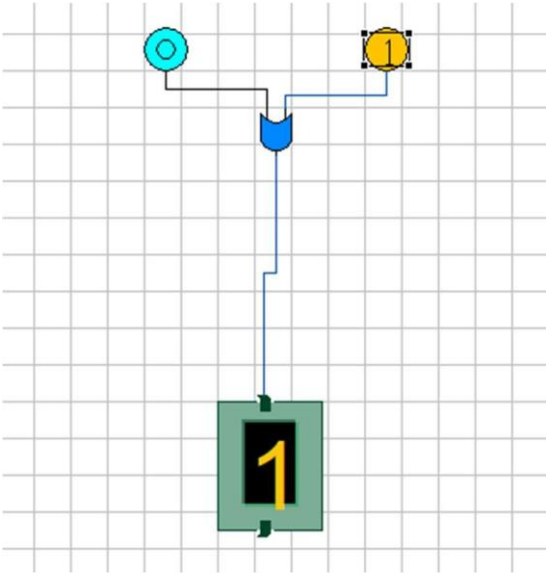
Conclusion :

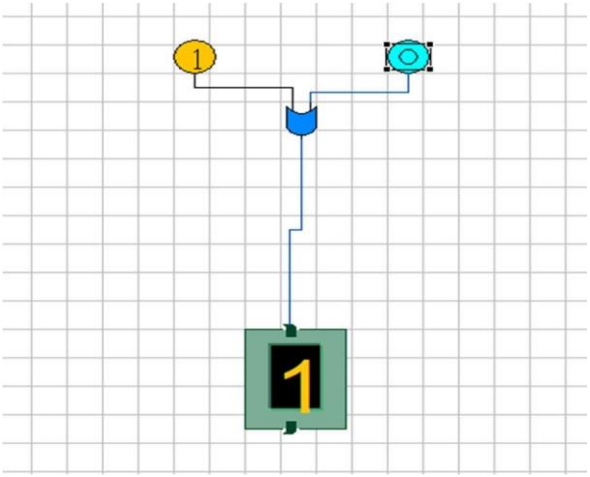
I have verified the truth table of various logic gate and proved the results.

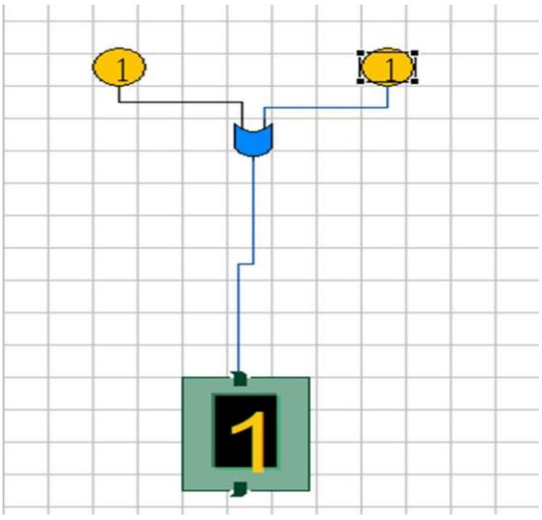
OUPUT:

Or gate :

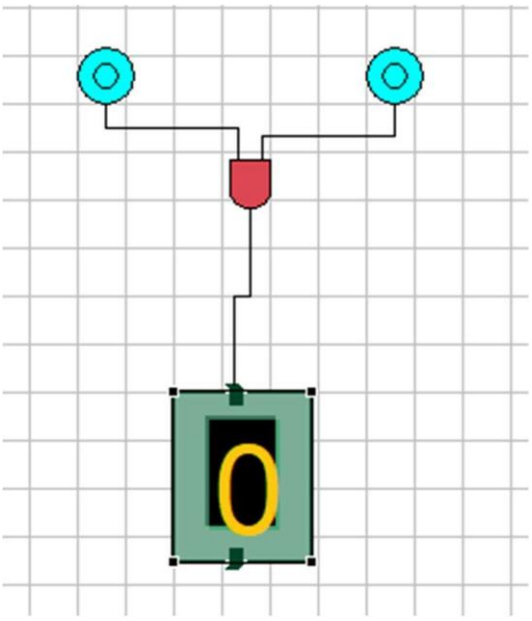


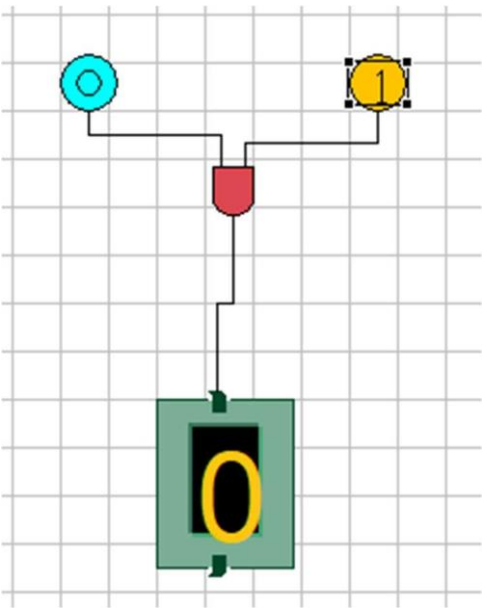


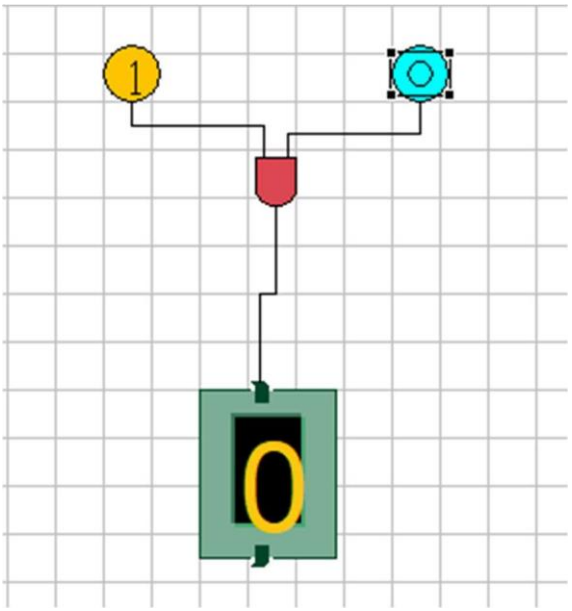


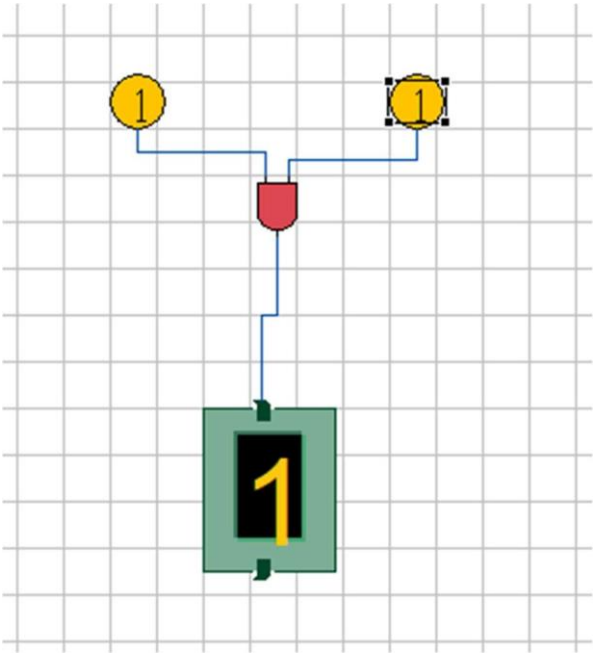


And Gate

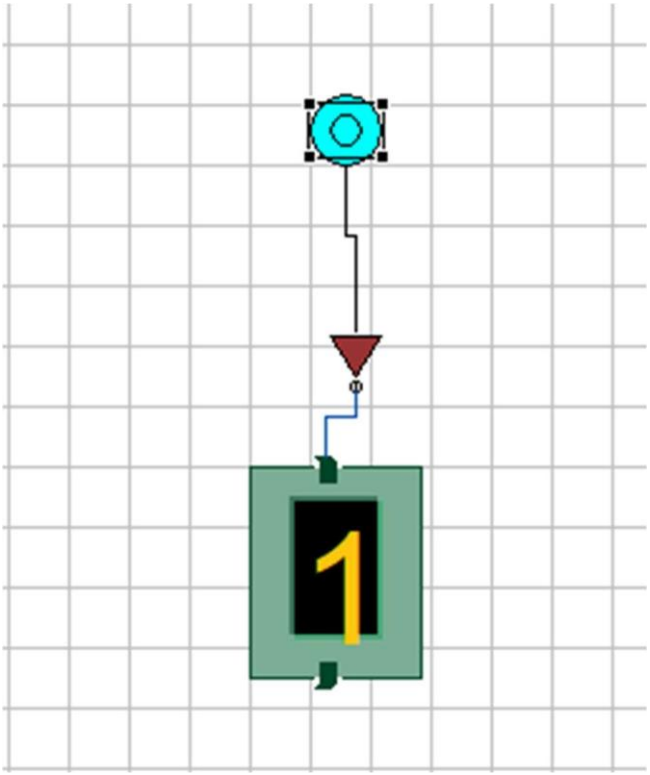


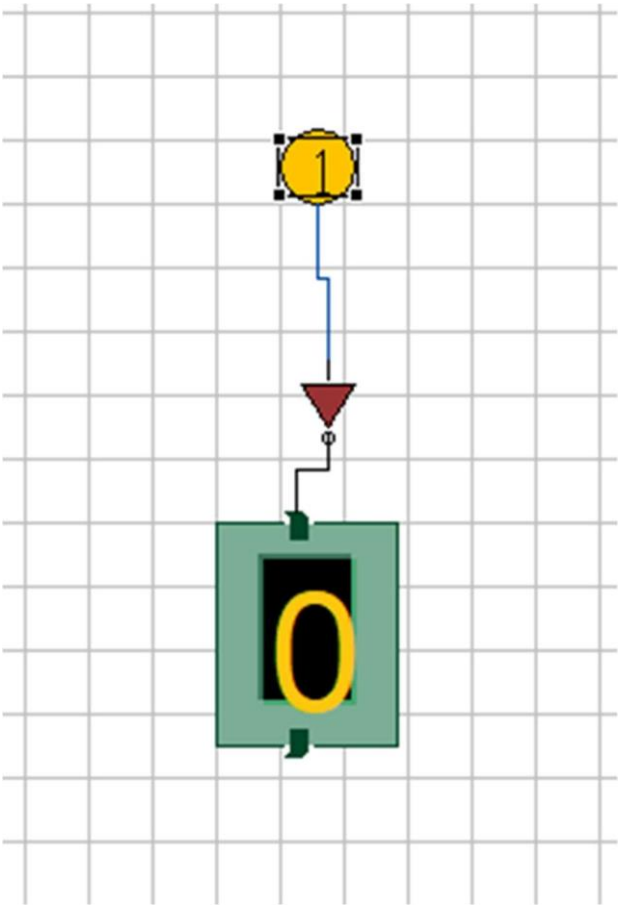




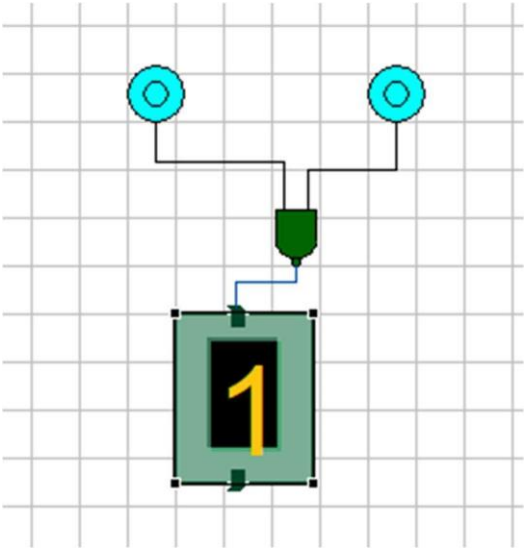


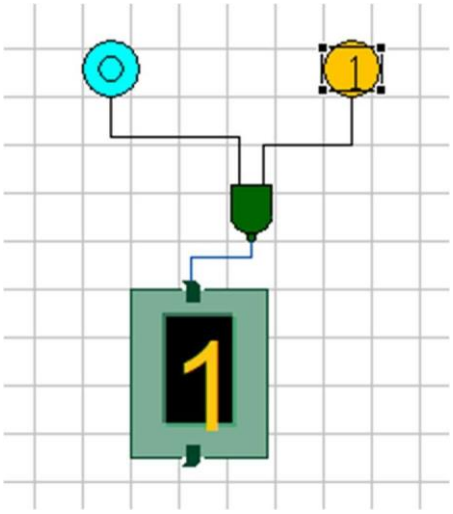
Not Gate

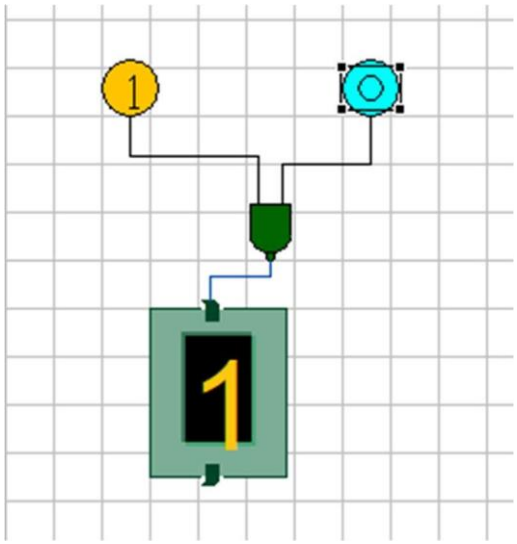


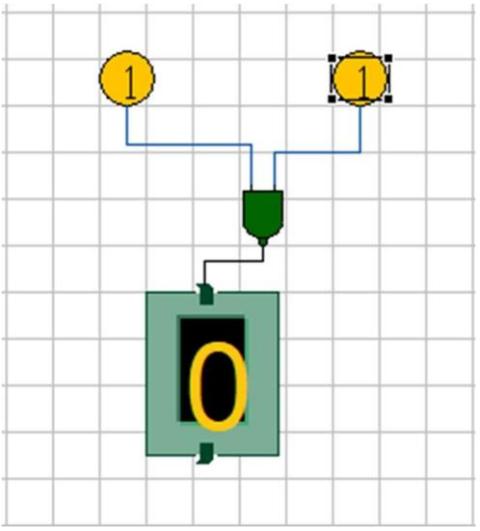


Nand Gate

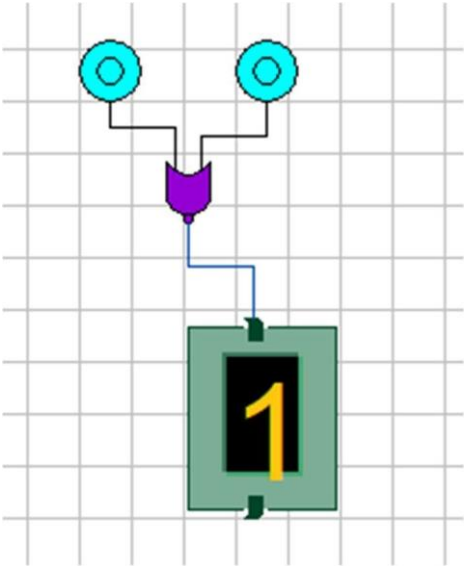


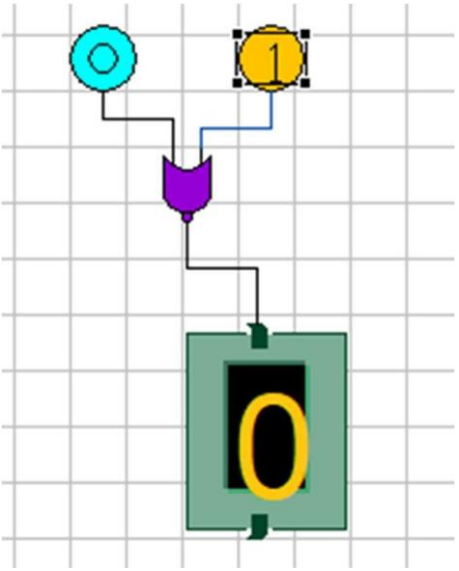


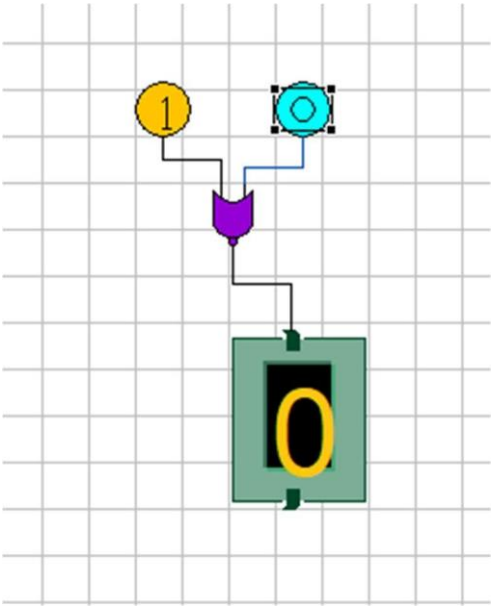


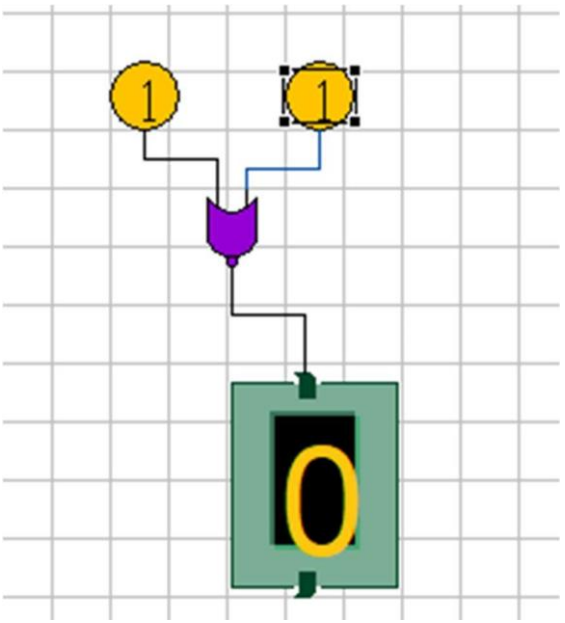


Nor gate

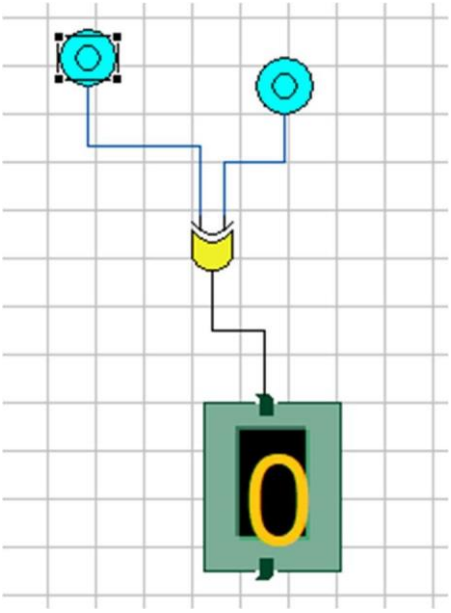


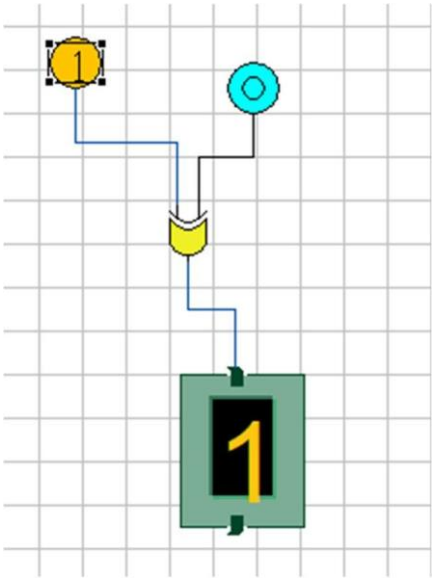


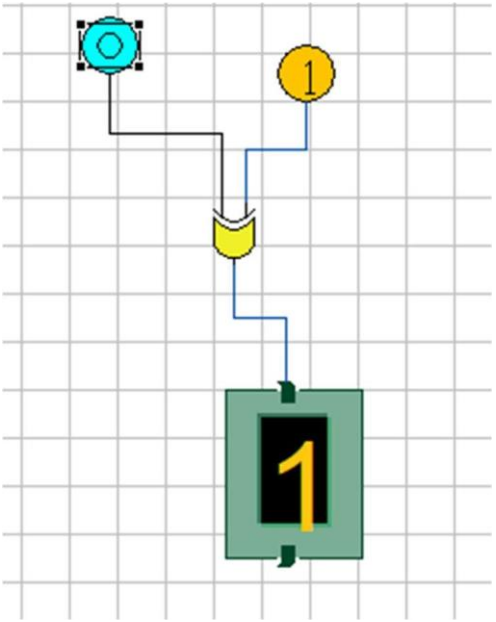


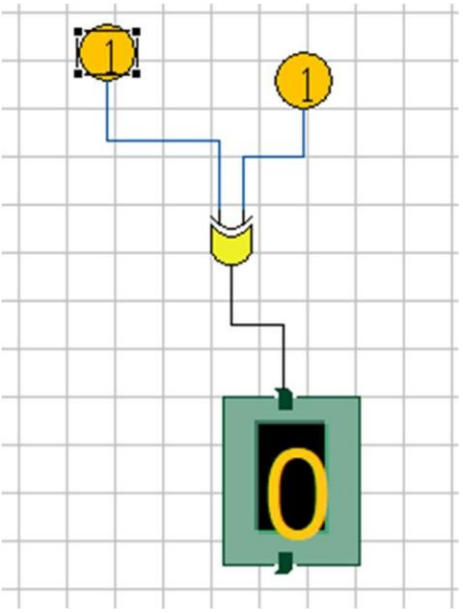


Ex Or gate









Ex nor gate