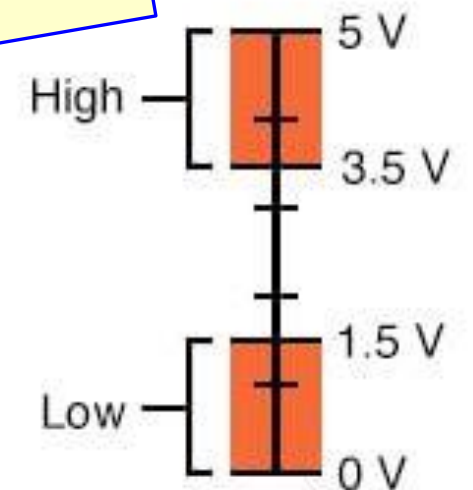
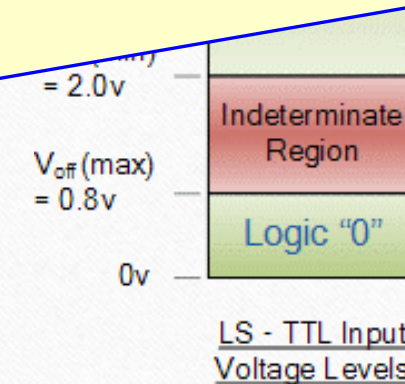
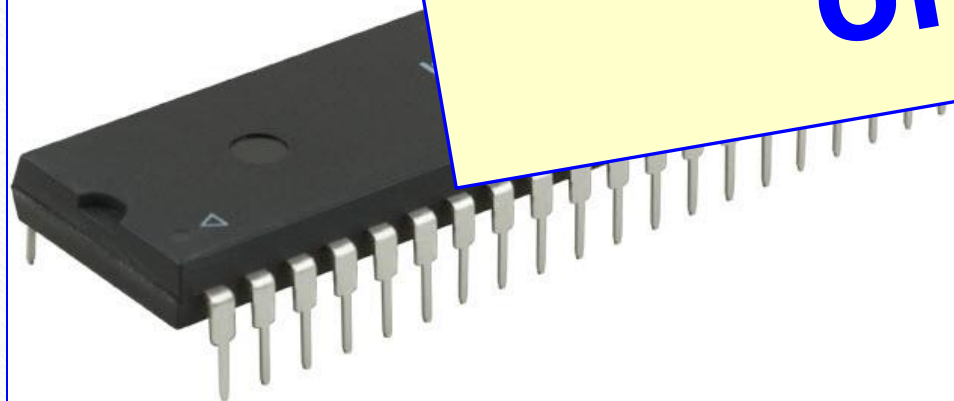


P1.0	1	40	VCC
P1.1	2	39	P0.0 (AD0)
P1.2	3	38	P0.1 (AD1)
P1.3	4	37	P0.2 (AD2)
P1.4	5	36	P0.3 (AD3)
P1.5	6	35	P0.4 (AD4)
P1.6	7	34	P0.5 (AD5)
P1.7	8	33	P0.6 (AD6)
RST	9		

Micro Controllers – 2.4 Addressing Modes of 8051....



CMOS Gate
Signal Levels

Addressing modes of 8051 :-

Addressing mode – It is a way to tackle / handle the Operand i.e. the Data.
Or a way to deal with the Data.

Different addressing modes of 8051 –

- 1) Immediate Addressing Mode
- 2) Register Addressing Mode
- 3) Direct Addressing Mode
- 4) Register Indirect Addressing Mode
- 5) Indexed Addressing Mode

Addressing modes of 8051 :-

1) Immediate Addressing Mode – Here the data to be transported is a part and parcel of the instruction itself.

e.g.

MOV A, #45H; Hexadecimal number 45 will be moved to Acc.

MOV R3, #0A3H; Hexadecimal number A3 will be moved to Register R3.

MOV DPTR, #1234H; Hexa. number 12 will go in DPH and 34 in DPL.

Size of the data and size of the register should be same. (MOV A, #245H; is illegal)

indicates that 45 is the data and not the address of a register.

0 (zero) is added prior to A, indicating that A is Hexadecimal number and not a character.

Addressing modes of 8051 :-

2) Register Addressing Mode – Here the data to be transported is stored in a register of source or destination and the name of the register is in the instruction.

e.g.

MOV A, R6; Contents of register R6 are shifted to Acc.

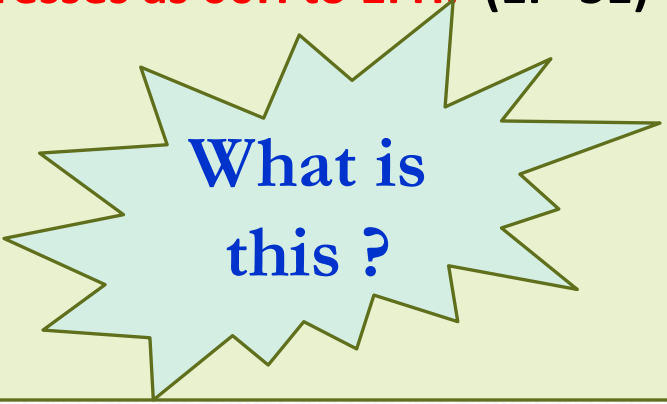
MOV R3, A; Contents of Accumulator are shifted to register R3

All registers are named as R0 to R7 only, with respective addresses as 00H to 1FH. (1F=31)

Proper precaution should be taken while coding the PSW.

Register to Register transfer is not allowed.

Thus, **MOV R5, R6;** is illegal.



What is
this ?

Addressing modes of 8051 :-

3) Direct Addressing Mode –

e.g.

MOV R2, 45H;

MOV 46H, 45H;

Here the data stored in the RAM location 45 H is moved to register R2.

Understand the difference between #45H and 45H

The 128 RAM locations are 00H to 7FH (7F = ??)

The SFRs have addresses starting from 80H to F0H (with gaps)

MOV P0, #45H; Data 45 is copied to Port 0

MOV P0, 45H; Contents of memory location 45 are copied to Port 0

MOV 80H, 45H; What is this ???

–: Addresses of the 21 SFRs :–

8A – TL0

8B – TL1

8C – TH0

8D – TH1

88 – TCON*

89 – TMOD

98 – SCON*

99 – SBUF

82 – DPL

83 – DPH

87 – PCON

80 – P0* (Port 0)

90 – P1* (Port 1)

A0 – P2* (Port 2)

B0 – P3* (Port 3)

E0 – A* (Accumulator)

F0 – B* (Extension of A)

81 – SP

D0 – PSW*

A8 – IE* (Interrupt)

B8 – IP* (Interrupt)

Note – There are gaps in the addresses of the SFRs.

Put a leading 0 if the address starts with a alphabet. e.g. 0A0, 0E0

Registers with a * are bit and byte addressable. Other only byte addressable.

Addressing modes of 8051 :-

4) Register Indirect Addressing Mode – Here a register will have an address in it and at that address there will be some data stored.

`MOV A, @R0;`

here the data stored in the register is say for e.g. 3CH. This is a RAM location where the actual data will be found. That data will be moved to the Acc.

“Only R0 and R1” from all banks can be addressed like this. (Not for R2 to R7)

R0 and R1 are called as “pointer registers” in the Register Indirect Addressing Mode.

Thus, `MOV A, @R4;` is illegal.

Addressing modes of 8051 :-

5) Indexed Addressing Mode –

MOVC A, @A+DPTR;

MOVC A, @A+PC;

Current contents of Acc. are added to contents of the DPTR. This will give a new number, which is address of memory location where the data is stored.

DPTR has 16 bit address (DPH and DPL) which is added to 8 bit contents of Acc.

Destination is always Acc.

e.g. DPTR = 01F3H and A = 08H 1) What are the contents of the A ?

Find the address

2) What is the data ?

Ans : 01FB.

8051 Microcontroller assembly language instruction set

8051 Microcontroller Instructions and Groups

<i>DATA TRANSFER</i>	<i>ARITHMETIC</i>	<i>LOGICAL</i>	<i>BOOLEAN</i>	<i>PROGRAM BRANCHING</i>
MOV	ADD	ANL	CLR	LJMP
MOVC	ADDC	ORL	SETB	AJMP
MOVB	SUBB	XRL	MOV	SJMP
PUSH	INC	CLR	JC	JZ
POP	DEC	CPL	JNC	JNZ
XCH	MUL	RL	JB	CJNE
XCHD	DIV	RLC	JNB	DJNZ
	DAA	RR	JBC	NOP
		RRC	ANL	LCALL
		SWAP	ORL	ACALL
			CPL	RET
				RETI
				JMP