VISHWAKARMA INSTITUTE OF TECHNOLOGY

Department of Engineering, Sciences and Humanities

FY – 2022-2023 -SEM II

ES1045: Computer Organization and Architecture

HOME ASSIGNMENT NO 5

Q. N.	CO No	BT* No	Description	Max marks
1	CO5	4	Draw and Explain Memory Hierarchy with reference to following parameters cost per bit, Size of the memory and speed of the Memory.	**3**
2	CO5	2	What is Locality of Reference? Explain Spatial Locality and temporal Locality with Example.	**3**
3	CO5	2	What is a ROM? What are different types of ROM and explain how do they differ from each other?	**4**
4	CO5	4	Difference between Static RAM and Dynamic RAM.	**3**
5	CO5	4,5	Consider a machine with a byte addressable main memory of size 128KB and block size of 256 bytes. Assume that a direct mapped cache consisting of 64 lines is used with this machine. How is Physical address divided into tag, index, and word? Also find size of cache memory.	**4**
6	CO5	4,5	A certain processor uses associative cache of size 16 KB. The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32 bit address. How many bits are required for tag and word offset field respectively in the address generated by the processor? Also find size of main memory.	**4**
7	CO5	4,5	Consider a 2 – way set associative cache of size 1MB.The cache block size is 128 bytes. Assume that the main memory is byte addressable and having size 256MB. How many bits are required for tag, set and word respectively?	**4**

Important Note: Last date of assignment submission is 15th May 2023.