Bansilal Ramnath Agarwal Charitable Trust's

VISHWAKARMA INSTITUTE OF TECHNOLOGY, PUNE – 411037.

(An Autonomous Institute Affiliated to Savitribai Phule Pune University)

Examination: ESE

Year: SY **Branch:** IT

Subject: Digital Electronics and Microprocessor **Subject Code:** IT2275

Max. Marks: 60 **Total Pages of Question Paper:** 2

Day & Date: Wed 23/11/2023 **Time:** 02:30 pm to 4:30 pm

Instructions to Candidate

1. All questions are compulsory.
2. Neat diagrams must be drawn wherever necessary.
3. Figures to the right indicate full marks.

Q. No.	CO No	BT* No		Max marks
Q. 1.			**Attempt the following**	
a)	1	1,2	Simplify the following Boolean expression using k-map $Y(A,B,C,D)= \sum m(0,1,2,3,4,5,6,11)$ $Y(A,B,C,D)= \sum m(0,1,2,3,4,7,8,9,10,11,12,14)$	6M
b)	1	1,2	Explain standard SOP form. Convert F (A, B, C, D) = $\bar{A}$+BCD +AC in to standard SOP form.	4M
Q. 2.			**Q. 2 (a) is compulsory and attempt any one from Q.2 (b) and Q.2 (c)**	
a)	2	3	Design a combinational logic circuit with four input variables that will produce logic 1 output when the number of 1s in the inputs is even.	6M
b)	2	3	Implement the following expression using 4:1MUX $Y(A,B,C)=\sum m(0,1,2,6,7)$	4M
c)	2	3	Design full adder using 3:8 decoder.	4M
Q. 3.			**Q. 3 (a) is compulsory and attempt any one from Q.3 (b) and Q.3 (c)**	
a)	3	2	Describe J-K Flip-flop with neat circuit diagram and excitation table.	6M
b)	3	1,2	Draw circuit diagram for MOD 6 UP counter using J-K flip flop	4M
c)	3	1,2	Draw the neat circuit diagram for 4 – bit UP ripple counter using J-K flip-flop.	4M
Q. 4.			**Q. 4 (a) is compulsory and attempt any one from Q.4 (b) and Q.4 (c)**	
a)	4	1	Enlist different addressing modes supported by 8086 explain one example for each.	6M
b)	4	2	Discuss physical address translation and find the physical address if CS=1A1A IP=1B1B.	4M
c)	4	2	Describe the memory segmentation with neat diagram.	4M

Q. 5.			**Attempt the following**	
a)	5	2	Differentiate between minimum and maximum mode with respect to pin functions of 8086	6M
b)	5	1	Draw the flag register for 8086 and explain each filled.	4M
Q. 6.			**Attempt the following**	
a)	6	2,3	Discuss and draw the Interrupt Vector Table.	4M
b)	6	2,3	Draw and describe the control word of 8254-Programmable Interval timer/counter	6M

CO Statements:

CO1: To understand all the concepts of Logic Gates and Boolean Functions.
CO2: To learn about Combinational Logic and Sequential Logic Circuits.
CO3: To design Combinational Logic and Sequential Logic Circuits.
CO4: To understand basics of 8086 Microprocessor and 8051 Microcontroller.
CO5: To understand architecture of 8086 Microprocessor and 8051 Microcontroller.
CO6: To learn Assembly Language Programming of 8086 and 8051.

***Blooms Taxonomy (BT) Level No:**

- 1.Remembering; 2. Understanding; 3. Applying; 4. Analyzing; 5. Evaluating; 6. Creating