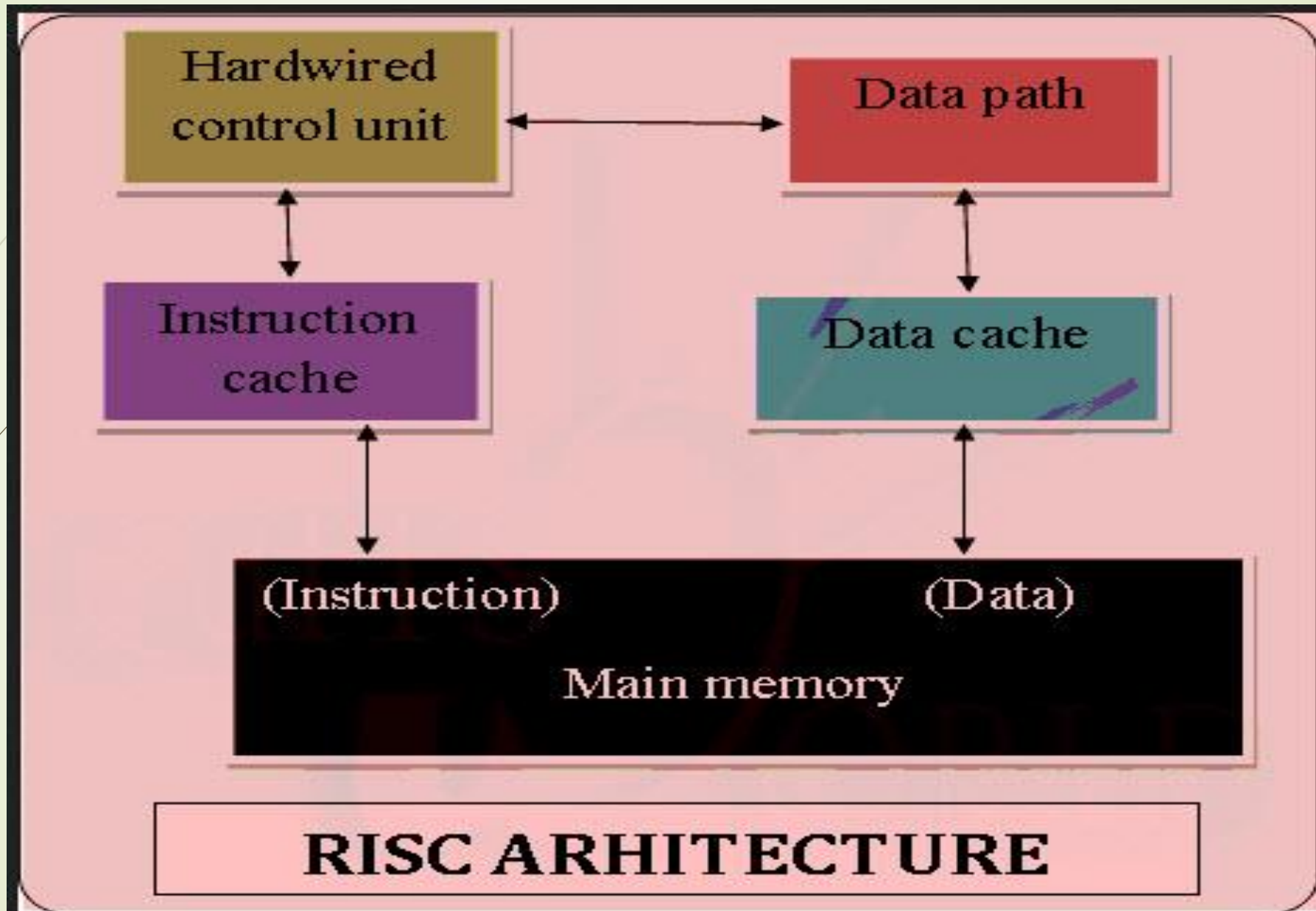# RISC Processors

By

Smita Mande

RISC
Reduced Instruction Set Computer Processor

- The main idea behind this is to make hardware simpler by using an instruction set composed of a few basic steps for loading, evaluating, and storing operations just like a load command will load data, a store command will store the data.

- It is built to minimize the instruction execution time by optimizing and limiting the number of instructions.

- each instruction cycle requires only one clock cycle, and each cycle contains three parameters: fetch, decode and execute

- RISC chips require several transistors, making it cheaper to design and reduce the execution time for instruction.

- Examples : SUN's SPARC, PowerPC, Microchip PIC processors, RISC-V.

Hardwired control unit

Data path

Instruction cache

Data cache

(Instruction)

(Data)

Main memory

RISC ARHITECTURE

Characteristic of RISC –

1. Simpler instruction, hence simple instruction decoding.

2. Instruction comes under size of one word.

3. Instruction takes a single clock cycle to get executed.

4. More general-purpose registers.

5. Simple Addressing Modes.

6. Fewer Data types.

7. A pipeline can be achieved.

8. Fixed length instruction format

CISC
Complex Instruction Set Architecture

- The main idea is that a single instruction will do all loading, evaluating, and storing operations just like a multiplication command will do stuff like loading data, evaluating, and storing it, hence it's complex.

- CISC approaches reducing the number of instruction on each program and ignoring the number of cycles per instruction

- It emphasizes to build complex instructions directly in the hardware because the hardware is always faster than software.

- CISC chips are relatively slower as compared to RISC chips

- Examples: VAX, AMD, Intel x86 and the System/360.
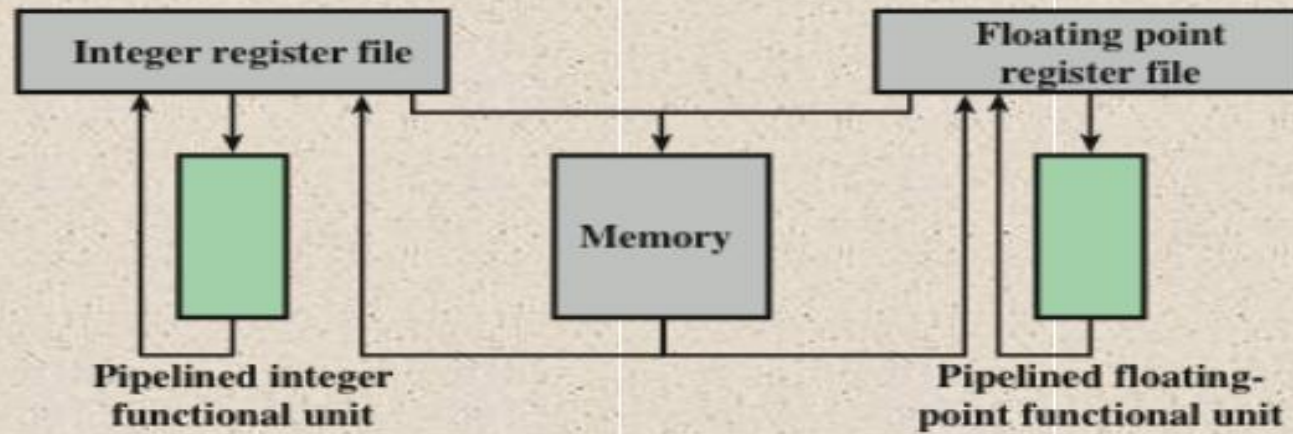
CISC ARCHITECTURE
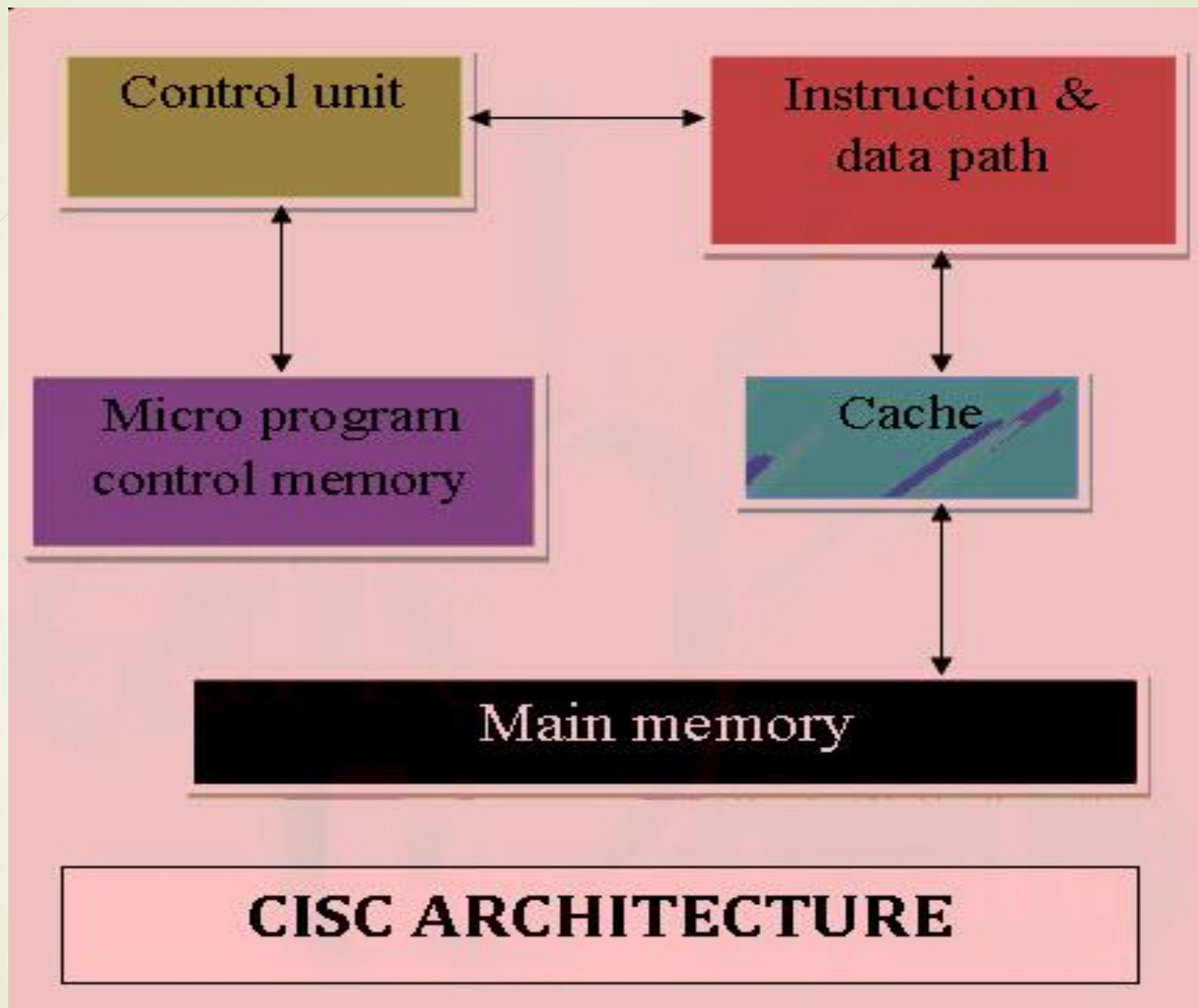
Characteristic of CISC –

1. Complex instruction, hence complex instruction decoding.

2. Instructions are larger than one-word size.

3. Instruction may take more than a single clock cycle to get executed.

4. Less number of general-purpose registers as operations get performed in memory itself.

5. Complex Addressing Modes.

6. More Data types.

7. Variable length instruction format
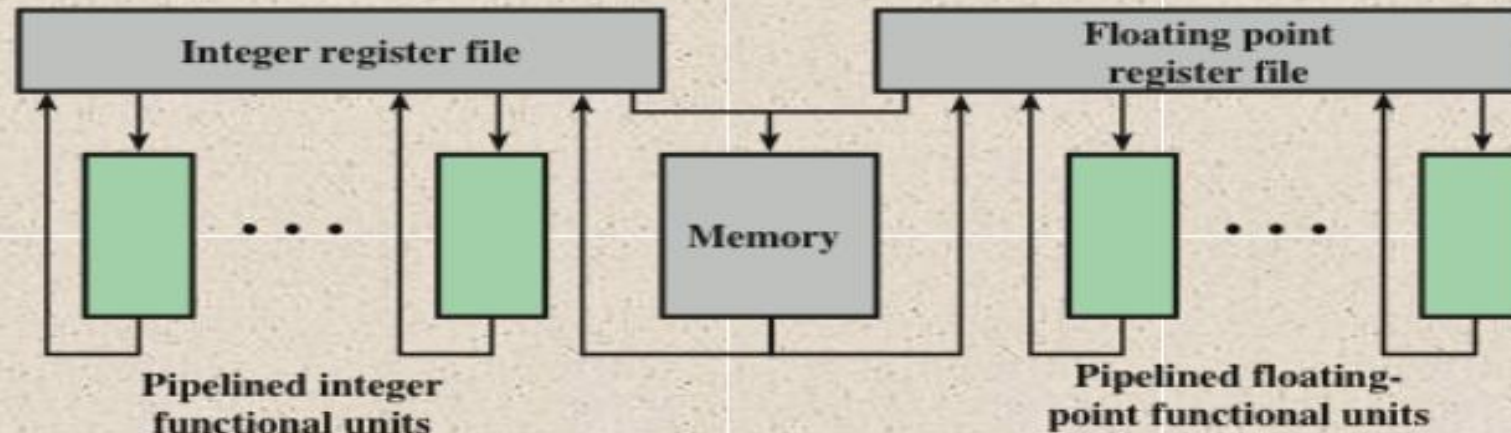
Difference between the RISC and CISC Processors

RISC	CISC
It emphasizes on software to optimize the instruction set.	It emphasizes on hardware to optimize the instruction set.
It requires multiple register sets to store the instruction.	It requires a single register set to store the instruction.
RISC has simple decoding of instruction.	CISC has complex decoding of instruction.
Uses of the pipeline are simple in RISC.	Uses of the pipeline are difficult in CISC.
It uses a limited number of instruction that requires less time to execute the instructions.	It uses a large number of instruction that requires more time to execute the instructions.
The execution time of RISC is very short.	The execution time of CISC is longer.
RISC architecture can be used with high-end applications like telecommunication, image processing, video processing, etc.	CISC architecture can be used with low-end applications like home automation, security system, etc.
It has fixed format instruction.	It has variable format instruction.
The program written for RISC architecture needs to take more space in memory.	Program written for CISC architecture tends to take less space in memory.
Example of RISC: ARM, PA-RISC, Power Architecture, Alpha, AVR, ARC and the SPARC.	Examples of CISC: VAX, Motorola 68000 family, System/360, AMD and the Intel x86 CPUs.

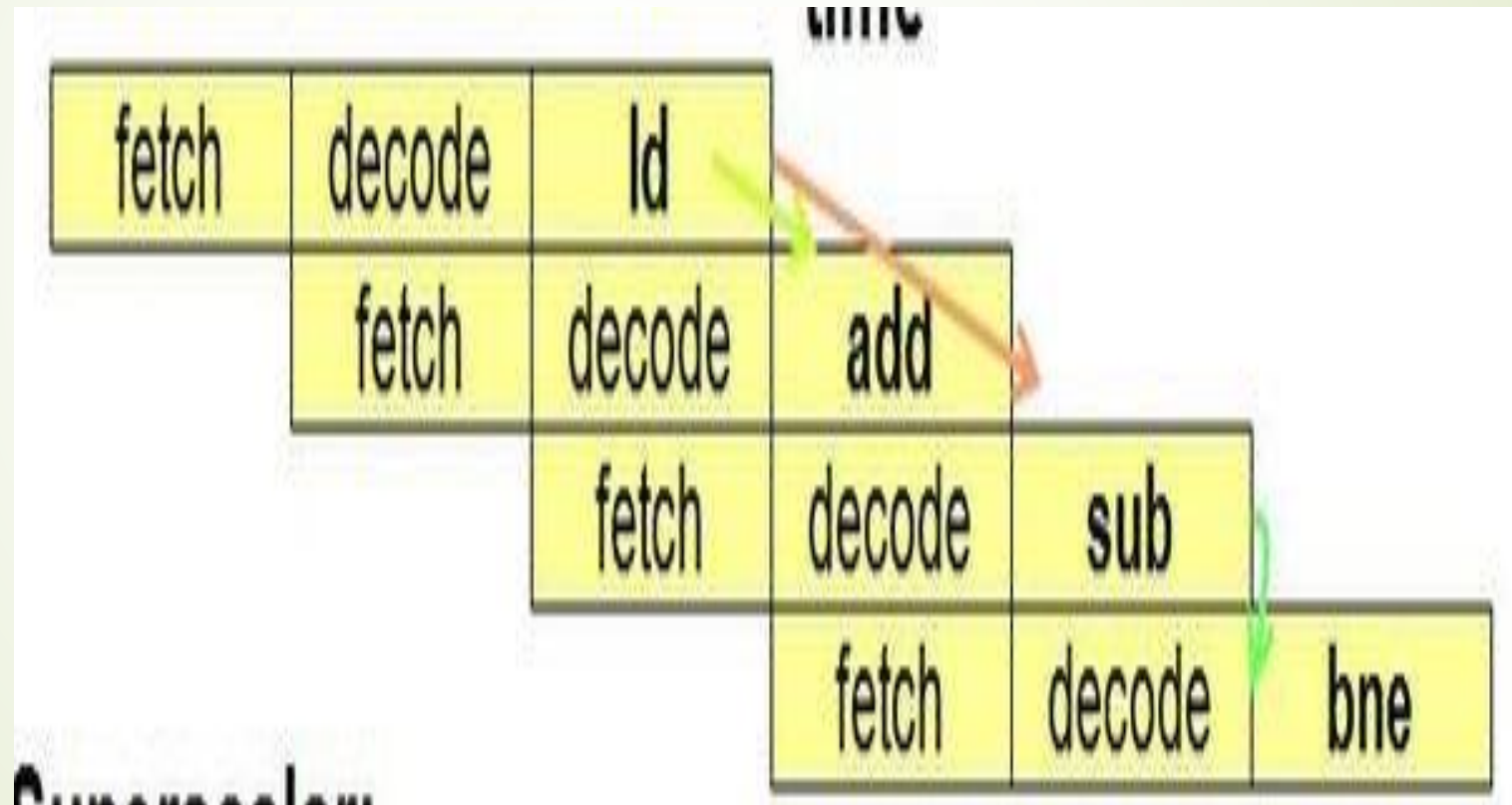Figure 16.1 Superscalar Organization Compared to Ordinary Scalar Organization
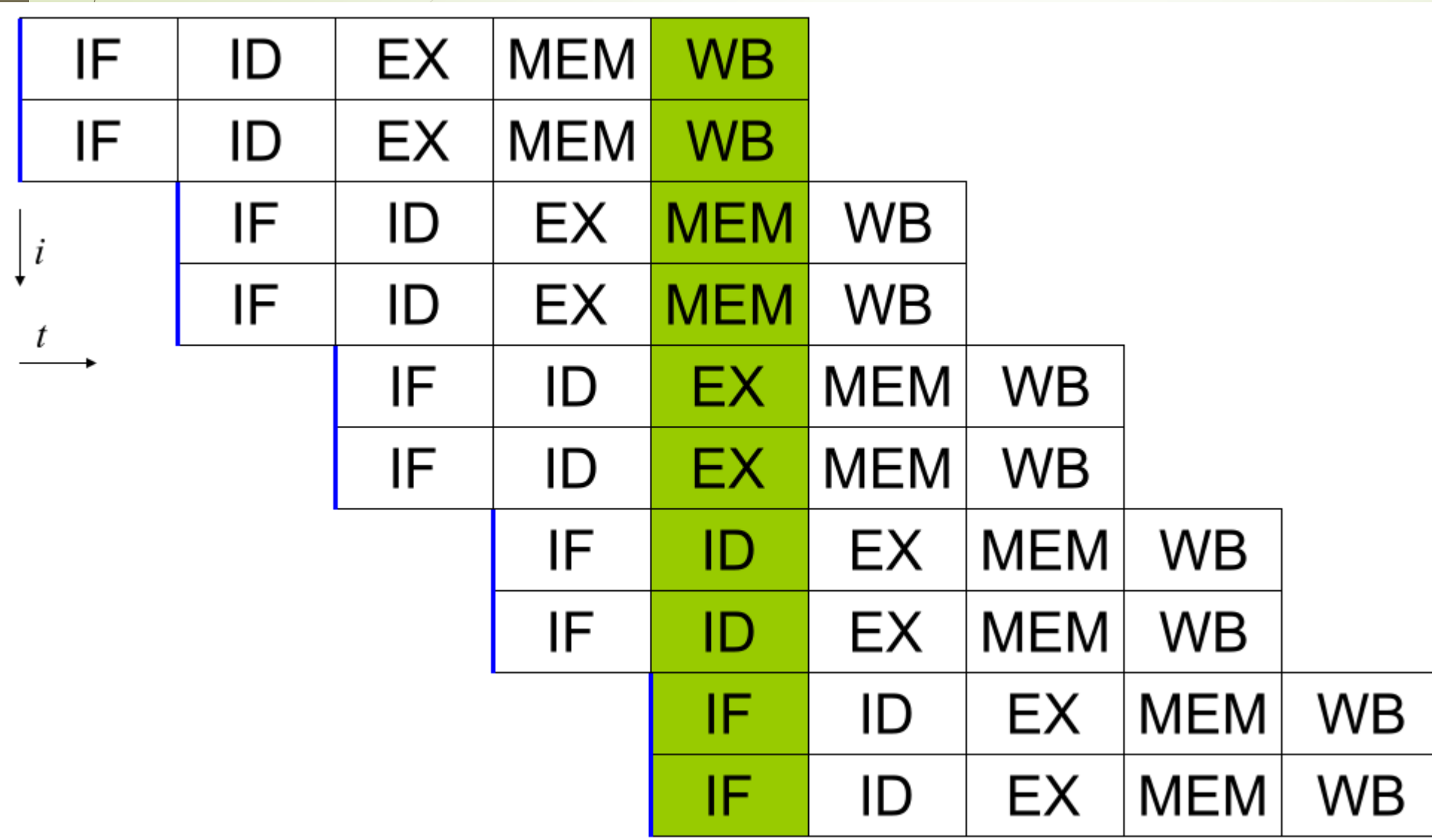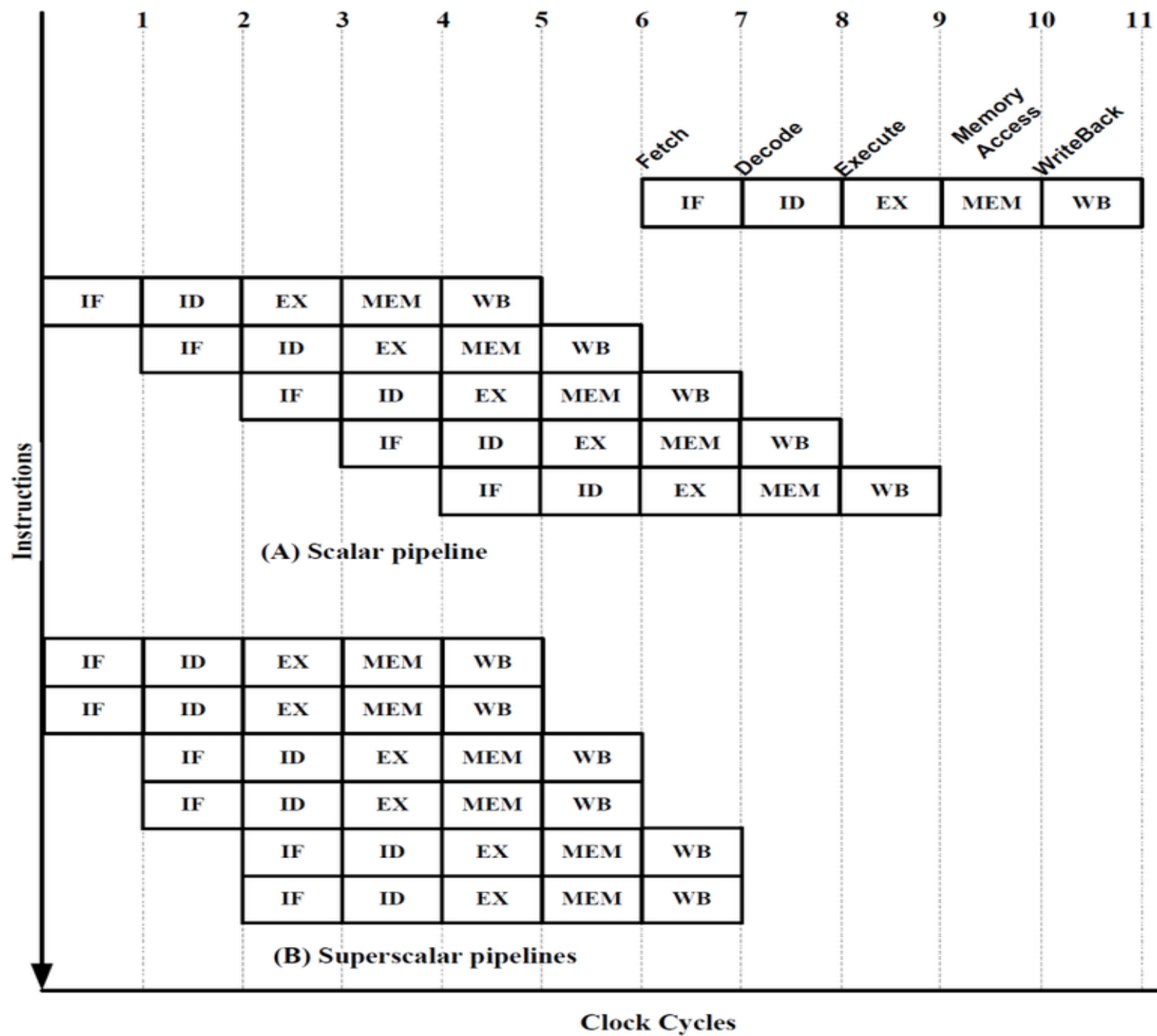
A scalar processor is one where instructions are executed in a pipeline as below but only a single instruction can be fetched or decoded in a single cycle.

A super scalar processor on the other hand can have multiple parallel instruction pipelines. A 2-way super scalar processor can fetch two instructions per cycle and supports two parallel pipeline as below

IF	ID	EX	MEM	WB				
IF	ID	EX	MEM	WB				
	IF	ID	EX	MEM	WB			
	IF	ID	EX	MEM	WB			
		IF	ID	EX	MEM	WB		
		IF	ID	EX	MEM	WB		
			IF	ID	EX	MEM	WB	
			IF	ID	EX	MEM	WB	
				IF	ID	EX	MEM	WB
				IF	ID	EX	MEM	WB

(A) Scalar pipeline

(B) Superscalar pipelines

Super pipeline Performance

- The performance is shown below in the figure:
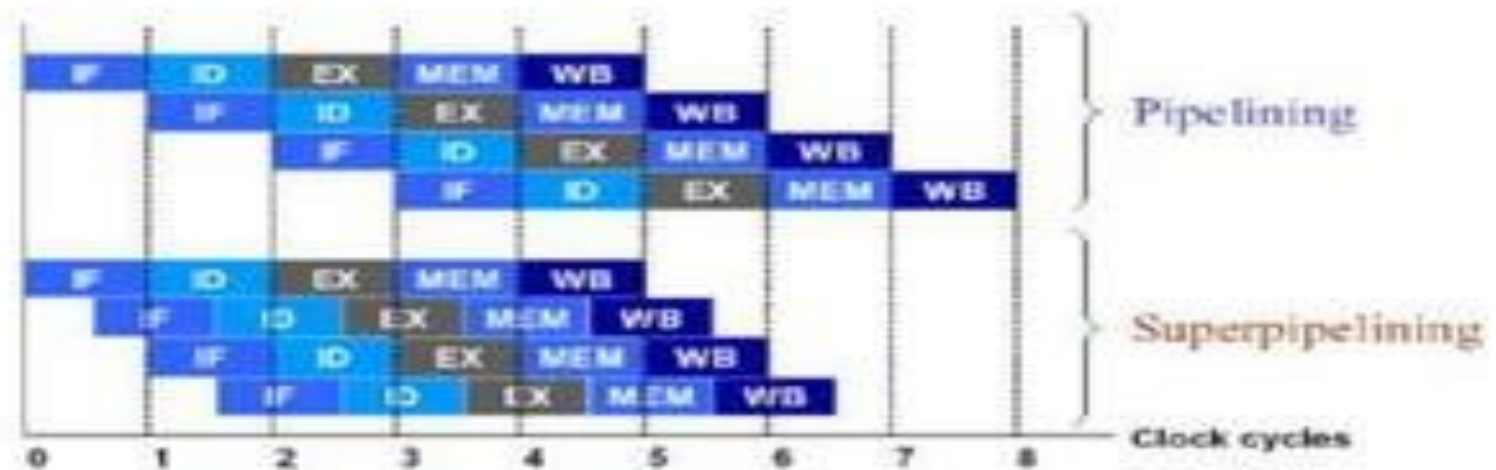
It is capable of performing two pipeline stages per cycle

Superscalar vs. Superpipelined

A comparison of a superpipelined and a superscalar approach to a base machine with an ordinary pipeline.