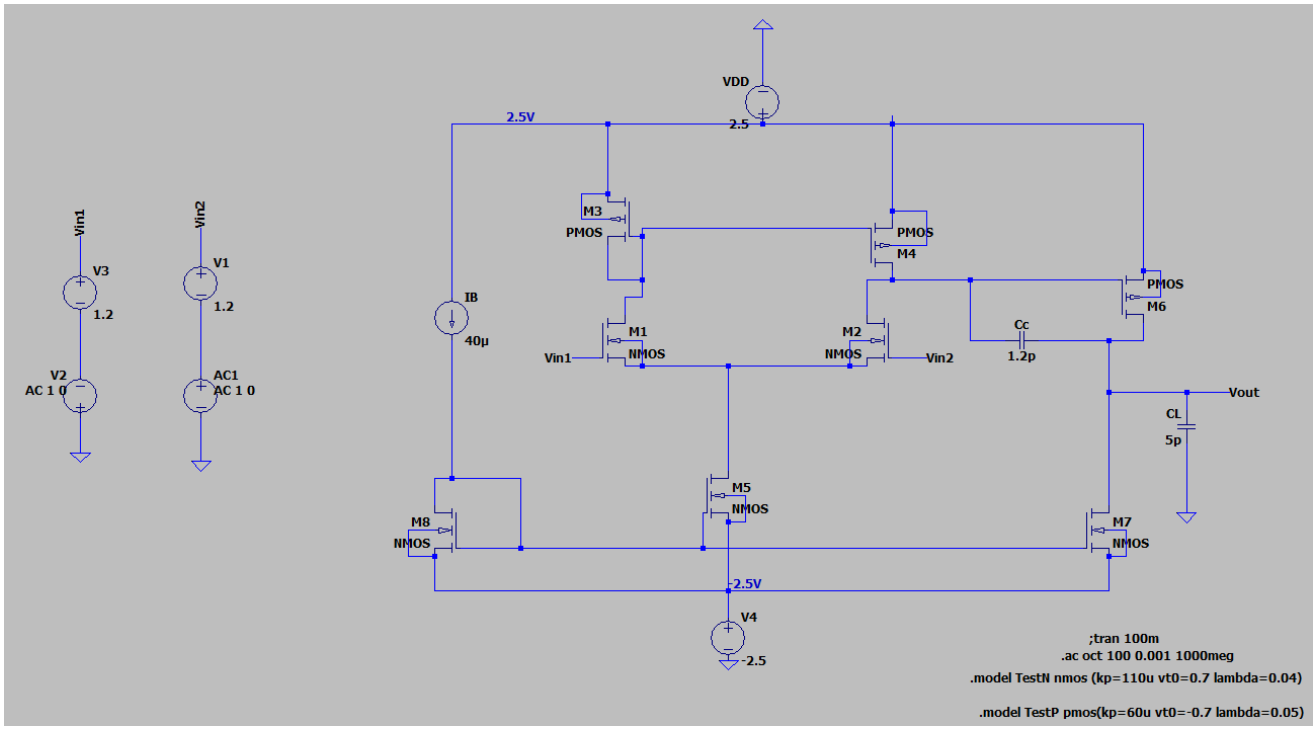
UDYAM'24

Commnet Problem Statement 1 TEAM-:OHMAZING



DESIGN OF TWO STAGE MILLER COMPENSATED OP-AMP USING MOSFET

-: Team Members:-

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Abstract :

In this project, we design and analyse a two-stage differential amplifier using metal-oxide-semiconductor field effect transistor (MOSFET) technology. The amplifier incorporates Miller compensation to enhance stability and performance. We explore the design steps, simulation results, and practical considerations.

Overview :

Design Specifications :

As per given in the problem statement we are supposed to design a two stage miller compensated opamp with following specifications : Gain Bandwidth of 50MHz , DC gain of 2000 , Capacitive load = 5pf , Phase margin >= 60deg , input common mode range 0.7 to 1.6 V , and suitable length and width of each nmos and pmos transistor .

About Circuit :

1) The circuit is made up of a total 8 mosfet out of which 3 are pmos and rest are nmos .
2) M3 and M4 are identical due to circuit mirroring and hence equal current flows from them also they have the same W/L values . The source terminal of M3 and M4 is at Vdd and the substrate terminal is connected to its source terminal respectively . Same goes for M1 and M2 .
3) The drain terminal of M1 and M2 are connected to the drain of M3 and M4 . Hence Vs3 = Vs4 = Vdd also Vd3 = Vg3 = Vd1 and Vd4 = Vg4 = Vd2 . These relations are further used in the calculations .

Concept and Theory :

A differential amplifier is a circuit that amplifies the difference between two input signals. Differential amplifiers are significant components in analogue systems' ICs .The voltage difference present at the inverting and non-inverting terminal gets amplified where the output is received.

Multiple stage amplifiers can be implemented to achieve higher gain circuits . A two stage opamp can provide high gain and high output swing . A two stage miller opamp will have two poles in its transfer function . Therefore a frequency compensation circuit must be implemented to ensure its stability. We can do this by approximating the two pole behaviour to single pole behaviour over a certain frequency range according to circuit design .

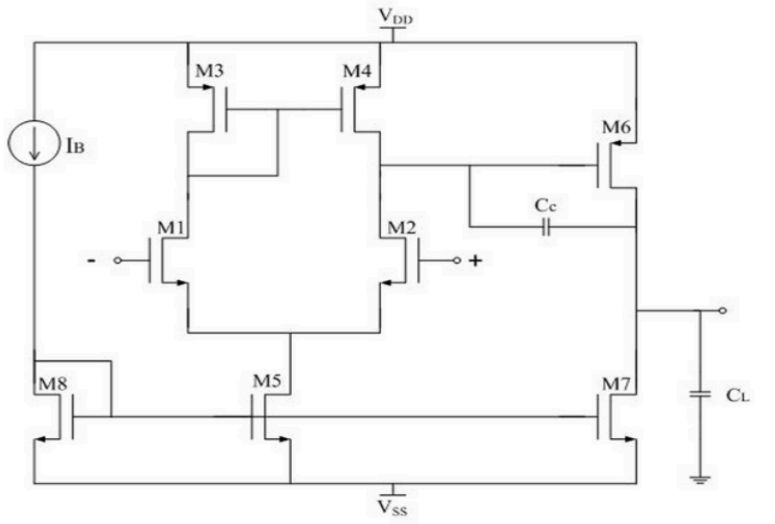


Figure 1: NMOS Two Stage op amp

Phase margin is the amount of phase shift when the amplifier's gain passes through 0dB. It is basically a measure of how close the second pole of the system is to causing instability. Phase starts to change on the order of a decade before the corner frequency. The phase shift must be less than 180°. The phase margin is 180°—the actual phase shift of the amplifier. Anything greater than 45° is usually acceptable. The higher the phase margin, the more stable the system.

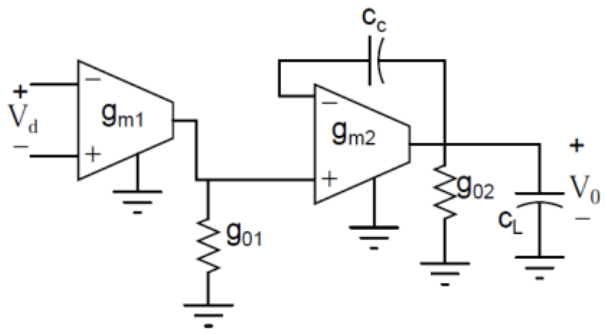


Figure 2: Block level representation of 2-stage Miller compensated OTA .

Basically in two stage amplifiers , the name itself suggests that there are two cascading amplifiers . The first one is a differential amplifier and the second one is a high gain amplifier .

About Miller Compensation :

Miller compensation uses a capacitor to bypass a stage (here it is present at output of first stage and second stage) in the amplifier at high frequencies, thereby eliminating the pole that stage creates . As we are dealing with stability of the op amp by trying to eliminate the effect of the second pole , this method is useful in that respect .The Miller effect makes one pole more dominant by moving the pole down in frequency, while the other becomes less dominant by moving the pole up in frequency (pole splitting). This helps us to achieve required phase margin .

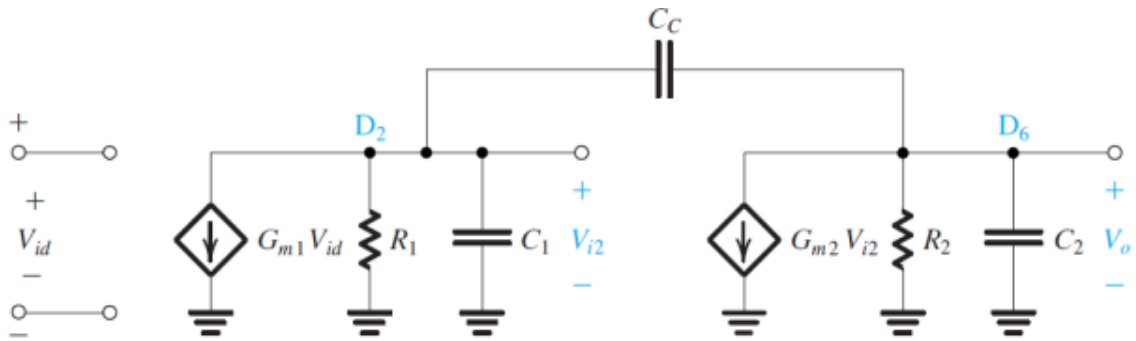


Figure 3:Small Signal model of Miller compensated opamp

Design Steps :

Following transistors parameter are known for the design: Vtn=|Vtp| = (0.7+-1.5) V, K′ n=(100+-10%) μAV ^−2 , K′ p= (50+-10%)μAV^ −2 . Fig. 1 shows the circuit level diagram of 2-stage Miller Compensated OTA.

The transfer function H(s) is given by

$$Vo(s)/ Vd(s) = K (1 – s/z1)/ (1 + s/p1)(1 + s/p2)$$

where, K = (gm1gm2/go1go2) is the small signal DC gain,
p1 = (go1go2/Ccgm2) is the dominant pole,
p2 = (gm2/CL) is the second pole,
z1 = (gm2/Cc)is the right half plane zero.

As seen earlier , our aim was to split the poles as much as possible to gain atleast 60dB gain bandwidth , so we aim to increase the value of gm2 .

Calculations :

**** All MOSFET's are in saturation**

1) To obtain a phase margin of 60◦ , it is required that the compensating capacitor Cc satisfy this following condition, i.e Cc >= 0.22Cl .

   Given Cl = 5pf

   ∴ Cc = 2pf

2) Slew rate = change in voltage per unit time .

   As the miller capacitance is at output , slew rate = Id5/Cc

   Let slew rate = 20V/μsec .

   ∴ Id5 = 20 * 2 = 40μA .

   ALL THE CALCULATIONS ARE SHOWN IN NEXT PAGE :

$$I_{d3} = \frac{1}{2} I_{d5} \quad \text{[Current Mirror]}$$

$$= \frac{1}{2}(40)$$

$$\boxed{I_{d3} = 20\,\mu A}$$

$$I_{d3} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_3 (V_{SG_3} - |V_{th}|_3)^2$$

$$= \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_3 (V_{S3} - V_{G3} - |V_{th}|_3)^2$$

$$V_{S3} = V_{DD}, \quad V_{G3} = V_{D3} = V_{D1}$$

$$= \frac{1}{2}$$

$$\left(\frac{W}{L}\right)_3 = \frac{2 I_{d3}}{\mu_p C_{ox} (V_{DD} - |V_{th3}|_{max} - V_{in(max)} + |V_{th1}|_{min})}$$

$$= \frac{2 \times 20}{60 (2.5 - 1.6 - 0.85 + 0.55)^2}$$

$$= 1.85$$

$$\boxed{\left(\frac{W}{L}\right)_3 \approx 2}$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 2.$$

$$g_{m_1} = GBW \times 2\pi \times C_c$$

$$= 50 \times 10^6 \times 2\pi \times 2 \times 10^{-12}$$

$$= 628.31\ \mu A/V$$

$$\left(\frac{W}{L}\right)_1 = \frac{g_{m_1}^2}{\mu_n C_{ox} I_{D5}} = \frac{(628.31)^2}{110 \times 40} = 89.72 \approx 90$$

$$\boxed{\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 90}$$

$$\left(\frac{W}{L}\right)_5 = \frac{2 I_{D5}}{\mu_n C_{ox} (V_{DS} sat)^2}$$

$$V_{DS5}\,sat = V_{in}(min) - V_{SS} - \sqrt{\frac{I_{D5}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} - V_{th,1}(max)$$

$$= 0.7 - (-2.5) - \sqrt{\frac{40}{110 \times 90}} - 0.85$$

$$= 2.35 - 0.0635$$

$$V_{DS}sat_5 = 2.28\ V$$

$$\left(\frac{W}{L}\right)_5 = \frac{2 \times 40}{110 \times (2.28)^2} = 0.14$$

$$\boxed{\left(\frac{W}{L}\right)_5 = 0.14}$$

$g_{m6} \geq 10 g_{m1}$ (for 60° Phase Margin)

$\geq 10 \times 628.31$

$$\boxed{g_{m6} \geq 6283.1\ \frac{\mu A}{V}}$$

$$g_{m4} = \sqrt{2 I_{D4} \mu_p C_{ox} \left(\frac{W}{L}\right)_4}$$

$$= \sqrt{2 \times 20 \times 60 \times 2}$$

$$\boxed{g_{m4} = 69.28\ \frac{\mu A}{V}}$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 \frac{g_{m6}}{g_{m4}}$$

$$= 2 \times \frac{6283.1}{69.28} = 181$$

$$\left(\frac{W}{L}\right)_6 = 181$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_{D7}}{I_{D5}} \times \left(\frac{W}{L}\right)_5$$

$$I_{D7} = I_{D6} = \frac{g_{m6}^2}{2\,\mu_p C_{ox}\left(\frac{W}{L}\right)_6}$$

$$= \frac{(6283.1)^2}{2 \times 60 \times 181}$$

$$I_{D7} = 1817.55\,\mu A$$

$$\left(\frac{W}{L}\right)_7 = \frac{1817.55}{40} \times 0.14$$

$$= 6.36$$

$$\left(\frac{W}{L}\right)_7 \approx 7$$

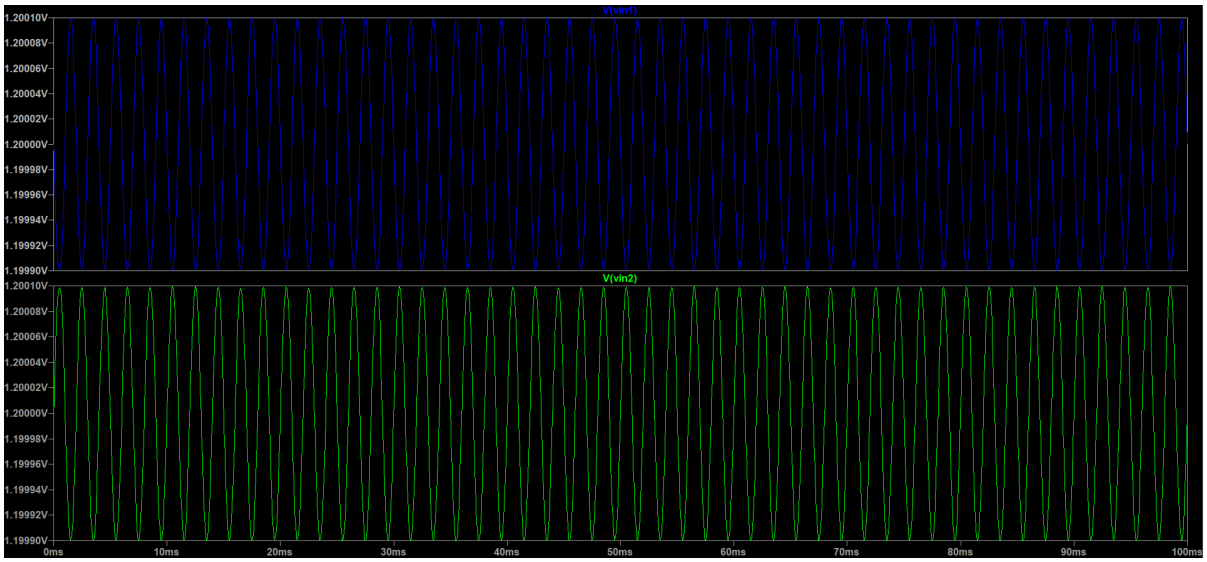
As the mosfet 5 and 8 are circuit mirrors , their W/L ratio is kept the same .

Mosfet	W/L	L(in μm)	W(in μm)
M1	90	1	45
M2	90	1	45
M3	2	0.5	1
M4	2	0.5	1
M5	0.14	0.5	0.07
M6	181	1	181
M7	7	1	7
M8	0.14	0.5	0.07

Optimisation :

1) Gain Bandwidth can be increased by decreasing the value of Cc as shown in the above formula .
2) A higher lambda(channel length modulation parameter) value indicates a more pronounced channel length modulation effect, meaning the effective channel length decreases more rapidly with increasing drain-source voltage. Conversely, a lower lambda value implies less channel length modulation and thus a more stable effective channel length with changing Vds. So, we have increased the length of 6 and 7 from 500 nm to 1μm . (Keeping W/L same) .
3) The gain is optimised by changing the value of W/L for M6 mosfet as this mosfet is directly involved in the second stage amplification .This value is decreased till we get a gain more than 60dB.
4) The gain can be optimised by increasing the value of W/L for 1 and 2 so that we get a higher differential gain at the first stage itself .

Simulation Result :

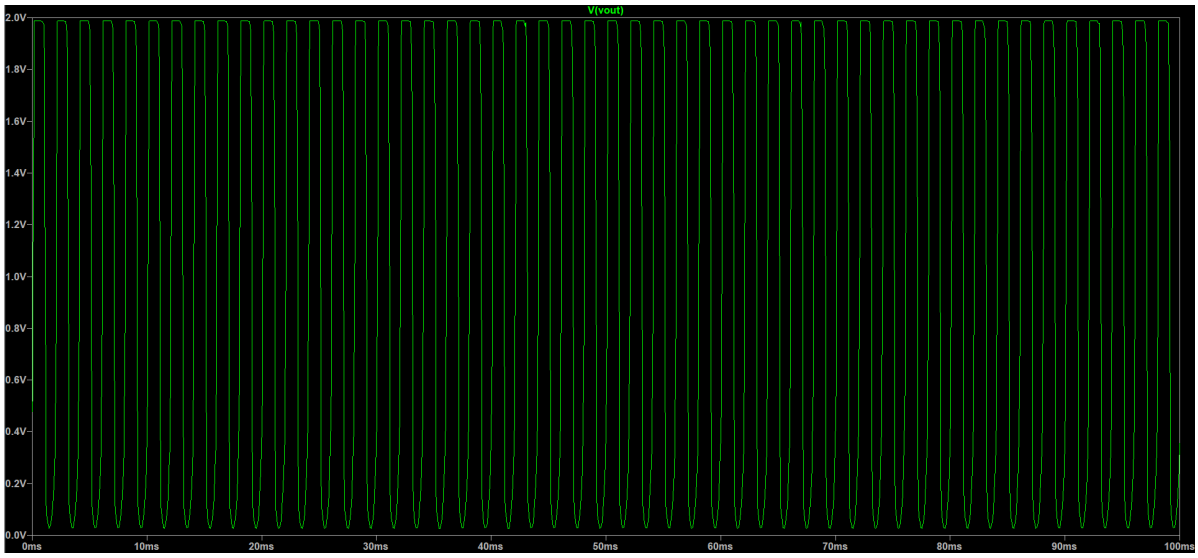


Input waveform as Vin1 and Vin2

Gain vs frequency and phase vs frequency curve(AC analysis)

Optimised :

Gain vs frequency and phase vs frequency curve(AC analysis)



Vout vs Time (Transient analysis)

Conclusion:

In conclusion, the two-stage differential amplifier utilising MOSFETs with Miller compensation has been successfully designed, analysed, and implemented. But we are

getting an approximate gain of 100dB instead of 66.6dB . The circuit can be further optimised to achieve the different required conditions.

-:THANK YOU:-

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