Incorrect Encoding by the Assembler

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1 Introduction

In this document we have given a comparison between the expected and actual encoding produced by the assembler. Only those instructions for which the encoding did not match are mentioned.

2 Observation

The set of instruction and their observations are given below-

- Shift- SLLD, SRLD, SRAD

  The error lies in the i[13] and i[6] bits of encoding.

  - The i[6] bit is always 0, correct being always 1.
  - The i[13] bit signifies whether the instruction has immediate or register input.
    - For immediate input, i[13] should be 1, but is 0 in actual encoding.
    - For register input, i[13] should be 0, but is 1 in actual encoding.

- Vector - SIMDI (VADDD, VSUBD, VUMULD, VSMULD)

  The error lies in the [9:7] bits of the encoding. The error is same for a specified data-type (8,16,32), regardless of the operation (add, sub, umul, smul).

  - For 8 bit- The second and third bytes are always 24, correct being 0c.
  - For 16 bit- The third byte is always 4, correct being 1.
  - For 32 bit- The third byte is always 0, correct being 2.

- Vector Floating Point

3 Shift Instructions

3.1 SLLD

Bits	31-30	29-25	24-19	18-14	13	12-7	6-5	4-0
Fields	10	rd	op3	rs1	i=0	unused(zero)	10	rs2
Expected	10	10010	100101	00010	0	000000	10	00100
Actual	10	10010	100101	00010	1	000001	00	00100

Table 1: SLLD(Instruction - slld g2, g4, l2(shift count reg rs2))

Bits	31-30	29-25	24-19	18-14	13	12-7	6-5	4-0
Fields	10	rd	op3	rs1	i=0	unused(zero)	10	imm
Expected	10	10010	100101	00010	1	000000	10	00010
Actual	10	10010	100101	00010	0	000001	00	00010

Table 2: SLLD(Instruction - srld g2, 2, l2)

3.2 SRLD

Bits	31-30	29-25	24-19	18-14	13	12-7	6-5	4-0
Fields	10	rd	op3	rs1	i=0	unused(zero)	10	rs2
Expected	10	00110	100110	00010	0	000000	10	00100
Actual	10	00110	100110	00010	1	000001	00	00100

Table 3: SRLD(Instruction - srld g2, g4, g6)

Bits	31-30	29-25	24-19	18-14	13	12-7	6-5	4-0
Fields	10	rd	op3	rs1	i=0	unused(zero)	10	imm
Expected	10	00110	100110	00010	1	000000	10	00010
Actual	10	00110	100110	00010	0	000001	00	00010

Table 4: SRLD(Instruction - srld g2, 2, g6)

3.3 SRAD

Bits	31-30	29-25	24-19	18-14	13	12-7	6-5	4-0
Fields	10	rd	op3	rs1	i=0	unused(zero)	10	rs2
Expected	10	10000	100111	00010	0	000000	10	00100
Actual	10	10000	100111	00010	1	000001	00	00100

Table 5: SRAD(Instruction - slld g2, g4, l0)

Bits	31-30	29-25	24-19	18-14	13	12-7	6-5	4-0
Fields	10	rd	op3	rs1	i=0	unused(zero)	10	imm
Expected	10	10000	100111	00010	1	000000	10	00010
Actual	10	10000	100111	00010	0	000001	00	00010

Table 6: SRAD(Instruction - slld g2, 2 , l0)

4 SIMD Instructions I

4.1 VADDD8, VADDD16, VADDD32

VADDD8

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	000000	00010	0	000	00110	00100
Actual	10	00110	000000	00010	0	000	10010	00100

Table 7: vaddd8 g2, g4, g6

VADDD16

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	000000	00010	0	000	01010	00100
Actual	10	00110	000000	00010	0	001	00010	00100

Table 8: vaddd16 g2, g4, g6

VADDD32

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	000000	00010	0	000	10010	00100
Actual	10	00110	000000	00010	0	000	00010	00100

Table 9: vaddd32 g2, g4, g6

4.2 VSUBD8, VSUBD16, VSUBD32

VSUBD8

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	000100	00010	0	000	00110	00100
Actual	10	00110	000100	00010	0	000	10010	00100

Table 10: vsubd8 g2, g4, g6

VSUBD16

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	000100	00010	0	000	01010	00100
Actual	10	00110	000100	00010	0	001	00010	00100

Table 11: vsubd16 g2, g4, g6

VSUBD32

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	00010	00010	0	000	10010	00100
Actual	10	00110	000100	00010	0	000	00010	00100

Table 12: vsubd32 g2, g4, g6

4.3 VUMULD8, VUMULD16, VUMULD32

VUMULD8

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	001010	00010	0	000	00110	00100
Actual	10	00110	001010	00010	0	000	10010	00100

Table 13: vumuld8 g2, g4, g6

VUMULD16

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	001010	00010	0	000	01010	00100
Actual	10	00110	001010	00010	0	001	00010	00100

Table 14: vumuld16 g2, g4, g6

VUMULD32

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	001010	00010	0	000	10010	00100
Actual	10	00110	001010	00010	0	000	00010	00100

Table 15: vumuld32 g2, g4, g6

4.4 VSMULD8, VSMULD16, VSMULD32

VSMULD8

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	011010	00010	0	000	00110	00100
Actual	10	00110	011010	00010	0	000	10010	00100

Table 16: vsmuld8 g2, g4, g6

VSMULD16

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	011010	00010	0	000	01010	00100
Actual	10	00110	011010	00010	0	001	00010	00100

Table 17: vsmuld16 g2, g4, g6

VSMULD32

Bits	31-30	29-25	24-19	18-14	13	12-10	9-5	4-0
Fields	Intsn	rd	op3	rs1	Instn	Unused	Instn	rs2
Expected	10	00110	011010	00010	0	000	10010	00100
Actual	10	00110	0011010	00010	0	000	00010	00100

Table 18: vsmuld32 g2, g4, g6