Vector Instruction are analyzed her. The inputs are mentiond along with the actual and expected results. Observations are mntioned with them.

Inputs -
rs1- f008c6f8 f008c6f8
rs2-f000d2fa f000d2fa

Instruction	Expected	Actual	Observaton	
VADDD8	e0 08 98 f2	e0 09 00 f2	Carry is being added	Intermediate result res8 is defined as 64 bit
VADDD16	e008 99f2 x1 = f008 ; y1 = f000	0008 01f2 x1 = 08 ; y1 =00	Carry is being added Only ower 8 bits are taken as input	Intermediate result res16 is defined as 64 bit Inputs are defined as 8 bits
VADDD32	E00999f2 x1 = f008c6f8 ; y1 = f000d2fa	01f2 x1 = f8 ; y1 = fa	Carry is being added Only lowest 8 bits are being taken as input resu	Intermediate result res32 is defined as 64 bit Inputs are defined as 8 bits