Gavin Vasandani

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Education

Imperial College London, Master of Engineering, Computer Engineering **Oct 2021 - Jun 2025**

- Combined degree in Department of Electrical Engineering and Department of Computing.
- Achieved First-Class Honours (equivalent to 4.0 GPA) in 1st, 2nd and 3rd year.
- Relevant Modules: Digital System Design, Instruction Arch. and Compilers, System Performance Engineering

Professional & Research Experience

Arctic Lake Technology, *Software and Hardware Engineering Intern* **April 2024 – Sept 2024**

- Intern in the FPGA team, integrating Arctic Lake's custom, high-performance trading system (ALX) with ultra-low latency pre-trade risk checking using FPGAs.
- *Project 1*: Developed a 32-bit Ethernet (ETH) module for TCP packet parsing, maximizing logic execution in each cycle to optimize latency. (Verilog, Vivado, Alveo U50)
- *Project 2*: Built a module to verify order messages against ESMA requirements, handling writing of ESMA parameters via a custom PCIe module.
- *Project 3*: Designed FPGA core, integrating all subsidiary modules for packet parsing, rejection logic, ESMA tests, order risk check and packet logging by writing received packets as frames to a logbook via PCIe.
- *Project 4*: Built a Java-based test harness to transmit packets from a NIC to the FPGA, simulating order packets sent by client for pre-trade risk checks. (Java, NIC)
- *Project 5*: Created TCP packet manager to handle unordered, duplicate, and corrupt packets by calculating the expected sequence number and checking invalid checksum bit of the incoming TCP packet. Used Linux TC (traffic control) to test packet corruption, reordering and duplication.
- Created Cocotb testbenches for unit testing of each module, and designed comrpehensive integration tests when building FPGA core and larger subsystems. (Python, Cocotb).
- *Project 6*: Created Jenkins CI/CD pipelines for automates testing, Docker builds, and nightly hardware tests (Jenkins, Docker, Kaniko, Gerrit)

AMD (Advanced Micro Devices) Inc., *Software and Hardware Engineering Intern* **Jun 2023 – Sept 2023**

- Intern in the Platform IP team within AMD's Adaptive and Embedded Computing Group.
- *Project 1*: Created SystemVerilog testbenches to verify CMS Subsystem IP, responsible for monitoring FPGA power management, temperature, and fault detection.
- Verified IP on 3 major simulators (XSim, VSA, Riviera) and committed on Vivado 2023.2.
- *Project 2:* Developed 16-bit low-latency CRC, an error-detecting program, in C to implement on CMS Subsystem.
- *Project 3:* Developed and deployed a script to generate randomized hardware configuration files from a YAML parameter file for the CMS Subsystem, accelerating time to reach complete functional coverage.

Jane Street IN FOCUS, *Software Engineering Track* **Apr 2022 – May 2022**

- *Project 1:* Learned functional programming using OCaml and developed backend for a snake game.
- *Project 2:* Created a trading bot in C++ that exploits discrepancies in the price of an ADR pair. Determined ADR's fair value through moving average. Achieved 3rd in Jane Street's Electronic Trading Competition.

Institute of Photonic Sciences, Quantum Computing and Engineering, *Student Research Intern* **Jun 2019 – Aug 2019**

- Selected as a student researcher from the Middle East for the Barcelona International Youth Science Competition.
- *Project 1:* Conducted experiment to validate the BB84 quantum key distribution protocol.

NASA Wallops Flight Center, Satellite Projects, *Student Research Intern* **Jun 2018 – Sept 2018**

- Synthesized a nitrogen-doped double-walled carbon nanotube epoxy resin for radiation shielding in manned spaceflight.
- Project selected by NASA and launched on RB-4 research satellite from NASA Wallops Flight Center, Virginia.

Projects

C90 to RISCV Assembly Compiler (C, Assembly)

- Developed C90 to RISCV compiler with support for arrays, recursion, and floating-point arithmetic.
- Improved memory allocation with static memory analysis and added a stack simulator for RISC-V memory emulation.

C++ Trading Platform (C++, Asio, Bash)

- Developed a multi-client, server trading platform using Asio Networking Library with custom memory management.
- Created and hosted price-time priority orderbook with pro-rata matching.
- Simulated market liquidity by creating market maker bots to provide buy and sell orders.

RISC-V Processor (SystemVerilog, C++)

- Designed a RISC-V processor with its complete instruction set architecture with 5-stage pipelining and 2-way associative cache with LRU replacement.
- Created extensive testbench in C++ and tested on IP using Verilator

Programming Languages

Advanced in C/C++, Verilog, SystemVerilog, Java, Python, Bash. **Intermediate in** OCaml, SQL, MATLAB, Swift
Tools: GDB, Valgrind, Cppcheck, Viper, Verilator, Cocotb, Vivado, Quartus, GTKWave, ModelSim, TC (Traffic Control)
Technologies: Linux, Git, Docker, Perforce, JIRA, Confluence, Swarm, AWS, Jenkins, Kaniko