NVDC Battery Buck-Boost Charge Controller with System Power Monitor and Processor Hot Monitor

1 Features

- **Charge from wide range of input sources**
  - **3.5V-24V input operating voltage**
  - **Supports USB2.0, USB 3.0, USB 3.1 (Type C), and USB_PD input current settings**
  - **Seamless transition between buck and boost operation**
  - **Input current and voltage regulation against source over-load**
- **Battery configuration: 1-4 cell**
- **Power/current monitor for CPU throttling**
  - **Comprehensive /PROCHOT profile**
  - **Input and battery current monitor**
  - **System power monitor**
- **Narrow-VDC(NVDC) power path management**
  - **Instant-on with no battery or deeply discharged battery**
  - **Battery supplements system when adapter is fully-loaded**
  - **Ideal diode operation in supplement mode**
- **Power up USB port from battery (USB OTG)**
  - **Output 3.8V-20V compatible with USB PD**
- **High switching frequency for 1uH-2.2uH low profile inductor**
- **Host Control Interface for flexible system configuration**
  - **SMBus/I2C port for optimal system performance and status reporting**
  - **Hardware pin to set input current limit without EC control**
- **High accuracy regulation and monitor**
  - **+/-0.5% charge voltage regulation**
  - **+/-2% input/charge current regulation**
  - **+/-2% input/charge current monitor**
  - **+/-5% power monitor**
- **Safety**
  - **Thermal shutdown**
  - **Input/system/battery over-voltage protection**
  - **MOSFET/inductor over-current protection**
- **Low battery quiescent current**
- **Package: 4x4 QFN**

2 Applications

- Ultra-book, notebook, detachable and tablet PC
- Industrial and Medical Equipment
- Portable Equipment with rechargeable battery

3 Description

The bq25700 is synchronous NVDC-1 battery buck-boost charge controller, offering low component count, high efficiency solution for space-constraint, multi-chemistry battery charging applications.

The NVDC-1 configuration allows the system to be regulated at battery voltage, but not drop below system minimum voltage. The system keeps operating even when the battery is completely discharged or removed. When load power exceeds input source rating, battery gets into supplement mode and prevents the input source from being overloaded.

The bq25700 charges battery from a wide range of input sources including USB adapter to high voltage USB PD sources and traditional adapters. During power up, the charger sets converter to buck, boost or buck-boost configuration based on input source and battery conditions. During the charging cycle, the charger automatically transits among buck, boost and buck-boost configuration without host control.

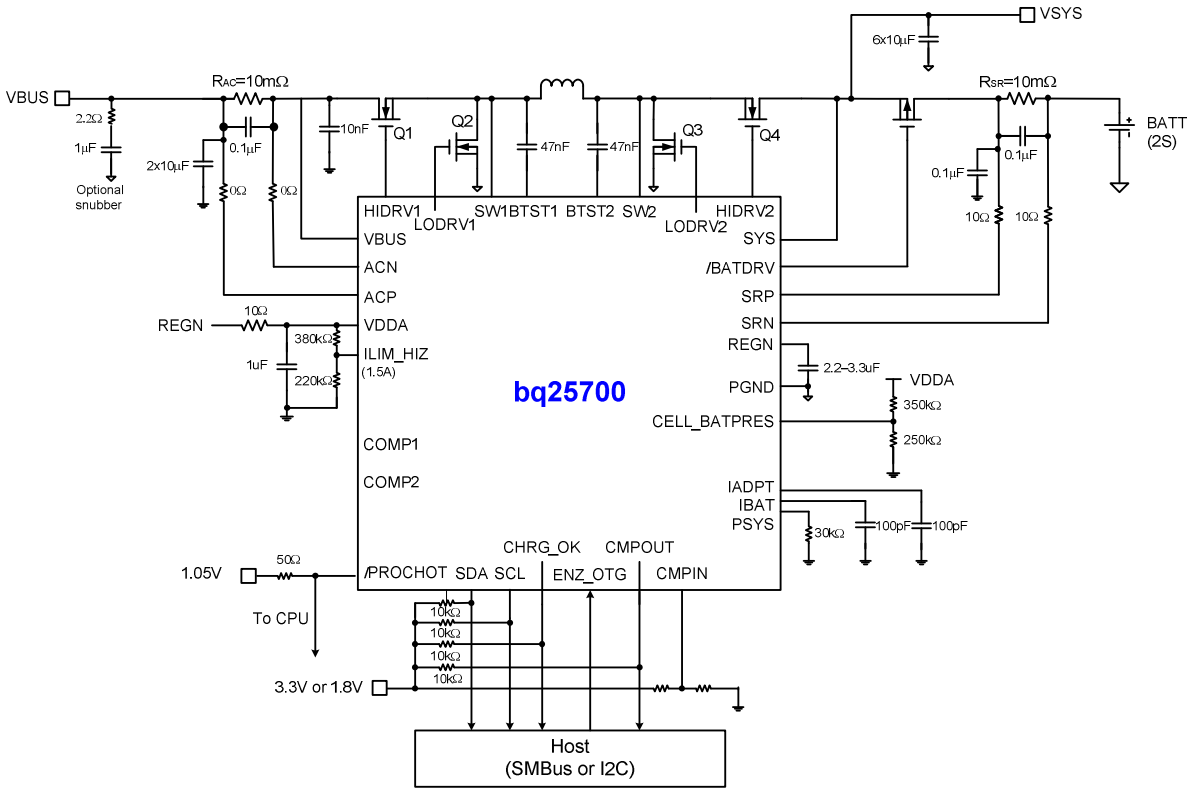
The bq25700 supports On-the-Go (OTG) function from 1-4 cell battery to generate 3.8V to 20V on VBUS.

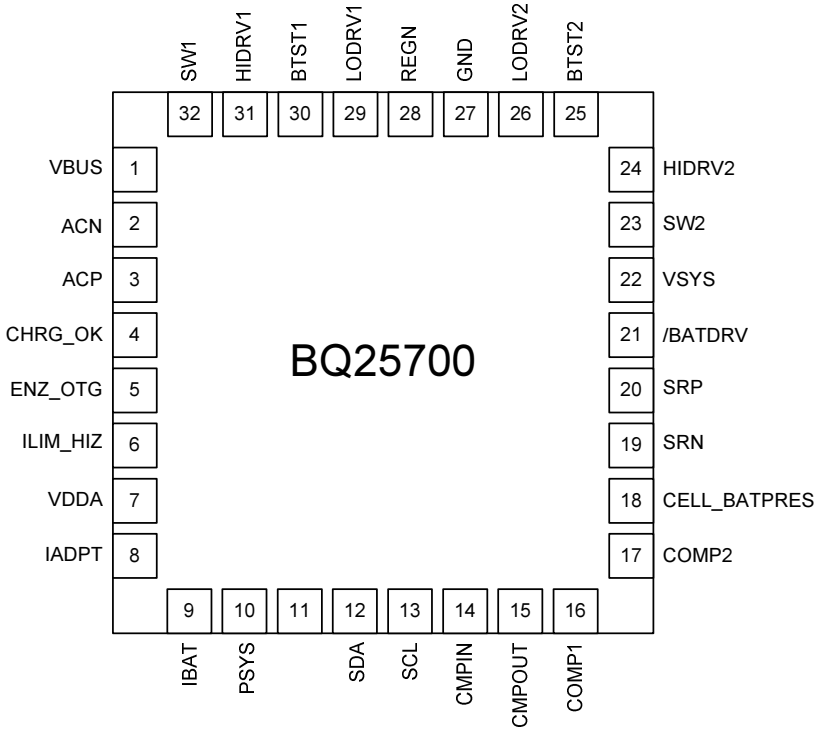
The bq25700 monitors adapter current, battery current and system power. The flexibly programmed /PROCHOT output goes directly to CPU for throttle back when needed.

4 Order Information

PART NUMBER	IC MARKING	ORDERING NUMBER	QUANTITY
bq25700	BQ25700	bq25700RSNR	3000
		bq25700RSNT	250

5 Application Diagram





PRODUCT PREVIEW

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6 Terminal Configuration and Functions

TERMINAL NAME	TYPE(1)	DESCRIPTION
VBUS	P	Charger input voltage. From USB port, the total input capacitance is no more than 10uF to PGND.
ACN	P	Input current sense resistor negative input. The leakage on ACP and ACN are matched. The series resistors on ACP/ACN is placed between filter cap and IC pins.
ACP	P	Input current sense resistor positive input. The leakage on ACP and ACN are matched. The series resistors on ACP/ACN is placed between filter cap and IC pins.
CHRG_OK	O	Open drain active high indicator to inform the system power source can be connected to the charger input. Connect to the pull up rail via 10kohm resistor.
ENZ_OTG	I	Active LOW to enable OTG mode. When ENZ_OTG pin is LOW and REG0x32[13] is HIGH, OTG is enabled, and VBUS is regulated at 5V (REG0x3B()). When the pin is not in use, hold the pin to ground.
ILIM_HIZ	I	Input current limit input. Program ILIM voltage by connecting a resistor divider from supply rail to ILIM pin to ground. The pin voltage is calculated as: V(ILIM) = 1V + 40 × IDPM × R_{AC}, in which IDPM is the target regulation current. When the pin voltage is below 1V, the device enters HIZ mode with lowest quiescent current. When the pin voltage is above 1V, the device is out of HIZ mode.
VDDA	P	Output from REGN 6V linear regulator output supplied from VBUS or SYS. The LDO is active when VBUS above UVLO. Connect a 10ohm resistor from REGN to VDDA and a 1μF ceramic capacitor from VDDA to power ground.
IADPT	O	Buffered adapter current output. $V_{(IADP)}$ = 40 or 80 × ($V_{(ACP)}$ – $V_{(ACN)}$). The ratio of 40x and 80x is selectable with SMBus. Place a resistor from IADPT pin to ground corresponding to inductor in use. For 2.2uH, the resistor is 113kOhm. Place 100pF or less ceramic decoupling capacitor from IADPT pin to ground. This pin can be floating if it is not in use. IADPT output voltage is clamped below 3.3 V.
IBAT	O	Buffered battery current selected by SMBus. $V_{(IBAT)}$ = 16 × ($V_{(SRP)}$ – $V_{(SRN)}$) for charge current, or $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRN)}$ – $V_{(SRP)}$) for discharge current, with ratio selectable through SMBus. Place 100pF or less ceramic decoupling capacitor from IBAT pin to ground. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V.
PSYS	O	Current mode system power monitor. The output current is proportional to the total power from the adapter and battery. The gain is selectable through SMBus. Place resistor from PSYS to ground to generate output voltage. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V. Place a cap in parallel with resistor for filtering.
/PROCHOT	O	Active low open drain output of “processor hot” indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the PROCHOT profile is triggered, a minimum 10-ms pulse is asserted.
SDA	I/O	SMBus/I2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10-kΩ pull-up resistor according to SMBus specifications.
SCL	I	SMBus/I2C clock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pull-up resistor according to SMBus specifications.
CMPIN	I	Input of independent comparator. Internal reference, output polarity and deglitch time is selectable by SMBus. With polarity HIGH (REG0x30[6]=1), place a resistor between CMPIN and CMPOUT to program hysteresis. With polarity LOW (REG0x30[6]=0), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN to ground.

CMPOUT	O	Open-drain output of independent comparator. Place 10kΩ pull-up resistor from CMPOUT to pull-up supply rail. Internal reference, output polarity and deglitch time are selectable by SMBus.
COMP1	I	Buck boost converter compensation pin 1.
COMP2	I	Buck boost converter compensation pin 2.
CELL_BATPRES	I	Battery cell selection pin for 1-4 cell battery setting. CELL pin is biased from REGN. CELL pin also sets SYSOVP threshold to 5V for 1-cell, 12V for 2-cell and 18.5V for 3-cell. When REG0x15() is above 15V, SYSOVP is disabled. CELL pin is pulled below 1V to indicate battery removal, When CELL pin goes below 1V, the battery is removed. The device exits LEARN mode, and disables charge. REG0x15() goes back to default.
SRN	P	Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN pin with a 0.1-μF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-μF ceramic capacitor from SRP to SRN to provide differential mode filtering. The leakage current on SRP and SRN are matched.
SRP	P	Charge current sense resistor positive input. Connect a 0.1-μF ceramic capacitor from SRP to SRN to provide differential mode filtering. The leakage current on SRP and SRN are matched.
/BATDRV	O	P-channel battery FET (BATFET) gate driver output. It is shorted to SYS to turn off the BATFET. It goes 6V below SYS to turn on BATFET. BATFET is in linear mode to regulate SYS at minimum system voltage when battery is depleted. BATFET is fully on during fast charge.
VSYS	P	System power supply. The system voltage regulation limit is programmed in REG0x15() and REG0x3E().
SW2	P	Boost mode high side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
HIDRV2	O	Boost mode high side power MOSFET driver. Connect to high side n-channel MOSFET gate. During buck mode, Q4 is always on.
BTST2	P	Boost mode high side power MOSFET driver power supply. Connect a 0.047-μF capacitor from BOOT2 to SW2. The bootstrap diode between REGN and BOOT2 is integrated.
LODRV2	O	Boost mode low side power MOSFET driver. Connect to low side n-channel MOSFET gate.
PGND	GND	IC power ground.
REGN	P	6V linear regulator output supplied from VBUS or SYS. The LDO is active when VBUS above UVLO. Connect a 2.2 or 3.3μF ceramic capacitor from REGN to power ground. REGN pin output is for power stage gate drive.
LODRV1	O	Buck mode low side power MOSFET driver. Connect to low side n-channel MOSFET gate.
BTST1	P	Buck mode high side power MOSFET driver power supply. Connect a 0.047-μF capacitor from BOOT1 to SW1. The bootstrap diode between REGN and BOOT1 is integrated.
HIDRV1	O	Buck mode high side power MOSFET driver. Connect to high side n-channel MOSFET gate. During boost mode, Q1 is always on.
SW1	P	Buck mode high side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.

7 Device Operating Conditions

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage	SRN, SRP, ACN, ACP, VBUS	-0.3	30	V
	SW1, SW2	-2.0	30	
	BTST1, BTST2, HIDRV1, HIDRV2, /BATDRV	-0.3	36	
	LODRV1, LODRV2 (2% duty cycle)	-4.0	7	
	HIDRV1, HIDRV2 (2% duty cycle)	-4.0	36	
	SW1, SW2 (2% duty cycle)	-4.0	30	
	SDA, SCL, REGN, PSYS, CHRG_OK, CELL_BATPRES, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP1, COMP2, CMPIN, CMPOUT	-0.3	7	
	/PROCHOT	-0.3	5.5	
	IADPT, IBAT, PSYS	-0.3	3.6	
Differential Voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	-0.3	7	V
	SRP-SRN, ACP-ACN	-0.5	0.5	
Temperature	Junction temperature range, T_J	-40	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{STG}	Storage temperature range	-55	155	°C
$V_{(HBM)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2000	V
$V_{(CDM)}$	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	ACN, ACP, VBUS	0	24	V
	SRN, SRP	0	19.2	
	SW1, SW2	-2	24	
	BTST1, BTST2, HIDRV1, HIDRV2, /BATDRV	0	30	
	SDA, SCL, REGN, PSYS, CHRG_OK, CELL, ILIM, LODRV1, LODRV2, VDDA, COMP1, COMP2, CMPIN, CMPOUT	0	6.5	
	/PROCHOT	0	5.3	
	IADPT, IBAT, PSYS	0	3.3	
Differential Voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	0	6.5	V
	SRP-SRN, ACP-ACN	-0.5	0.5	
Temperature	Junction temperature range, T_J	-20	125	°C
	Operating free-air temperature range T_A	-40	85	

8 Electrical Charactristics

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{INPUT_OP}	Input Voltage Operating Range		3.5		26	V
V_{SYSMAX_RNG}	System Voltage Regulation, measured on VSYS		1.024		19.2	V
V_{SYSMAX_ACC}	System Voltage Regulation Accuracy (Charge Disable)	REG0x15() = 0x41A0H (16.800V)		V_{SRN}+150mV		V
			-2		2	%
		REG0x15() = 0x3130H (12.592V)		V_{SRN}+150mV		V
			-2		2	%
		REG0x15() = 0x20D0H (8.400V)		V_{SRN}+150mV		V
			-3		3	%
		REG0x15() = 0x1060H (4.192V)		V_{SRN}+150mV		V
			-3		3	%
V_{SYSMIN_RNG}	System Voltage Regulation, measured on VSYS		1.024		19.2	V
$V_{SYSMIN\_REG\_ACC}$	Minimum System Voltage Regulation Accuracy (Charge Enable, VBAT below REG0x3E() setting)	REG0x3E() = 0x3000H		12.288		V
			-2		2	%
		REG0x3E() = 0x2400H		9.216		V
			-2		2	%
		REG0x3E() = 0x1800H		6.144		V
			-3		3	%
		REG0x3E() = 0x0E00H		3.584		V
			-3		3	%
V_{BAT_RNG}	Battery Voltage Regulation		1.024		19.2	V
$V_{BAT\_REG\_ACC}$	Battery Voltage Regulation Accuracy (Charge Enable) (-20C to 85C)	REG0x15() = 0x41A0H		16.8		V
			-0.5		0.5	%
		REG0x15() = 0x3130H		12.592		V
			-0.5		0.5	%
		REG0x15() = 0x20D0H		8.4		V
			-0.6		0.6	%
		REG0x15() = 0x1060H		4.192		V
			-0.8		0.8	%
$V_{IREG\_CHG\_RNG}$	Charge Current Regulation Differential Voltage Range	$V_{IREG\_CHG} = V_{SRP} - V_{SRN}$	0		81.28	mV
$I_{CHRG\_REG\_ACC}$	Charge Current Regulation Accuracy 10mohm current sensing resistor, VBAT above 0x3E() setting (-20C to 85C)	REG0x14()=0x1000H		4096		mA
			-2		2	%
		REG0x14()=0x0800H		2048		mA
			-3		3	%
		REG0x14()=0x0800H		2048		mA
			-3		3	%
		REG0x14()=0x0400H		1024		mA
			-5		5	%
		REG0x14()=0x0200H		512		mA
			-10		10	%
I_{CLAMP}	Pre-charge Current Clamp	CELL 2s-4s		384		mA
		CELL 1s, V_{SRN}<3V		384		mA
		CELL 1s, V_{SRN}>3V		2		A
$I_{PRECHRG\_REG\_ACC}$	Precharge Current Regulation Accuracy with 10ohm SRP/SRN	REG0x14()=0x0180H		384		mA
			-15		15	%

	series resistor, VBAT below REG0x3E() setting (VIN=20V)	REG0x14()=0x0100H		256		mA
			-20		20	%
		REG0x14()=0x00C0H		192		mA
			-25		25	%
		REG0x14()=0x0080H		128		mA
			-30		30	%
$I_{LEAK\_SRP\_SRN}$	SRP, SRN leakage current mismatch		TBD		TBD	uA
$V_{IREG\_DPM\_RNG}$	Input Current Regulation Differential Voltage Range	$V_{IREG\_DPM} = V_{ACP} – V_{ACN}$	0		63.5	mV
$I_{DPM\_REG\_ACC}$	Input Current Regulation Accuracy with 50mA LSB	IIN_HOST() = 0x5000H	3840		4000	mA
		IIN_HOST() = 0x3C00H	2880		3000	mA
		IIN_HOST() = 0x1E00H	1400		1500	mA
		IIN_HOST() = 0x0A00H	400		500	mA
		IIN_HOST() = 0x0200H	50		100	mA
$I_{LEAK\_ACP\_ACN}$	ACP, ACN leakage current mismatch		TBD		TBD	uA
$V_{IREG\_DPM\_RNG\_ILIM}$	Voltage Range for Input Current Regulation		1		4	V
$I_{DPM\_REG\_ACC\_ILIM}$	Input Current Regulation Accuracy on ILIM pin	ILIM=2.6V	3840		4000	mA
		ILIM=2.2V	2880		3000	mA
		ILIM=1.6V	1400		1500	mA
		ILIM=1.2V	400		500	mA
		ILIM=1.04V	50		100	mA
I_{LEAK_ILIM}	ILIM pin leakage		-1		1	uA
$V_{IREG\_DPM\_RNG}$	Input Voltage Regulation Range	Voltage on VBUS	3.8		20.256	V
$V_{OTG\_REG\_ACC}$	OTG Voltage Regulation Accuracy	REG0x3D()=0x3AC0H		18840		mV
			-2		2	%
		REG0x3D()=0x1B80H		10840		mV
			-2.5		2.5	%
		REG0x3D()=0x0280H		4440		mV
			-3		3	%
$V_{IOTG\_REG\_RNG}$	Input Current Regulation Differential Voltage Range	$V_{IREG\_DPM} = V_{ACP} – V_{ACN}$	0		81.28	mV
I_{OTG_ACC}	Input Current Regulation Accuracy with 50mA LSB	OTGCurrent() = 0x3C00H	2880		3000	mA
		OTGCurrent() = 0x1E00H	1400		1500	mA
		OTGCurrent() = 0x0A00H	400		500	mA
$V_{IREG\_DPM\_RNG}$	Input Voltage Regulation Range	Voltage on VBUS	3.8		20.12	V
$V_{OTG\_REG\_ACC}$	OTG Voltage Regulation Accuracy	REG0x3D()=0x3F80H		20.056		V
			-2		2	%
		REG0x3D()=0x2040H		12.056		V
			-2		2	%
		REG0x3D()=0x04C0H		5.016		V
			-3		3	%
V_{REGN_REG}	REGN Regulator Voltage (0mA - 60mA)	V_{VBUS} = 10V	5.7	6	6.3	V
$V_{DROPOUT}$	REGN voltage in drop out mode	V_{VBUS}=5V, I_{LOAD}=20mA	4.1	4.6	4.7	V
$I_{REGN\_LIM\_Charging}$	REGN Current Limit when converter is enabled	V_{VBUS} = 10V, force V_{REGN} = 4V	50	65		mA
C_{REGN}	REGN Output Capacitor Required for Stability.	I_{LOAD} = 100uA to 50mA	2.2			uF
C_{VDDA}	REGN Output Capacitor Required	I_{LOAD} = 100uA to 50mA	1			uF

	for Stability.					
V_{REGN_REG}	VDDA Regulator Voltage (0mA - 60mA)	V_{VBUS} = 10V	5.7	6	6.3	V
$V_{DROPOUT}$	VDDA voltage in drop out mode	V_{VBUS}=5V, I_{LOAD}=20mA	4.1	4.6	4.7	V
$I_{REGN\_LIM\_Charging}$	VDDA Current Limit when converter is enabled	V_{VBUS} = 10V, force V_{REGN} = 4V	50	65		mA
C_{REGN}	VDDA Output Capacitor Required for Stability.	I_{LOAD} = 100uA to 50mA	2.2			uF
C_{VDDA}	VDDA Output Capacitor Required for Stability.	I_{LOAD} = 100uA to 50mA	1			uF
$I_{BAT\_BATFET\_OFF}$	System powered by battery. BATFET off. $I_{SRN}+I_{SRP}+I_{SW2}+I_{BTST2}+I_{SW1}+I_{BTST1}+I_{ACP}+I_{ACN}+I_{VBUS}+I_{VSYS}$	VBAT<UVLO			5	µA
		VBAT=18V, REG0x30[2]=1		TBD		µA
$I_{BAT\_BATFET\_ON}$	System powered by battery. BATFET on. $I_{SRN}+I_{SRP}+I_{SW2}+I_{BTST2}+I_{SW1}+I_{BTST1}+I_{ACP}+I_{ACN}+I_{VBUS}+I_{VSYS}$	VBAT=18V, REG0x12[15]=1, in low power mode		20		µA
		VBAT=18V, REG0x12[15]=0, REG0x30[14:13]=01, REGN off		TBD		µA
		VBAT=18V, REG0x12[15]=0, REG0x30[14:13]=10, REGN off		TBD		µA
		VBAT=18V, REG0x12[15]=0, REG0x30[12]=1, REGN on.		TBD		µA
$I_{AC\_STANDBY}$	Input standby quiescent current, $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST1}+I_{SW2}+I_{BTST2}$	VIN=20V, VBAT=12.6V, 3s		TBD		µA
		VIN=5V, VBAT=8.4V, 2s		TBD		µA
$I_{AC\_SW\_LIGHT\_buck}$	Input current during PFM in buck mode, 200mW output power $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST}+I_{SW2}+I_{BTST2}$	VIN=20V, VBAT=12.6V, 3s, REG0x12[10]=0; MOSFET Qg=4 nF;		1.5	2	mA
		VIN=20V, VBAT=12.6V, 3s, REG0x12[10]=1 (OOA 40kHz); MOSFET Qg=4 nF;		3	5	mA
$I_{AC\_SW\_buck}$	Input current during PWM in buck mode $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST1}+I_{SW2}+I_{BTST2}$	VIN=20V, VBAT=12.6V, 3s, 800kHz switching frequency, MOSFET Qg=4 nF		8		mA
$I_{AC\_SW\_LIGHT\_boost}$	Input current during PFM in boost mode, 200mW output power $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST2}+I_{SW2}+I_{BTST2}$	VIN=5V, VBAT=8.4V, 2s, REG0x12[10]=0; MOSFET Qg=4 nF;		1.5	2	mA
		VIN=5V, VBAT=8.4V, 2s, REG0x12[10]=1; limit 40kHZ; MOSFET Qg=4 nF;		3	5	mA
$I_{AC\_SW\_boost}$	Input current during PWM in boost mode $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST1}+I_{SW2}+I_{BTST2}$	VIN=5V, VBAT=8.4V, 2s, 800kHz switching frequency, MOSFET Qg=4 nF		8		mA
$I_{AC\_SW\_LIGHT\_buckboost}$	Input current during PFM in buck boost mode, 200mW output power $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST1}+I_{SW2}+I_{BTST2}$	VIN=12V, VBAT=12V, REG0x12[10]=0; MOSFET Qg=4 nF;		1.5	2	mA
		VIN=12V, VBAT=12V, REG0x12[10]=1; limit 40kHZ; MOSFET Qg=4 nF;		3	5	mA
$I_{AC\_SW\_buckboost}$	Input current during PWM in buck boost mode, $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST2}+I_{SW2}+I_{BTST2}$	VIN=12V, VBAT=12V, 800kHz switching frequency, MOSFET Qg=4 nF		8		mA
$I_{OTG\_STANDBY}$	Standby current in OTG mode $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST2}+I_{SW2}+I_{BTST2}$	VBAT=8.4V, VBUS=5V		TBD		mA
		VBAT=8.4V, VBUS=12V		TBD		mA
		VBAT=8.4V, VBUS=20V		TBD		mA

$I_{OTG\_STANDBY}$	Quiescent current during PFM in OTG mode $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST2}+I_{SW2}+I_{BTST2}$	VBAT=8.4V, VBUS=5V, 800kHz switching frequency, MOSFET Qg=4 nF		TBD		mA
		VBAT=8.4V, VBUS=12V, 800kHz switching frequency, MOSFET Qg=4 nF		TBD		mA
		VBAT=8.4V, VBUS=20V, 800kHz switching frequency, MOSFET Qg=4 nF		TBD		mA
I_{OTG_SW}	Quiescent current during PWM in OTG mode $I_{VBUS}+I_{ACP}+I_{ACN}+I_{VSYS}+I_{SRP}+I_{SRN}+I_{SW1}+I_{BTST2}+I_{SW2}+I_{BTST2}$	VBAT=8.4V, VBUS=5V, 800kHz switching frequency, MOSFET Qg=4 nF		TBD		mA
		VBAT=8.4V, VBUS=12V, 800kHz switching frequency, MOSFET Qg=4 nF		TBD		mA
		VBAT=8.4V, VBUS=20V, 800kHz switching frequency, MOSFET Qg=4 nF		TBD		mA
V_{ACP/N_OP}	Input Common Mode Range	Voltage on ACP/ACN	3.8		26	V
V_{IADP_CLAMP}	IADP Output Clamp Voltage		3.1	3.2	3.3	V
I_{IADP}	IADP Output Current				1	mA
A_{IADP}	Input Current Sensing Gain	$V_{(IADP)}/V_{(ACP-ACN)}$, REG0x12[4]=0		40		V/V
		$V_{(IADP)}/V_{(ACP-ACN)}$, REG0x12[4]=1		80		V/V
V_{IADP_ACC}	Input Current Monitor Accuracy	$V_{(ACP-ACN)}$ = 40.96mV	-2		2	%
		$V_{(ACP-ACN)}$ = 20.48mV	-3		3	%
		$V_{(ACP-ACN)}$ =10.24mV	-6		6	%
		$V_{(ACP-ACN)}$ = 5.12mV	-10		10	%
C_{IADP_MAX}	Maximum Output Load Capacitance				100	pF
V_{SRP/N_OP}	Battery Common Mode Range	Voltage on SRP/SRN	2.5		18	V
V_{IBAT_CLAMP}	IBAT Output Clamp Voltage		3.1	3.2	3.3	V
I_{IBAT}	IBAT Output Current				1	mA
A_{IBAT_DCHG}	Discharge Current Sensing Gain on IBAT pin	$V_{(IBAT)}/V_{(SRN-SRP)}$, REG0x12[3]=0,		8		V/V
		$V_{(IBAT)}/V_{(SRN-SRP)}$, REG0x12[3]=1,		16		V/V
$I_{IBAT\_DCHG\_ACC}$	Discharge Current Monitor Accuracy on IBAT pin	$V_{(SRN-SRP)}$ = 40.96mV	-2		2	%
		$V_{(SRN-SRP)}$ = 20.48mV	-3		3	%
		$V_{(SRN-SRP)}$ =10.24mV	-5		5	%
		$V_{(SRN-SRP)}$ = 5.12mV	-10		10	%
A_{IBAT_CHG}	Charge Current Sensing Gain on IBAT pin	$V_{(IBAT)}/V_{(SRP-SRN)}$		20		V/V
$I_{IBAT\_CHG\_ACC}$	Charge Current Monitor Accuracy on IBAT pin (0-85C)	$V_{(SRP-SRN)}$ = 40.96mV	-2		2	%
		$V_{(SRP-SRN)}$ = 20.48mV	-3		3	%
		$V_{(SRP-SRN)}$ =10.24mV	-5		-5	%
		$V_{(SRP-SRN)}$ = 5.12mV	-10		10	%
C_{IBAT_MAX}	Maximum Output Load Capacitance				100	pF
V_{PMON}	PMON Output Voltage Range		0		3.3	V
I_{PMON}	PMON Output Current		0		160	uA
A_{PMON}	PMON System Gain	$V_{(PMON)}/(P(IN)+P(BAT))$, REG0x30[9]=1		1		uA/W

V_{PMON_ACC}	PMON Gain Accuracy (REG0x3B[9]=1)	Adapter Only with System Power = 19.5V/45W	-5		5	%
		Battery Only with System Power 11V/44W	-5		5	%
V_{PMON_CLAMP}	PMON Clamp Voltage		3		3.3	V
V_{VBUS_UVLOZ}	VBUS Under-Voltage Rising Threshold	VBUS Rising		3.5		V
V_{VBUS_UVLO}	VBUS Under-Voltage Falling Threshold	VBUS Falling		3.2		V
$V_{VBUS\_UVLO\_HYST}$	VBUS Under-voltage hystersis			300		mV
V_{VBUS_CONVEN}	VBUS Converter Eanble Rising Threshold	VBUS Rising	3.8			V
$V_{VBUS\_CONVENZ}$	VBUS Converter Enable Falling Threshold	VBUS Falling			3.5	V
$V_{VBUS\_CONVEN\_HYST}$	VBUS Converter Enable Hysteresis			200		mV
V_{VBAT_UVLOZ}	VBAT Under-Voltage Rising Threshold	VSRN Rising			2.7	V
V_{VBAT_UVLO}	VBAT Under-Voltage Falling Threshold	VSRN Falling		2.4		V
$V_{VBAT\_UVLO\_HYST}$	VBAT Under-Voltage Hysteresis			200		mV
V_{VBAT_OTGEN}	VBAT OTG Enable Rising Threshold	VSRN Rising			2.7	V
V_{VBAT_OTGENZ}	VBAT OTG Enable Falling Threshold	VSRN Falling		2.4		V/cell
$V_{VBAT\_OTGEN\_HYST}$	VBAT OTG Enable Hysteresis			200		mV
$V_{VBUS\_OTG\_UV}$	VBUS Under-Voltage Falling Threshold	REG0x3B()=5V		4.0		V
		REG0x3B()=12V		9.6		V
		REG0x3B()=20V		16.0		V
$V_{VBUS\_OTG\_UV}$	VBUS Under-Voltage Rising Threshold	REG0x3B()=5V		TBD		V
		REG0x3B()=12V		TBD		V
		REG0x3B()=20V		TBD		V
$V_{VBUS\_OTG\_UV\_HYST}$	VBUS Under-Voltage Hysteresis			TBD		mV
$V_{VBUS\_OTG\_OV}$	VBUS Over-Voltage Rising Threshold	REG0x3B()=5V		5.5		V
		REG0x3B()=12V		13.0		V
		REG0x3B()=20V		21.5		V
$V_{VBUS\_OTG\_OV}$	VBUS Over-Voltage Falling Threshold	REG0x3B()=5V		TBD		V
		REG0x3B()=12V		TBD		V
		REG0x3B()=20V		TBD		V
$V_{VBUS\_OTG\_OV\_HYST}$	VBUS Over-Voltage Hysteresis			TBD		mV
$V_{USB\_QUAL\_RISE}$	USB Qualification Rising Threshold	VBUS Rising		6.5		V
$V_{USB\_QUAL\_FALL}$	USB Qualification Falling Threshold	VBUS Falling		6.2		V
$V_{USB\_QUAL\_HYST}$	USB Qualification Hysteresis			300		mV
$V_{BAT\_SYSMIN\_RISE}$	LDO mode to fast charge mode threshold, VSRN rising	as percentage of 0x3E()	94	96	99	%
$V_{BAT\_SYSMIN\_FALL}$	LDO mode to fast charge mode threshold, VSRN falling	as percentage of 0x3E()		92		%
$V_{BAT\_SYSMIN\_HYST}$	Fast charge mode to LDO mode threshold hysteresis	as percentage of 0x3E()		4		%
V_{BATLV_FALL}	BATLOWV falling Threshold	1s		2.90		V
		2-4s		5.80		V
V_{BATLV_RISE}	BATLOWV rising Threshold	1s		3.00		V
		2-4s		6.00		V
V_{BATLV_RHYST}	BATLOWV hysteresis	1s		100		mV
		2-4s		200		mV
V_{ACOV_RISE}	VBUS Over-Voltage Rising	VBUS Rising	25	26	28	V

	Threshold					
V_{ACOV_FALL}	VBUS Over-Voltage falling Threshold	VBUS Falling		25		V
V_{ACOV_HYST}	VBUS Over-Voltage Hysteresis			1		V
$t_{ACOV\_RISE\_DEG}$	VBUS Over-Voltage Rising Deglitch	VBUS Rising to stop converter		100		us
$t_{ACOV\_FALL\_DEG}$	VBUS Over-Voltage Falling Deglitch	VBUS Falling to start converter		3		ms
V_{ACOC}	ACP to ACN Rising Threshold, w.r.t. ILIM2 in REG0x33[15:11]	Voltage across input sense resistor rising, Reg0x33[8]=1		200		%
V_{ACOC_FLOOR}	Measure between ACP and ACN	Set IDPM to min	44	50	55	mV
$V_{ACOC\_CEILING}$	Measure between ACP and ACN	SET IDPM to max	174	180	185	mV
$t_{ACOC\_DEG\_RISE}$	Rising Deglitch Time	Deglitch time to trigger ACOC		100		us
t_{ACOC_RELAX}	Relax Time	Relax time before converter starts again		100		ms
V_{SYSOVP_RISE}	System Over-Voltage Rising Threshold to turn off converter	1s	4.9	5.0	5.1	V
		2s	11.8	12.0	12.2	V
		3s	18.0	18.5	19.0	V
V_{SYSOVP_FALL}	System Over-Voltage Falling Threshold	1s		4.8		V
		2s		11.5		V
		3s		17.5		V
V_{SYSOVP_HYST}	System Over-Voltage Hysteresis	1s		200		mV
		2s		500		mV
		3s		1000		mV
I_{SYSOVP}	Discharge Current when SYSOVP stop switching was triggered	on SRP and SRN		20		mA
V_{BATOVP_RISE}	Over-Voltage Rising Threshold as percentage of V_{BAT_REG} in REG0x15()	1s, 4.2V	103	104	105	%
		2s, 8.4V	101	102	103	%
		3s, 12.6V	101	102	103	%
		4s, 16.8V	101	102	103	%
V_{BATOVP_FALL}	Over-Voltage Falling Threshold as percentage of V_{BAT_REG} in REG0x15()	1s	101	102	103	%
		2s, 8.4V	100	101	102	%
		3s, 12.6V	100	101	102	%
		4s, 16.8V	100	101	102	%
V_{BATOVP_HYST}	Over-Voltage Hysteresis as percentage of V_{BAT_REG} in REG0x15()	1s		2		%
		2s, 8.4V		1		%
		3s, 12.6V		1		%
		4s, 16.8V		1		%
I_{BATOVP}	Discharge Current during BATOVP	on SRP and SRN		20		mA
t_{BATOVP_RISE}	Over-Voltage Rising Deglitch to turn off BATDRV to disable charge			20		ms
T_{SHUT_RISE}	Thermal Shutdown Rising Temperature	Temperature Increasing		155		°C
T_{SHUTF_FALL}	Thermal Shutdown Falling Temperature	Temperature Reducing		135		°C
T_{SHUT_HYS}	Thermal Shutdown Hysteresis			20		°C
t_{SHUT_RDEG}	Thermal Shutdown Rising Deglitch			100		us
t_{SHUT_FHYS}	Thermal Shutdown Falling Deglitch			10		ms
$V_{SYS\_PROCHOT}$	Vsys threshold falling threshold	Reg0x33[7:6]=00, 1s		2.775		V
		Reg0x33[7:6]=00, 2-4s		5.75		V
		Reg0x33[7:6]=01, 1s	2.95	3.00	3.05	V
		Reg0x33[7:6]=01, 2-4s	5.90	6.00	6.10	V
		Reg0x33[7:6]=10, 1s		3.125		V

		Reg0x33[7:6]=10, 2-4s		6.25		V
		Reg0x33[7:6]=11, 1s		3.25		V
		Reg0x33[7:6]=11, 2-4s		6.50		V
$t_{SYS\_PRO\_RISE\_DEG}$	Vsys Rising Deglitch for throttling			20		us
V_{ICRIT_PRO}	Input current rising threshold for throttling as percentage above ILIM2 (REG0x33[15:11])	Reg0x33[15:11]=00000	107	110	113	%
		Reg0x33[15:11]=01001	107	110	113	%
		Reg0x33[15:11]=11110	107	110	113	%
V_{INOM_PRO}	INOM rising threshold as percentage of IIN (REG0x3F())		107	110	113	%
V_{IDCHG_PRO}	IDCHG threshold for throttling for IDSCHG of 6A	Reg0x34 [15:10]=001100		6144		mA
			98		102	%
V_{INDEP_CMP}	Independent Comparator Threshold	Reg0x30[7]=1, CMPIN rising	1.17	1.2	1.23	V
		Reg0x30[7]=0, CMPIN rising	2.27	2.3	2.33	V
$V_{INDEP\_CMP\_HYS}$	Independent Comparator Hysteresis	Reg0x3B [6]=0, CMPIN falling		100		mV
F_{SW}	PWM Switching Frequency	Reg0x12[9]=0	680	800	920	kHz
		Reg0x12[9]=1	1020	1200	1380	kHz
V_{BATDRV_ON}	Gate Drive Voltage on BATFET		8.5	9.5	10.5	V
V_{BATDRV_DIODE}	Drain-source Voltage on BATFET during ideal diode operaiton			30		mV
R_{BATDRV_ON}	Measured by sourcing 100uA current to /BATDRV		3.0	3.5	4.0	kΩ
R_{BATDRV_OFF}	Measured by sinking 100uA current from /BATDRV		1.5	2.0	2.5	kΩ
$R_{DS\_HI\_ON\_Q1}$	High Side Driver (HSD) Turn-On Resistance	$V_{BTST1} – V_{SW1}$ = 5 V		4		Ω
$R_{DS\_HI\_OFF\_Q1}$	High Side Driver Turn-Off Resistance	$V_{BTST1} – V_{SW1}$ = 5 V		0.65	1.3	Ω
$V_{BTST1\_REFRESH}$	Bootstrap Refresh Comparator Falling Threshold Voltage	$V_{BTST1} – V_{SW1}$ when low side refresh pulse is requested	3.5	3.8	4.1	V
$R_{DS\_HI\_ON\_Q4}$	High Side Driver (HSD) Turn-On Resistance	$V_{BTST2} – V_{SW2}$ = 5 V		4		Ω
$R_{DS\_HI\_OFF\_Q4}$	High Side Driver Turn-Off Resistance	$V_{BTST2} – V_{SW2}$ = 5 V		0.65	1.3	Ω
$V_{BTST2\_REFRESH}$	Bootstrap Refresh Comparator Falling Threshold Voltage	$V_{BTST2} – V_{SW2}$ when low side refresh pulse is requested	3.5	3.8	4.1	V
$R_{DS\_LO\_ON\_Q2}$	Low Side Driver (LSD) Turn-On Resistance	$V_{BTST1} – V_{SW1}$ = 5.5V		5.5		Ω
$R_{DS\_LO\_OFF\_Q2}$	Low Side Driver Turn-Off Resistance	$V_{BTST1} – V_{SW1}$ = 5.5V		1	1.45	Ω
$R_{DS\_LO\_ON\_Q3}$	Low Side Driver (LSD) Turn-On Resistance	$V_{BTST2} – V_{SW2}$ = 5.5V		5.5		Ω
$R_{DS\_LO\_OFF\_Q3}$	Low Side Driver Turn-Off Resistance	$V_{BTST2} – V_{SW2}$ = 5.5V		1	1.45	Ω
SS_{STEP_DAC}	Soft Start Step Size	-		64		mA
SS_{STEP_DAC}	Soft Start Step Time	-		30		us
V_{F_D1}	Forward bias Voltage	I_F=20mA at 25C		0.8		V
V_{R_D1}	Reverse Breakdown Voltage	I_R=2uA at 25C			20	V
V_{F_D2}	Forward bias Voltage	I_F=20mA at 25C		0.8		V
V_{R_D2}	Reverse Breakdown Voltage	I_R=2uA at 25C			20	V
$t_{DEADTIME\_RISE}$	Driver Dead Time from Low Side to High Side			20		ns
$t_{DEADTIME\_FALL}$	Driver Dead Time from High Side to Low Side			20		ns
V_{IN_LO}	Input low threshold	I2C			0.4	V
		SMBus			0.8	V
V_{IN_HI}	Input high threshold	I2C	1.3			V

		SMBus	2.1			V
V_{OUT_LO}	Output Saturation Voltage	5 mA drain current			0.4	V
V_{OUT_LEAK}	Leakage Current	V = 7V	-1		1	μA
$V_{OUT\_LO\_PROCHOT}$	Output Saturation Voltage	50ohm pull up to 1.05V/5mA load			300	mV
$V_{OUT\_LEAK\_PROCHOT}$	Leakage Current	V = 5.5V	-1		1	μA
V_{CELL_4S}	4S	w.r.t. REGN	66	75		%
V_{CELL_3S}	3S	w.r.t. REGN	50	55	66	%
V_{CELL_2S}	2S	w.r.t. REGN	33	40	50	%
V_{CELL_1S}	1S	w.r.t. REGN	16.5	25	33	%
$R_{CELL\_BATPRES\_RISE}$	Battery is present	w.r.t REGN	16.5			%
$R_{CELL\_BATPRES\_FALL}$	Battery is removed.				0.9	V
I_{LEAK_COMP1}	COMP1 Leakage		-100		100	nA
I_{LEAK_COMP2}	COMP2 Leakage		-100		100	nA

9 Device Block Diagram (TBD)

10 Device Description

Note: Only SMBus register bits are referred in this section. For corresponding I2C register bits, please check 11.

10.1 Device HIZ State

The charger enters HIZ mode when ILIM_HIZ pin voltage is below 1V or REG0x32[15] is set to 1. During HIZ mode, the input source is present, and the charger is in the low quiescent current mode with REGN LDO enabled. The quiescent current is 100uA (typical) and 150uA(max).

10.2 Power Up from Battery without DC Source

If only battery is present and the voltage is above UVLOZ (2.7V rising and 2.4V falling), the BATFET turns on and connects battery to system. By default, the charger device is in low power mode (REG0x12[15]=1) with lowest quiescent current. The LDO stay off.
When device moves to performance mode (REG0x12[15]=0), The host enables IBAT buffer through SMBus/I2C to monitor discharge current. In order for PSYS, /PROCHOT or independent comparator, REGN LDO is enabled for accurate reference.

10.3 Power Up from DC Source

When an input source plugs in, the charger device checks the input source voltage to turn on LDO and all the bias circuits. It will sets the input current limit before starts the converter if the host hasn't written to REG0x3F(). The power up sequence from DC source is as below:

1. Enable 6V LDO
2. Input Voltage and Current Limit Setup
3. Battery CELL configuration
4. Converter Power-up

10.3.1.1 CHRG_OK Indicator

CHRG_OK is an active HIGH open drain indicator. It indicates the charger is in normal operation when the following conditions are valid.

- VBUS is above V_{ENCONV} (3.8V)
- VBUS below V_{ACOV} (24V)

10.3.2 Input Voltage and Current Limit Setup

After CHRG_OK goes HIGH, the converter is ready to start. The IINDPM in REG0x3F() is set to 1.5A (VBUS<V_{USB_QUAL}) or 3A (VBUS>V_{USB_QUAL}).
Charger device initiates a VBUS voltage measurement without load (VBUS@noLoad).

- VBUS<V_{USB_QUAL}, the default VINDPM threshold is VBUS@noLoad-640mV or 64mVx10.
- VBUS>V_{USB_QUAL}, the default VINDPM threshold is VBUS@noLoad-1.28V or 64mVx20.

After input current and voltage limits are set, the charger device is ready to power up. The host can always update input current and voltage limit based on input source type.
When a new adapter plugs in, the VINDPM threshold written by the host is discarded because host doesn't know what kind of input source is attached. If the previous value from host is higher than the new adapter voltage, charger won't be able to draw power from the new adapter, and system may not power up.

10.3.3 Battery Cell Configuration

CELL pin is biased with resistors from REGN to CELL to GND. After REGN LDO is activated, the device detects the battery configuration through CELL pin bias voltage.

10.4 Converter Operation

The charger employs a synchronous buck-boost converter that allows for charging from a standard 5V or high voltage power source. The charger operates in buck, buck-boost and boost mode. The buck-boost can operate uninterruptedly and continuously across the three operation modes.

Table 1 MOSFET Operation

Mode	Buck	Buck-boost	Boost
Q1	Switching	Switching	ON
Q2	Switching	Switching	OFF
Q3	OFF	Switching	Switching
Q4	ON	Switching	ON

10.5 High Accuracy Current and Power Monitor (IADPT, IDCHG and PSYS)

10.5.1 High Accuracy Current Sense Amplifier (IADP and IBAT)

As an industry standard, a high-accuracy current sense amplifier (CSA) is used to monitor the input current (IADP) and the charge/discharge current (IBAT). IADP voltage is 40X or 80X the differential voltage across ACP and ACN. IBAT voltage is 16X (during charging), or 8X/16X (during discharging) of the differential across SRP and SRN. After input voltage or battery voltage is above V(UVLO), IADP output becomes valid. To lower the voltage on current monitoring, a resistor divider from CSA output to GND can be used and accuracy over temperature can still be achieved.

$V_{(IADP)}$=40 or 80 × ($V_{(ACP)}$-$V_{(ACN)}$)

$V_{(IBAT)}$=16 × ($V_{(SRP)}$-$V_{(SRN)}$) during battery charging

$V_{(IBAT)}$=8 or 16 × ($V_{(SRN)}$-$V_{(SRP)}$) during battery discharging

A maximum 100-pF capacitor is recommended to connect on the output for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay. The CSA output voltage is clamped at 3.3 V.

10.5.2 High Accuracy Power Sense Amplifier (PSYS)

The charger monitors total available power from adapter and battery together. The ratio of PSYS current and total power K(PSYS) can be programmed in REG0x30[9] with default 1μA/W. The input and charge sense resistors (R_{AC} and R_{SR}) are programmed in REG0x30[11:10].

10.6 Processor Hot Indication

When CPU is running turbo mode, the peak power may exceed total available power from adapter and battery. The adapter current and battery discharge overshoot, or system voltage drop indicates the system power may be too high. When the adapter or battery is removed, the remaining power source may not support the peak power in turbo mode. The processor hot function monitors these events, and /PROCHOT pulse is asserted.

The /PROCHOT triggering events include:

- ICRIT: adapter peak current
- INOM: adapter average current (110% of input current limit)
- IDCHG: battery discharge current
- VSYS: system voltage on SRN for 2s - 4s battery
- ACOK: upon adapter removal (ACOK pin HIGH to LOW)
- BATPRES: upon battery removal (CELL_BATPRES pin goes LOW)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)

The threshold of ICRIT, IDCHG or VSYS, and the deglitch time of ICRIT, INOM, IDCHG or CMPOUT are programmable through SMBus/I2C. Each triggering event can be individually enabled in REG0x34[6:0].

When any event in PROCHOT profile is triggered, PROCHOT is asserted low for minimum 10ms programmable in 0x33[4:3]. At the end of the 10ms, if the PROCHOT event is still active, the pulse gets extended.

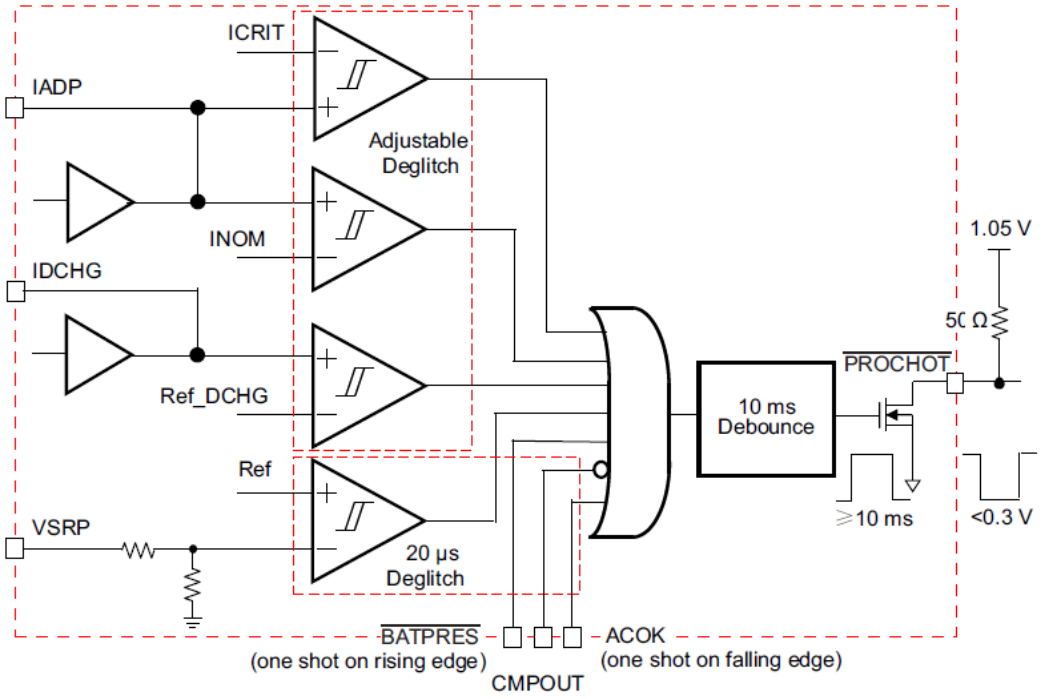

Figure 1 /PROCHOT Profile

10.7 Device Protection

10.7.1 Watchdog Timer

The charger includes watchdog timer to terminate charging if the charger does not receive a write MaxChargeVoltage() or write ChargeCurrent() command within 175s (adjustable via REG0x12[14:13]). When watchdog timeout occurs, all register values keep unchanged except ChargeCurrent() resets to zero. Battery charging is suspended. Write MaxChargeVoltage() or wirte ChargeCurrent() commands must be re-sent to reset watchdog timer and resume charging. Write REG0x12[14:13]=00 to disable watchdog timer also resume charging.

10.7.2 Input Over-voltage Protection (ACOV)

The charger has fixed ACOV voltage. When VBUS pin voltage is higher than ACOV, it is considered as adapter over voltage. CHRG_OK will be pulled low, and converter will be disabled. As system falls below battery voltage, BATFET will be turned on. When VCC pin voltage falls below ACOV, it is considered as adapter voltage returns back to normal voltage. CHRG_OK will be pulled high by external pull up resistor. The converter will resume if enable charge conditions are valid.

10.7.3 Input Over-current Protection (ACOC)

If the input current exceeds the 1.25X or 2X (REG0x31[2]) of ICRIT (REG0x33[15:11]) set point , converter stops switching. After 100ms, converter will start switching again.

10.7.4 Battery Over-voltage Protection (BATOVP)

Battery over-voltage may happen when battery is removed during charging or the user plugs in a wrong battery. The BATOVP threshold is 104% (1s) or 102% (2s – 4s) of regulation voltage set in REG0x15().

10.7.5 Battery Short

If BAT voltage falls below SYSMIN during charging, the maximum current is limited to 384mA.

10.7.6 Thermal Shutdown (TSHUT)

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature exceeds the 155°C. The charger stays off until the junction temperature falls below 135°C. During

thermal shut down, the LDO current limit is reduced to 16mA and REGN LDO stays off. Once the temperature falls below 135°C, charge can be resumed with soft start.

11 Programming

The charger supports battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 2 Charger Command Summary. The SMBUS address is 0x12H (0001001_X), where X is the read/write bit. The I2C address is D4H (1101010_X), where X is the read/write bit. ManufacturerID() and DeviceID() is assigned identify the charger device. The ManufacturerID() command always returns 0x0040H.

11.1 Register Maps

Table 2 Charger Command Summary

SMBus ADDR	I2C ADDR (MSB/LSB)	REGISTER NAME	R/W	DESCRIPTION	POR STATE
0x12	01/00	ChargeOption0()	R/W	Charge Option 0	•
0x14	03/02	ChargeCurrent()	R/W	7-bit Charge Current Setting	• LSB 64mA, Range: 8128mA
0x15	05/04	MaxChargeVoltage()	R/W	11-bit Charge Voltage Setting	• LSB 16mV • Default: 1S-4200mV, 2S-8400mV, 3S-12600mV, 4S-16800mV
0x30	31/30	ChargeOption1()	R/W	Charge Option 1	•
0x31	33/32	ChargeOption2()	R/W	Charge Option 2	•
0x32	35/34	ChargeOption3()	R/W	Charge Option 3	•
0x33	37/36	ProchotOption0()	R/W	/PROCHOT Option 0	•
0x34	39/38	ProchotOption1()	R/W	/PROCHOT Option 1	•
0x20	21/20	ChargerStatus()	RO	Charger Status	•
0x21	23/22	ProchotStatus()	RO	“Processor Hot” Trigger Events	•
0x22	25/24	IIN_DPM()	RO	7-bit Input Current Limit used for DPM	• LSB: 50mA, Range: 0mA-6350mA
0x3B	07/06	OTGVoltage()	R/W	8-bit input voltage DPM regulation threshold	• LSB 64mV, Range: 3776mV – 20096mV
0x3C	09/08	OTGCurrent()	R/W	7-bit OTG Output Current Limit	• LSB 50mA, Range: 0A – 6350mA
0x3D	0B/0A	InputVoltage()	R/W	8-bit input voltage DPM regulation threshold	• LSB 64mV, Range: 3800mV – 20120mV
0x3E	0D/0C	MinSystemVoltage()	R/W	6-Bit Minimum System Voltage Setting	• LSB: 256mV, Range: 1024mV-16182mV • Default: 1S-3.584V, 2S-6.144V, 3S-9.216V, 4S-12.288mV
0x3F	0F/0E	IIN_HOST()	R/W	6-bit Input Current Limit set by host	• LSB: 50mA, Range: 0mA-6350mA
0xFE	2E	ManufacturerID()	RO	Manufacturer ID	0x0040H
0xFF	2F	DeviceAddress()	RO	Device ID	

11.2 Setting Charge and /PROCHOT Options

Table 3. ChargeOption0 Register

SMBus 0x12H	I2C 01H	BIT NAME	DESCRIPTION
[15]	[7]	Low power Mode Enable (EN_LWPWR)	0: IC in performance mode with battery only. The /PROCHOT, current/power monitor buffer and comparator follow register setting. **1: IC in low power mode with battery only with lowest quiescent current.**

			<default @ POR>
[14:13]	[6:5]	WATCHDOG Timer Adjust (WDTMR_ADJ)	Set maximum delay between consecutive SMBus/I2C write of charge voltage or charge current command. If IC does not receive write on MaxChargeVoltage() or ChargeCurrent() within the watchdog time period, the charger will be suspended by setting ChargeCurrent() to 0mA. After expiration, the timer will resume upon the write of MaxChargeVoltage() or ChargeCurrent(). The charge will resume if the values are valid. 00: Disable Watchdog Timer 01: Enabled, 5 sec 10: Enabled, 88 sec **11: Enable Watchdog Timer, 175sec <default @ POR>**
[12]	[4]	IDPM Auto Disable (IDPM_AUTO_DISABLE)	When /BATPRES pin is LOW, the charger automatically disables the IDPM function by setting EN_IDPM (REG0x12[1]) to 0. The host can enable IDPM function later by writing EN_IDPM bit (REG0x12[1]) to 1. **0 – Disable this function. IDPM is not disabled when /BATPRES goes LOW <default @ POR>** 1 – Enable this function. IDPM is disabled when /BATPRES goes LOW.
[11]	[3]	Add OTG to CHRG_OK (OTG_ON_CHRGOK)	Drive CHRG_OK to HIGH when the device is in OTG mode. **0: Disable <default @ POR>** 1: Enable
[10]	[2]	Out of Audio Enable (EN_OOA)	**0: No limit of PFM burst frequency <default @ POR>** 1: Set minimum PFM burst frequency to above 25kHz to avoid audio noise
[9]	[1]	Switching Frequency (PWM_FREQ)	Two converter switching frequencies. One for small inductor and the other for big inductor. Inductor value: 1uH/1.5uH/2.2uH/3.3uH/4.7uH. Currently, customer uses 800kHz with 2.2uH/3.3uH, and 1.2MHz with 1uH/1.5uH. 0: 1200kHz **1: 800kHz default @ POR>**
[8]	[0]	Reserved	0 - Reserved
	I2C 00H	**BIT NAME**	**DESCRIPTION**
[7:6]	[7:6]	Reserved	0 - Reserved
[5]	[5]	LEARN Enable (EN_LEARN)	Set this bit 1 will enter LERN mode. In LEARN mode, converter turns off and BATFET turns on to discharge. Set this bit 0 will stop LEARN mode and turn back on buck converter. When /BATPRES pin is LOW, the IC exits LEARN mode and this bit is set back to 0. Upon LEARN mode exit, converter needs quick response to keep system from crashing. **0: Disable LEARN Mode <default @ POR>** 1: Enable LEARN Mode
[4]	[4]	IADP Amplifier Ratio (IADP_GAIN)	The ratio of voltage on IADP and voltage across ACP and ACN. **0: 40x <default @ POR>** 1: 80x
[3]	[3]	IBAT Amplifier Ratio (IBAT_GAIN)	The ratio of voltage on IBAT and voltage across ACN and ACP during battery discharging. 0: 8x **1: 16x <default @ POR>**
[2]	[2]	LDO Mode Enable (EN_LDO)	0: Disable LDO mode, BATFET fully ON. Precharge current is set by battery pack LDO. The system is regulated at MaxChargeVoltage(). **1: Enable LDO mode, Precharge current is set by ChargeCurrent() and clamped below 384mA (2 cell – 4 cell) or 2A (1 cell). The system is regulated at MinSystemVoltage() <default@POR>**
[1]	[1]	IDPM Enable (EN_IDPM)	Host writes this bit to enable IDPM regulation loop. When the IDPM is disabled by the charger (please refer to IDPM_AUTO_DISABLE), this bit goes LOW. 0 – IDPM disabled **1 – IDPM enabled <default @ POR>**
[0]	[0]	Charge Inhibit (CHRG_INHIBIT)	When this bit is 0, battery charging will start with valid MaxChargeVoltage() and ChargeCurrnet() values. **0: Enable Charge <default @ POR>**

			1: Inhibit Charge

Table 4. ChargeOption1 Register

SMBus 0x30H	I2C 31H	BIT NAME	DESCRIPTION
[15]	[7]	IBAT Enable (EN_IBAT)	Enable the IBAT output buffer. In low power mode (REG0x12[15]=1), IBAT buffer is always disabled regardless of this bit value. **0: Turn off IBAT buffer to minimize Iq <default @ POR>** 1: Turn on IBAT buffer
[14:13]	[6:5]	Reserved	0 - Reserved
[12]	[4]	PSYS Enable (EN_PSYS)	Enable PSYS sensing circuit and output buffer (whole PSYS circuit). In low power mode (REG0x12[15]=1), PSYS sensing and buffer are always disabled regardless of this bit value. **0: Turn off PMO buffer to minimize Iq <default @ POR>** 1: Turn on PSYS buffer
[11]	[3]	Input Sense Resistor (RSNS_RAC)	Input sense resistor RAC 0: 10mohm **<default @ POR>** 1: 20mohm
[10]	[2]	Charge Sense Resistor (RSNS_RSR)	Charge sense resistor RSR 0: 10mohm **<default @ POR>** 1: 20mohm
[9]	[1]	PSYS Gain (PSYS_RATIO)	Ratio of PSYS output current vs total input and battery power with 10mohm sense resistor. With the sense resistor is 10mohm (RAC and RSR) 0: 0.25uA/W **1: 1uA/W <default @ POR>**
[8]	[0]	Reserved	0 – Reserved
	I2C 30H	**BIT NAME**	**DESCRIPTION**
[7]	[7]	Independent Comparator Reference (CMP_REF)	Independent comparator internal reference. **0: 2.3V <default @ POR>** 1: 1.2V
[6]	[6]	Independent Comparator Polarity (CMP_POL)	Independent comparator output polarity **0: When CMPIN is above internal threshold, CMPOUT is LOW (internal hysteresis) <default @ POR>** 1: When CMPIN is below internal threshold, CMPOUT is LOW (external hysteresis)
[5:4]	[5:4]	Independent Comparator Deglitch Time (CMP_DEG)	Independent comparator deglitch time, only applied to the falling edge of CMPOUT (HIGH→LOW). 00: Independent comparator is disabled **01: Independent comparator is enabled with output deglitch time 1us <default @ POR>** 10: Independent comparator is enabled with output deglitch time 2ms 11 – Independent comparator is enabled with output deglitch time 5 sec
[3]	[3]	Force Power Path Off (FORCE_LATCHOFF)	When comparator triggers (usually monitors board temperature), charger turns off Q1 and Q4 (same as disable converter) so that the system is disconnected from the input source. At the same time, CHRG_OK signal goes to LOW to notify the system. **0 – Disable this function <default @ POR>** 1 – Enable this function
[2]	[2]	Reserved	0 – Reserved
[1]	[1]	Discharge SRN for Shipping	When this bit is 1, discharge BAT pin down below 3.8V in 140ms. When 140ms is over, this bit is reset to 0. **0 : Disable discharge mode <default @ POR>**

		Mode (EN_SHIP_DCHG)	1: Enable discharge mode
[0]	[0]	Auto Wakeup Enable (AUTO_WAKEUP_EN)	When this bit is HIGH, if the battery is below minimum system voltage (REG0x3E()), the IC will automatically enable 128mA charging current for 30 mins. Once the battery is charged up above minimum system voltage (by 5%?), charge will terminate and the bit is reset to LOW. 0: Disable **1: Enable <default @ POR> (set by EEPROM)**

Table 5. ChargeOption2 Register

SMBUs 0x31H	I2C 33H	BIT NAME	DESCRIPTION
[15:8]	[7:0]	Reserved	0 - Reserved
	I2C 32H	**BIT NAME**	**DESCRIPTION**
[7]	[7]	EN_EXTILIM	0: Input current limit is set by REG0x3F. **1: Input current limit is set by the lower value of ILIM pin and REG0x3F. <default @ POR>**
[6]	[6]	EN_ICHG_IDCHG	**0: IBAT pin as discharge current. <default @ POR>** 1: IBAT pin as charge current.
[5]	[5]	Q2 OCP Threshold (Q2_OCP)	Cycle-by-cycle OCP protection threshold by sensing voltage between GND and SW.. 0: Disable **1: 300mV <default @ POR>**
[4]	[4]	Q3 OCP Threshold (Q3_OCP)	Cycle-by-cycle OCP protection threshold by sensing voltage between GND and SW. 0: Disable **1: 300mV <default @ POR>**
[3]	[3]	ACOC Enable (EN_ACOC)	Input over-current (ACOC) protection by sensing the voltage across ACP and CAN. Upon ACOC (after 100us blank-out time), converter is disabled. 100ms later, the converter will turn on again. If 7 times of ACOC happens in 90sec, converter will be latched off. (?) **0: Disable ACOC <default @ POR>.** 1: ACOC threshold 125% or 200% ICRIT (REG0x33[8]).
[2]	[2]	ACOC Limit (ACOC_VTH)	Set MOSFET OCP threshold as percentage of IDPM with current sensed from R_{AC}. 0: 125% of ICRIT **1: 200% of ICRIT <default @ POR>**
[1]	[1]	BATOC Enable (EN_BATOC)	Battery discharge over-current (BATOC) protection by sensing the voltage across SRN and SRP. Upon BATOC, converter is disabled. Later, the converter will turn on again. 0: Disable BATOC <default @ POR>. **1: BATOC threshold 125% or 200% IDCHG (REG0x34[15:11]). <default @ POR>**
[0]	[0]	BATOC Limit (BATOC_VTH)	Set battery discharge over-current threshold as percentage of PROCHOT battery discharge current limit. 0: 125% of PROCHOT IDCHG **1: 200% of PROCHOT IDCHG <default @ POR>**

Table 6. ChargeOption3 Register

SMBus 0x32H	I2C 35H	BIT NAME	DESCRIPTION
[15]	[7]	Device HIZ Mode Enable (EN_HIZ)	When the charger is in HIZ mode, the device draws minimal quiescent current. With VBUS above UVLO. REGN LDO is off, and system powers from battery. **0: Device not in HIZ mode <default @ POR>** 1: Device in HIZ mode
[14]	[6]	Reset Registers (RESET_REG)	All the registers go back to default setting except VINDPM register. 0: Idle 1: Reset all the registers to default values. After reset, this bit goes back to 0.

[13]	5]	Reset VINDPM Threshold (RESET_VINDPM)	0: Idle 1: Re-measure VINDPM threshold when converter is disabled. After VINDPM is measured again, this bit goes back to 0 and converter starts.
[12]	[4]	OTG Mode Enable (EN_OTG)	Enable device in OTG mode **0: Not in OTG <default @ POR>** 1: In OTG mode to supply VBUS from battery
[11:8]	[3:0]	Reserved	0 - Reserved
	I2C 34H	**BIT NAME**	**DESCRIPTION**
[7:0]	[7:0]	Reserved	0 - Reserved

Table 7. ProchotOption0 Register

SMBus 0x33H	I2C 37H	BIT NAME	DESCRIPTION
[15:11]	[7:3]	ICRIT Threshold (ILIM2_VTH)	5 bits, percentage of IDPM in 0x3FH. Measure current between ACP and ACN. Trigger when the current is above this threshold. 00000:110% 00001:110% 00010:115% 00011:120%.... 10010:195% 10011:200% 10100:205% 10101:210% 10110:215% 10111:220% 11000:225% 11001:230% 11010:250% 11011:300% 11100:350% 11101:400% 11110:450% 11111:Out of Range (Ignored) Step: 5%, Default 150%
[10:9]	[2:1]	ICRIT Deglitch time (ICRIT_DEG)	ICRIT is set to be 110% of ILIM2. Typical ICRIT deglitch time to trigger /PROCHOT. 00: 15us **01: 100us <default @ POR>** 10: 400us (max 500us) 11: 800us (max 1ms)
[8]	[0]	Reserved	0 - Reserved
	I2C 36H	**BIT NAME**	**DESCRIPTION**
[7:6]	[7:6]	VSYS Threshold (VSYS_VTH)	Measure on SRP with fixed 20us deglitch time. Trigger when SYS pin voltage is below the threshold. 00: 5.75V (2-4s) or 2.85V (1s) **01: 6V (2-4s) or 3.1V (1s) <default @ POR>** 10: 6.25V (2-4s) or 3.35V (1s) 11: 6.5V (2-4s) or 3.6V (1s)
[5]	[5]	/PROCHOT Pulse Extension Enable (EN_PROCHOT_EXT)	When pulse extension is enabled, keep /PROCHOT pin voltage LOW till host write 0x33[2]=1. **0: Disable pulse extension <default @ POR>** 1: Enable pulse extension
[4:3]	[4:3]	/PROCHOT Pulse Width (PROCHOT_WIDTH)	Minimum /PROCHOT pulse width when REG0x33[5]=0 00: 100us 01: 1ms **10: 10ms <default @ POR>** 11: 5ms
[2]	[2]	/PROCHOT Pulse Clear (PROCHOT_CLEAR)	Clear /PROCHOT pulse when 0x3C[5]=1. 0: Clear /PROCHOT pulse and drive /PROCHOT pin HIGH. **1: Idle <default @ POR>**
[1]	[1]	INOM Deglitch Time (INOM_DEG)	INOM is always 10% above IDPM in 0x3FH. Measure current between ACP and ACN. Trigger when the current is above this threshold. Match bq24770. **0: 1ms (has to be max) <default @ POR>** 1: 50ms (max 60ms)

[0]	[0]	Reserved	0 – Reserved

Table 8. ProchotOption1 Register

SMBus 0x34H	I2C 39H	BIT NAME	DESCRIPTION
[15:10]	[7:2]	IDCHG Threshold (IDCHG_VTH)	6 bit, range, range 0A – 32256mA, step 512mA. Measure current between SRN and SRP. Trigger when the discharge current is above the threshold. If the value is programmed to 0mA, /PROCHOT is always triggered. **Default: 16384mA**
[9:8]	[1:0]	IDCHG Deglitch Time (IDCHG_DEG)	Match bq24770 as typical value. 00: 1.6ms **01: 100us <default @ POR>** 10: 6ms 11: 12ms
	I2C 38H	**BIT NAME**	**DESCRIPTION**
[7]	[7]	Reserved	0 – Reserved
[6:0]	[6:0]	/PROCHOT Profile (PROCHOT_PROFILE)	When adapter is present, the /PROCHOT function is enabled by the below bits. When adapter is removed, ICRIT, INOM /BATPRES and ACOK functions are automatically disabled in the /PROCHOT envelope. Independent comparator, IDCHG and VSYS function setting are preserved. When all the bits are 0, /PROCHOT function is disabled. Bit6: Independent comparator, **0: disable <default @ POR>**; 1: enable Bit5: ICRIT, 0: disable; **1: enable <default @ POR>** Bit4: INOM, **0: disable <default @ POR>**; 1: enable Bit3: IDCHG, **0: disable <default @ POR>**; 1: enable (In low power mode, in order to enable IDCHG in /PROCHOT,EN_ IDCHG bit (ChargeOptions1[11]) has to be HIGH too) Bit2: VSYS, **0: disable <default @ POR>**; 1: enable Bit1: /BATPRES, **0: disable <default @ POR>** ; 1: enable (one-shot rising edge triggered) If /BATPRES is enabled in /PROCHOT after battery is removed, it will immediately sent out /PROCHOT pulse. Bit0: ACOK, **0: disable <default @ POR>** ; 1: enable (one-shot falling edge triggered) ChargeOption0[15]=0 to assert /PROCHOT pulse after adapter removal. If /BATPRES is enabled in /PROCHOT after battery is removed, it will immediately sent out /PROCHOT pulse.

11.3 Charge and /PROCHOT Status

Table 9. Charger Status Register

SMBus 0x20H	I2C 21H	BIT NAME	DESCRIPTION
[15]	[7]	Input Source Status (AC_STAT)	Input source status, same as CHRG_OK bit 0: Input not present 1: Input is present
[14:13]	[6:5]	Reserved	0 - Reserved
[12]	[4]	IN_VINDPM	0: Charger is not in VINDPM 1: Charger is in VINDPM
[11]	[3]	IN_IINDPM	0: Charger is not in IINDPM 1: Charger is in IINDPM
[10]	[2]	IN_FCHRG	0: Charger is not in fast charge 1: Charger is in fast charger
[9]	[1]	IN_PCHRG	0: Charger is not in pre-charge 1: Charger is in pre-charge
[8]	[0]	IN_OTG	0: Charger is not in OTG 1: Charge is in OTG

	I2C 20H	BIT NAME	DESCRIPTION
[7]	[7]	Fault ACOV	The faults are latched until a read from host. 0: No fault; 1: ACOV
[6]	[6]	Fault BATOC	The faults are latched until a read from host. 0: No fault, 1: BATOC
[5]	[5]	Fault ACOC	The faults are latched until a read from host. 0: No fault; 1: ACOC
[4]	[4]	SYSOVP Status& Clear (SYSOVP_STAT)	When the SYSOVP occurs, this bit is HIGH. During the SYSOVP, the converter is disabled. After the SYSOVP is removed, the user must write a 0 to this bit or unplug the adapter to clear the SYSOVP condition to enable the converter again. **0: Not in SYSOVP <default @ POR>** 1: In SYSOVP. Once SYSOVP is removed, write 0 to clear SYSOVP latch.
[3:0]	[3:0]	Reserved	0 – Reserved

Table 10. ProchotStatus Register

SMBus 0x21H	I2C 23H	BIT NAME	DESCRIPTION (Read Only)
[15:8]	-	Reserved	0 – Reserved
	I2C 22H		
[7]	-	Reserved	0 – Reserved
[6:0]	[6:0]	/PROCHOT status (STAT)	The status bits can be reset back to 000 after: READ by host after /PROCHOT pulse is asserted; AND current /PROCHOT event is gone. Multiple /PROCHOT events: Assume there are two PROCHOT events, event A and event B. Event A triggers /PROCHOT first, but event B is also true. Both status bits will be HIGH. At the end of the 10ms /PROCHOT pulse, if /PROCHOT is still active (either by A or B), the /PROCHOT pulse is extended. Bit6: Independent comparator, 0: Not triggered; 1: Triggered Bit5: ICRIT, 0: Not triggered; 1: Triggered Bit4: INOM, 0: Not triggered; 1: Triggered Bit3: IDCHG, 0: Not triggered; 1: Triggered Bit2: VSYS, 0: Not triggered; 1: Triggered Bit1: /BATPRES, 0: Not triggered ; 1: Triggered Bit0: ACOK, 0: Not triggered ; 1: Triggered

11.4 ID Registers

Table 11. Manufacture ID Register

SMBus 0xFEH	I2C 2EH	BIT NAME	DESCRIPTION (Read Only)
[15:0]	[7:0]	MANUFACTURE_ID	0x0040H

Table 12. Device ID Register

SMBus 0xFFH	I2C 2FH	BIT NAME	DESCRIPTION (Read Only)
[15:8]	[7:0]	Reserved	0 – Reserved
[7:0]	[7:0]	DEVICE_ID	SMBUs: 0x40H I2C: 41H

11.5 Charge Current Register

To set the charge current, write a 16-bit ChargeCurrent() command (REG0x14()) using the data format listed in Table 13. Charge Current Register (0x14H) with 10mΩ Sense Resistor

With 10mΩ sense resistor, the charger provides charge current range of 64mA to 8.128A, with 64mA step resolution. Any write below 64mA is considered as 0mA. Upon POR, ChargeCurrent() is 0A. Any conditions for CHRG_OK low except ACOV will reset the ChargeCurrent() to zero. /BATPRES going LOW (battery removal) will reset ChargeCurrent() to 0A.

Charge current is not reset in ACOC, TSHUT, power path latch off (REG0x30[1]), and SYSOVP.

A 0.1μF capacitor between SRP and SRN for differential mode filtering is recommended; a 0.1μF capacitor between SRN and ground, and an optional 0.1μF capacitor between SRP and ground for common mode filtering. Meanwhile, the capacitance on SRP should not be higher than 0.1μF in order to properly sense the voltage across SRP and SRN for cycle-by-cycle current detection.

The SRP and SRN pins are used to sense voltage drop across RSR with default value of 10mΩ. However, resistors of other values can also be used. For a larger sense resistor, a larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss. If current sensing resistor value is too high, it may trigger an over current protection threshold because the current ripple voltage is too high. In such a case, either a higher inductance value or a lower current sensing resistor value should be used to limit the current ripple voltage level. A current sensing resistor value no more than 20mΩ is suggested.

Table 13. Charge Current Register (0x14H) with 10mΩ Sense Resistor

SMBus 0x14H	I2C 03H	BIT NAME	DESCRIPTION
15	7	-	Not used. 1 = invalid write.
14	6	-	Not used. 1 = invalid write.
13	5	-	Not used. 1 = invalid write.
12	4	Charge Current, bit 6	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current.
11	3	Charge Current, bit 5	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current.
10	2	Charge Current, bit 4	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current.
9	1	Charge Current, bit 3	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current.
8	0	Charge Current, bit 2	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current.
	I2C 02H		
7	7	Charge Current, bit 1	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current.
6	6	Charge Current, bit 0	0 = Adds 0mA of charger current. 1 = Adds 64mA of charger current.
5	5	-	Not used. Value Ignored.
4	4	-	Not used. Value Ignored.
3	3	-	Not used. Value Ignored.
2	2	-	Not used. Value Ignored.
1	1	-	Not used. Value Ignored.
0	0	-	Not used. Value Ignored.

11.5.1 Battery Pre-charge Current Clamp

During pre-charge, BATFET works in linear mode, or LDO mode (default REG0x12[2]=1) and system is regulated at MinSystemVoltage(). For 2-4 cell battery, the threshold from pre-charge to fast charge is the system minimum voltage, and the current is clamped at 384mA. For 1s battery, the threshold is fixed 3V rising and 2.8V falling, and the current is clamped at 2.048A.

11.6 Max Charge Voltage Register

To set the output charge voltage, write a 16-bit ChargeVoltage() command (REG0x15()) using the data format listed in Table 14. The charger provides charge voltage range from 1.024V to 19.200V, with 16mV step resolution. Any write below 1.024V is ignored. Upon POR or when charge is disabled, the system is regulated at MaxChargeVoltage().

Upon POR, REG0x15() is by default set as 4192mV for 1s, 8400mV for 2s, 12592mV for 3s or 16800mV for 4s. After CHRG_OK, if host writes REG0x14() before REG0x15(), the charge will start after the write to REG0x14().If the battery is different from 4.2V/cell, the host has to write to REG0x15() before REG0x14() for correct battery voltage setting. Write REG0x15() to 0 will set REG0x15() to default value on CELL pin, and force REG0x14() to zero to disable charge.

The SRN pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, and directly place a decoupling capacitor (0.1μF recommended) as close to IC as possible to decouple high frequency noise.

Table 14. MaxChargeVoltage Register (0x15H)

SMBus 0x15H	I2C 05H	BIT NAME	DESCRIPTION
15	7	-	Not used. 1 = invalid write.
14	6	Max Charge Voltage, bit 10	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage.
13	5	Max Charge Voltage, bit 9	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
12	4	Max Charge Voltage, bit 8	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
11	3	Max Charge Voltage, bit 7	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
10	2	Max Charge Voltage, bit 6	0 = Adds 0mV of charger voltage. 1 = Adds 1024mV of charger voltage.
9	1	Max Charge Voltage, bit 5	0 = Adds 0mV of charger voltage. 1 = Adds 512mV of charger voltage.
8	0	Max Charge Voltage, bit 4	0 = Adds 0mV of charger voltage. 1 = Adds 256mV of charger voltage.
	I2C 04H		
7	7	Max Charge Voltage, bit 3	0 = Adds 0mV of charger voltage. 1 = Adds 128mV of charger voltage.
6	6	Max Charge Voltage, bit 2	0 = Adds 0mV of charger voltage. 1 = Adds 64mV of charger voltage.
5	5	Max Charge Voltage, bit 1	0 = Adds 0mV of charger voltage. 1 = Adds 32mV of charger voltage.
4	4	Max Charge Voltage, bit 0	0 = Adds 0mV of charger voltage. 1 = Adds 16mV of charger voltage.
3	3	-	Not used. Value Ignored.
2	2	-	Not used. Value Ignored.
1	1	-	Not used. Value Ignored.
0	0	-	Not used. Value Ignored.

11.7 Minimum System Voltage Register

To set the minimum system voltage, write a 16-bit MinSystemVoltage() command (REG0x3E()) using the data format listed in Table 15. Minimum System Voltage Register The charger provides minimum system voltage range from 1.024V to 16.128V, with 256mV step resolution. Upon POR, MinSystemVoltage() is 3.584V for 1S, 6.144V for 2S and 9.216V for 3S, and 12.288V for 4S.

Table 15. Minimum System Voltage Register

SMBus 0x3EH	I2C 0DH	BIT NAME	DESCRIPTION

15	7	-	Not used. 1 = invalid write.
14	6	-	Not used. 1 = invalid write.
13	5	Min System Voltage, bit 5	0 = Adds 0mV of system Voltage. 1 = Adds 8192mV of system Voltage.
12	4	Min System Voltage, bit 4	0 = Adds 0mV of system Voltage. 1 = Adds 4096mV of system Voltage.
11	3	Min System Voltage, bit 3	0 = Adds 0mV of system Voltage. 1 = Adds 2048mV of system Voltage.
10	2	Min System Voltage, bit 2	0 = Adds 0mV of system Voltage. 1 = Adds 1024mV of system Voltage.
9	1	Min System Voltage, bit 1	0 = Adds 0mV of system Voltage. 1 = Adds 512mV of system Voltage.
8	0	Min System Voltage, bit 0	0 = Adds 0mV of system Voltage. 1 = Adds 256mV of system Voltage.
7		-	Not used. Value Ignored.
6		-	Not used. Value Ignored.
5		-	Not used. Value Ignored.
4		-	Not used. Value Ignored.
3		-	Not used. Value Ignored.
2		-	Not used. Value Ignored.
1		-	Not used. Value Ignored.
0		-	Not used. Value Ignored.

11.7.1 System Voltage during Operation

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The system voltage is regulated between MinSystemVoltage() and MaxChargeVoltage().

When battery voltage is above above MinSystemVoltage(), system is slightly above the battery voltage.

When battery voltage is below MinSystemVoltage(), system is regulated at MinSystemVoltage().

11.8 Input Current and Input Voltage Registers for Dynamic Power Management

System current normally fluctuates as portions of the system current when system are powered up or put to sleep. With the input current limit, the current rating requirement of the AC wall adapter can be lowered, reducing system cost.

The charger supports Dynamic Power Management (DPM). Normally, input power source provide power for system load and/or charge the battery. When the input current exceeds the input current setting, or the input voltage falls below input voltage setting, the charger decreases the charge current to provide priority to system load. As the system current rises, the available charge current drops accordingly toward zero. If the system load keeps increasing after charge current drops down to zero, the system voltage starts to drop. As the system voltage drops below battery voltage, the battery will discharge to supply the heavy system load.

11.8.1 Input Current Registers

To set the maximum input current limit, write a 16-bit IIN_HOST() command (REG0x3F()) using the data format listed in Table 16. IIN_HOST Register with 10mΩ Sense Resistor**Error! Reference source not found.** When using a 10mΩ sense resistor, the charger provides an input-current limit range of 50mA to 6350mA, with 50mA resolution. The default current limit is 3.25A. Due to USB current setting requirement, the register setting specifies the maximum current, instead of the typical current. Upon adapter removal, the input current limit is reset to 3.25A default.

The ACP and ACN pins are used to sense R_{AC} with default value of 10mΩ. However, resistors of other values can also be used. For a larger sense resistor, larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss.

Instead of using the internal DPM loop, the user can build up external input current regulation loop and have the feedback signal on ILIM.

$$V_{ILIM} = 1V + 40 \times \left(V_{ACP} - V_{ACN}\right) = 40 \times I_{DPM} \times R_{AC}$$

In order to disable ILIM pin, the host can write to 0x31[7] to disable ILIM pin, or pull ILIM pin above 3.0V.

With I2C, host only writes to REG0F() to set the value. REG0E() doesn't exist.

Table 16. IIN_HOST Register with 10mΩ Sense Resistor

SMBus 0x3FH	I2C 0FH	BIT NAME	DESCRIPTION
15	7	-	Not used. 1 = invalid write.
14	6	Input Current set by host, bit 6	0 = Adds 0mA of input current. 1 = Adds 3200mA of input current.
13	5	Input Current set by host, bit 5	0 = Adds 0mA of input current. 1 = Adds 1600mA of input current.
12	4	Input Current set by host, bit 4	0 = Adds 0mA of input current. 1 = Adds 800mA of input current.
11	3	Input Current set by host, bit 3	0 = Adds 0mA of input current. 1 = Adds 400mA of input current.
10	2	Input Current set by host, bit 2	0 = Adds 0mA of input current. 1 = Adds 200mA of input current.
9	1	Input Current set by host, bit 1	0 = Adds 0mA of input current. 1 = Adds 100mA of input current.
8	0	Input Current set by host, bit 0	0 = Adds 0mA of input current. 1 = Adds 50mA of input current.
	I2C 0EH		
7	7	-	Not used. Value Ignored.
6	6	-	Not used. Value Ignored.
5	5	-	Not used. Value Ignored.
4	4	-	Not used. Value Ignored.
3	3	-	Not used. Value Ignored.
2	2	-	Not used. Value Ignored.
1	1	-	Not used. Value Ignored.
0	0	-	Not used. Value Ignored.

IIN_DPM register reflects the actual input current limit programmed in the register.

Table 17. IIN_DPM Register with 10mΩ Sense Resistor

SMBus 0x22H	I2C 25H	BIT NAME	DESCRIPTION
15	7	-	Not used. 1 = invalid write.
14	6	Input Current in DPM, bit 6	0 = Adds 0mA of input current. 1 = Adds 3200mA of input current.
13	5	Input Current in DPM, bit 5	0 = Adds 0mA of input current. 1 = Adds 1600mA of input current.
12	4	Input Current in DPM, bit 4	0 = Adds 0mA of input current. 1 = Adds 800mA of input current.
11	3	Input Current in DPM, bit 3	0 = Adds 0mA of input current. 1 = Adds 400mA of input current.
10	2	Input Current in DPM, bit 2	0 = Adds 0mA of input current. 1 = Adds 200mA of input current.
9	1	Input Current in DPM, bit 1	0 = Adds 0mA of input current. 1 = Adds 100mA of input current.
8	0	Input Current in DPM, bit 0	0 = Adds 0mA of input current. 1 = Adds 50mA of input current.
	I2C 24H		
7	7	-	Not used. Value Ignored.
6	6	-	Not used. Value Ignored.
5	5	-	Not used. Value Ignored.

4	4	-	Not used. Value Ignored.
3	3	-	Not used. Value Ignored.
2	2	-	Not used. Value Ignored.
1	1	-	Not used. Value Ignored.
0	0	-	Not used. Value Ignored.

11.8.2 Input Voltage Register

To set the input voltage limit, write a 16-bit InputVoltage() command (REG0x3D()) using the data format listed in Table 18. Input Voltage Register **Error! Reference source not found.**If the input voltage drops more than the InputVoltage() allows, the device enters DPM and reduce the charge current. The default offset voltage is 600mV below the no-load VBus voltage.

In order to disable input voltage regulation, set VINDPM threshold 3.776V, below minimum converter operation voltage.

Table 18. Input Voltage Register

SMBus 0x3DH	I2C 0BH	BIT NAME	DESCRIPTION
15	7	-	Not used. 1 = invalid write.
14	6	-	Not used. 1 = invalid write.
13	5	Input Voltage, bit 7	0 = Adds 0mV of input voltage. 1 = Adds 8192mV of input voltage.
12	4	Input Voltage, bit 6	0 = Adds 0mV of input voltage. 1 = Adds 4096mV of input voltage.
11	3	Input Voltage, bit 5	0 = Adds 0mV of input voltage. 1 = Adds 2048mV of input voltage.
10	2	Input Voltage, bit 4	0 = Adds 0mV of input voltage. 1 = Adds 1024mV of input voltage.
9	1	Input Voltage, bit 3	0 = Adds 0mAVof input voltage. 1 = Adds 512mV of input voltage.
8	0	Input Voltage, bit 2	0 = Adds 0mV of input voltage. 1 = Adds 256mV of input voltage.
	I2C 0AH		
7	7	Input Voltage, bit 1	0 = Adds 0mV of input voltage. 1 = Adds 128mV of input voltage.
6	6	Input Voltage, bit 0	0 = Adds 0mV of input voltage. 1 = Adds 64mV of input voltage.
5	5	-	Not used. Value Ignored.
4	4	-	Not used. Value Ignored.
3	3	-	Not used. Value Ignored.
2	2	-	Not used. Value Ignored.
1	1	-	Not used. Value Ignored.
0	0	-	Not used. Value Ignored.

11.9 OTG Current and OTG Voltage Registers

11.9.1 OTG Voltage Register

To set the OTG output voltage limit, write to REG0x3B() using the data format listed in Table 19**Error! Reference source not found.**.

Table 19. OTG Voltage Register

SMBus 0x3BH	I2C 07H	BIT NAME	DESCRIPTION
15	7	-	Not used. 1 = invalid write.
14	6	-	Not used. 1 = invalid write.
13	5	OTG Voltage, bit 7	0 = Adds 0mV of OTG voltage. 1 = Adds 8192mV of OTG voltage.
12	4	OTG Voltage, bit 6	0 = Adds 0mV of OTG voltage.

			1 = Adds 12800mV of OTG voltage.
11	3	OTG Voltage, bit 5	0 = Adds 0mV of OTG voltage. 1 = Adds 6400mV of OTG voltage.
10	2	OTG Voltage, bit 4	0 = Adds 0mV of OTG voltage. 1 = Adds 3200mV of OTG voltage.
9	1	OTG Voltage, bit 3	0 = Adds 0mAVof OTG voltage. 1 = Adds 1600mV of OTG voltage.
8	0	OTG Voltage, bit 2	0 = Adds 0mV of OTG voltage. 1 = Adds 256mV of OTG voltage.
	I2C 06H		
7	7	OTG Voltage, bit 1	0 = Adds 0mV of OTG voltage. 1 = Adds 128mV of OTG voltage.
6	6	OTG Voltage, bit 0	0 = Adds 0mV of OTG voltage. 1 = Adds 64mV of OTG voltage.
5	5	-	Not used. Value Ignored.
4	4	-	Not used. Value Ignored.
3	3	-	Not used. Value Ignored.
2	2	-	Not used. Value Ignored.
1	1	-	Not used. Value Ignored.
0	0	-	Not used. Value Ignored.

11.9.2 OTG Current Register

To set the OTG output current limit, write to REG0x3C() using the data format listed in Table 20**Error! Reference source not found.**. The actual voltage is DC voltage plus the offset voltage.

Table 20. OTG Current Register

SMBus 0x3CH	I2C 09H	BIT NAME	DESCRIPTION
15	7	-	Not used. 1 = invalid write.
14	6	OTG Current set by host, bit 6	0 = Adds 0mA of OTG current. 1 = Adds 3200mA of OTG current.
13	5	OTG Current set by host, bit 5	0 = Adds 0mA of OTG current. 1 = Adds 1600mA of OTG current.
12	4	OTG Current set by host, bit 4	0 = Adds 0mA of OTG current. 1 = Adds 800mA of OTG current.
11	3	OTG Current set by host, bit 3	0 = Adds 0mA of OTG current. 1 = Adds 400mA of OTG current.
10	2	OTG Current set by host, bit 2	0 = Adds 0mA of OTG current. 1 = Adds 200mA of OTG current.
9	1	OTG Current set by host, bit 1	0 = Adds 0mA of OTG current. 1 = Adds 100mA of OTG current.
8	0	OTG Current set by host, bit 0	0 = Adds 0mA of OTG current. 1 = Adds 50mA of OTG current.
	I2C 08H		
7	7	-	Not used. Value Ignored.
6	6	-	Not used. Value Ignored.
5	5	-	Not used. Value Ignored.
4	4	-	Not used. Value Ignored.
3	3	-	Not used. Value Ignored.
2	2	-	Not used. Value Ignored.
1	1	-	Not used. Value Ignored.
0	0	-	Not used. Value Ignored.

12 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 31) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to switching MOSFET's supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET's gate pins and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.
3. Place inductor input pin to switching MOSFET's output pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 32 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC
5. Place output capacitor next to the sensing resistor output and ground 6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling
8. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground (power pad should tie to analog ground in this case if possible).
9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible 10. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground.

Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.

11. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the WQFN information, See SCBA017 and SLUA271.