Power up for eMMC Application Note

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Purpose

This application note will show eMMC power-up and guide you how to provide power supply in the systems using eMMC.

This application note focuses on the initial power up state that system designers have to confirm to escape from booting failure.

Special attention is given to the necessary current for the power-on slop, bump and power noise. This is helpful for mobile system hardware engineers.

References

- JEDEC eMMC Card Product Std

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1. eMMC Power up & Guidelines

1.1 eMMC power-up guidelines

An eMMC bus power-up is handled locally in each device and in the bus master. Figure 1 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence.

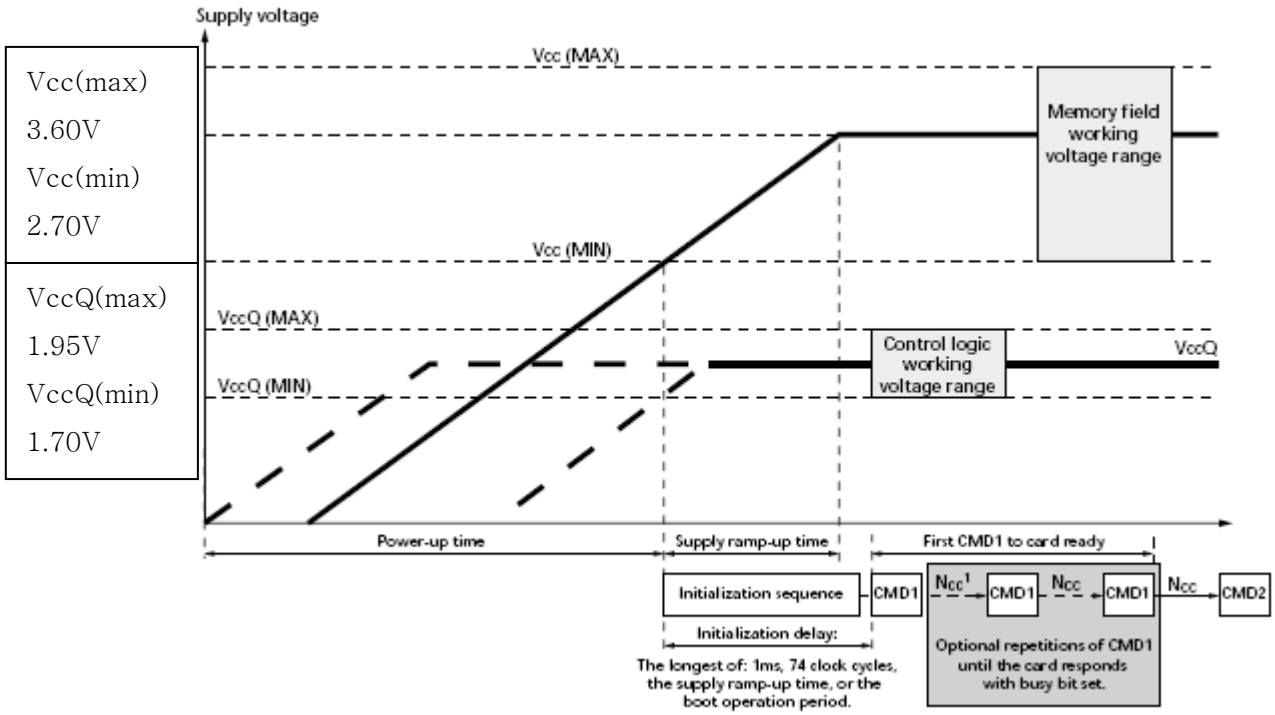

Figure 1 Power-up diagram

1.2 eMMC power-up guidelines

An eMMC power-up must adhere to the following guidelines:

• **When power-up is initiated, VCC should be ramped up first, or both can be ramped up simultaneously. To have more stable power up state, Vcc should be ramped up earlier than VccQ**.

• After power up, the eMMC enters the pre-idle state.

• If the eMMC does not support boot mode or its BOOT_PARTITION_ENABLE bit is cleared, the

eMMC moves immediately to the idle state. While in the idle state, the eMMC ignores all bus transactionsuntil CMD1 is received. If the eMMC supports only specification v4.2 or earlier versions, the device enters the idle state immediately following power-up.

• If the BOOT_PARTITION_ENABLE bit is set, the eMMC moves to the pre-boot state, and the

eMMC waits for the boot-initiation sequence. Following the boot operation period, the eMMC enters the idle state. During the pre-boot state, if the eMMC receives any CMD-line transaction other than the boot initiation sequence (keeping CMD line low for at least 74 clock cycles) and CMD1, the eMMC moves to the Idle state. If eMMC receives the boot initiation sequence (keeping the CMD line low for at least 74 clock cycles), the eMMC begins boot operation. After boot operation is terminated, the eMMC enters the idle state and shall be ready for CMD1 operation. If the eMMC receives CMD1 in the preboot state, it begins responding to the command and moves to the card identification mode.

• While in the idle state, the eMMC ignores all bus transactions until CMD1 is received.

• CMD1 is a special synchronization command used to negotiate the operation voltage range and to poll the device until it is out of its power-up sequence. In addition to the operation voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready, and the host must wait until this bit is cleared. The device must complete its initialization within
1 second of the first CMD1 issued with a valid OCR range.

• The bus master moves the device out of the idle state. Because the power-up time and the supply rampup time depend on application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.

• After power-up, the host starts the clock and sends the initializing sequence on the CMD line. The sequence length is the longest of: 1ms, 74 clocks, the supply ramp-up time, or the boot operation period. An additional 10 clocks (beyond the 64 clocks of the power-up sequence) are provided to eliminate power-up synchronization problems.

• Every bus master must implement CMD1.

2. Power up Failure Example.

2.1 VccQ is ramped up earlier than Vcc.

If VccQ is ramped up earlier than Vcc, the power of controller could be working, but there is no response until Flash Memory using Vcc wakes up. It is major booting up failure during power up cycling. Figure 2 show the failure sequence.

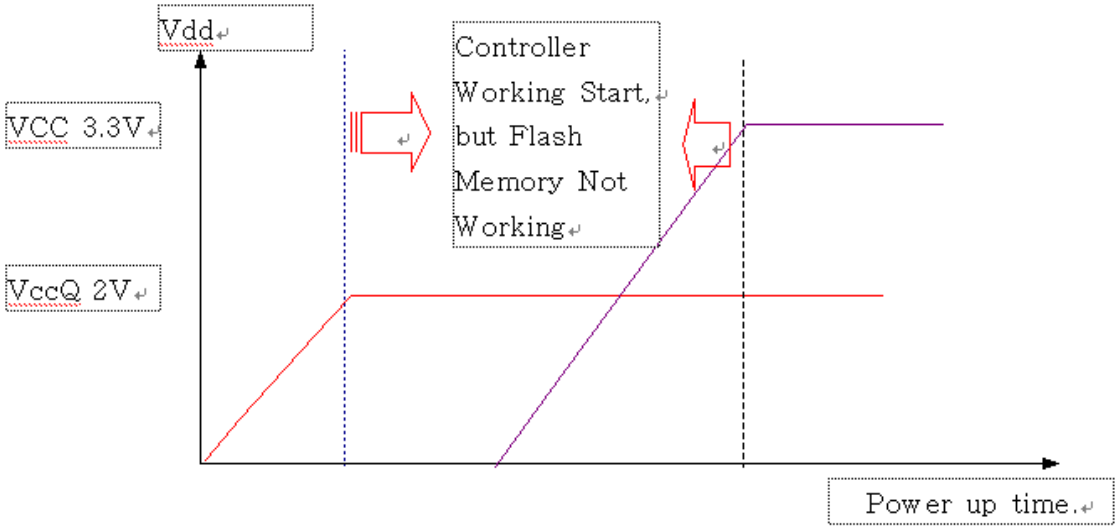

Figure 2 Power-up Failure Example (VccQ Earlier than Vcc)

2.2 Vcc and VccQ are ramped up simultaneously but slow slop.

As we mentioned previous chapter, Vcc and VccQ could be ramped up simultaneously. If the slop is too slow or the slop has step range, it makes failure at booting up. (Controller has been ready to send CMD, but Flash Memory not

Figure3 displays those kinds of failures.

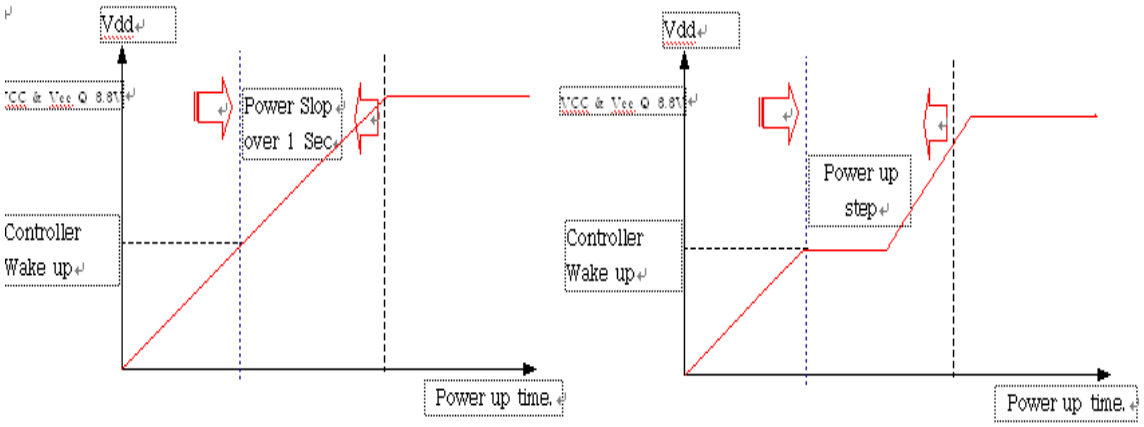

Figure 3 Power Slow up and step pulse failure

2.3 Failure condition Bump or Fluctuation at power up

If the power supply on the system is unstable and has bump or fluctuation, it makes eMMC failure.

Figure4 shows that failure occurs on the condition Bump voltage which is under Flash memory operation Voltage.

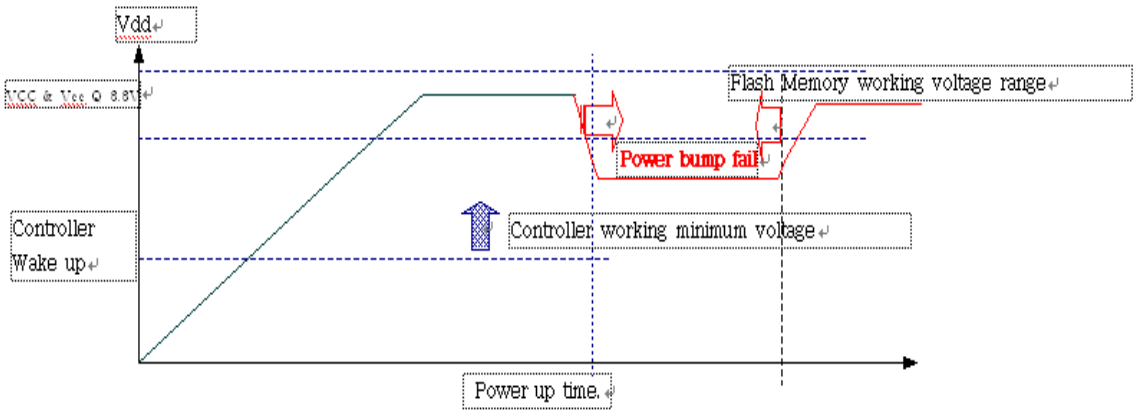

Figure 4 Power Bump or Fluctuation failures