Samsung e·MMC Product family

e.MMC 5.0 Specification compatibility

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	1. Initial issue	Feb. 27, 2013	Target	S.M.Lee
0.1	1. User density and part number of 16GB product are changed in Table 1 2. Extended CSD Registers are updated in Chapter 6.4 - OPT_ERASE_SIZE is Chasnged to 0x01 - SEC_COUNT of 16GB is changed to 0x1D1F000 - RPMB_SIZE_MULT of 8GB is changed to 0x04 - RPMB_SIZE_MULT of 16,32,64GB is changed to 0x20 - MAX_ENH_SIZE_MULT of 16GB is changed to 0x3A3	Mar. 20, 2013	Target	S.M.Lee
0.2	1. Part numbers are changed in Table 1	Apr. 19, 2013	Target	S.M.Lee
1.0	1. Performance of 64GB is changed in Table 15 2. Extended CSD Registers are updated in Chapter 6.4 - Register values are updated according to JEDEC eMMC5.0 3. Clock duty cycle of device input and output timing in HS400 mode is changed in Chapter 7.3.1 and 7.3.2 respectively 4. Active power of 64GB is changed in Table 27 5. C_{BGA} naming is changed to C_{DEVICE} in Chapter 8.5 6. Min. value of C_{DEVICE} is deleted and CL value is changed to 13pF in Table 32	May. 31, 2013	Final	S.M.Lee

Revision History Appendix(0.1)

Before(ver.0.0)

[Table 1] Product List

Capacities	e-MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
8 GB	KLM8G1GEAC-B001	64Gb MLC x 1	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
16 GB	KLMAG2GEAC-B002	64Gb MLC x 2	91.7%			
32 GB	KLMBG4GEAC-B001	64Gb MLC x 4	91.0%			
64 GB	KLMCG8GEAC-B001	64Gb MLC x 8			11.5mm x 13mm x 1.2mm	

[Table 20] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD slice	CSD Value			
					8GB	16GB	32GB	64GB
Optimal Erase Size	OPT_ERASE_SIZE	1	R	[257]	0x02			
Sector Count	SEC_COUNT	4	R	[215:212]	0xE90000	0x1D5A000	0x3A3E000	0x747C000
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x04			
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x1D2	0x3AB	0x747	0xE8F

After(ver.0.1)

[Table 1] Product List

Capacities	e-MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
8 GB	KLM8G1GEAC-B001	64Gb MLC x 1	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
16 GB	KLMAG2GEAC-B001	64Gb MLC x 2				
32 GB	KLMBG4GEAC-B001	64Gb MLC x 4				
64 GB	KLMCG8GEAC-B001	64Gb MLC x 8			11.5mm x 13mm x 1.2mm	

[Table 20] Extended CSD Register

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Optimal Erase Size	OPT_ERASE_SIZE	1	R	[257]	0x01			
Sector Count	SEC_COUNT	4	R	[215:212]	0xE90000	0x1D1F000	0x3A3E000	0x747C000
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x04		0x20	
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x1D2	0x3A3	0x747	0xE8F

Revision History Appendix(0.2)

Before(ver.0.1)

[Table 1] Product List

Capacities	e-MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
8 GB	KLM8G1GEAC-B001	64Gb MLC x 1	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
16 GB	KLMAG2GEAC-B001	64Gb MLC x 2				
32 GB	KLMBG4GEAC-B001	64Gb MLC x 4				
64 GB	KLMCG8GEAC-B001	64Gb MLC x 8			11.5mm x 13mm x 1.2mm	

After(ver.0.2)

[Table 1] Product List

Capacities	e-MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
8 GB	KLM8G1GEAC-B031	64Gb MLC x 1	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
16 GB	KLMAG2GEAC-B031	64Gb MLC x 2				
32 GB	KLMBG4GEAC-B031	64Gb MLC x 4				
64 GB	KLMCG8GEAC-B031	64Gb MLC x 8			11.5mm x 13mm x 1.2mm	

Revision History Appendix(1.0)

Before(ver.0.2)

[Table 15] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
8 GB	175	18
16 GB	220	40
32 GB	250	50
64 GB		70

* Test / Estimation Condition : Bus width x8, 200MHz DDR, 512KB data transfer, w/o file system overhead

7.3.1 HS400 Device Input Timing

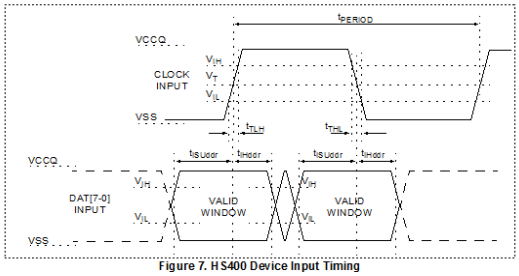

Figure 7. HS400 Device Input Timing

NOTE:
1) t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min).
2) V_{IH} denotes V_{IH}(min.) and V_{IL} denotes V_{IL}(max.)

[Table 22] HS400 Device input timing

Parameter	Symbol	Min	Max.	Unit
Input CLK				
Cycle time data transfer mode	t_{PERIOD}	5	-	ns
Clock rising / falling time	t_{TLH}, t_{THL}	-	0.1 * t_{PERIOD}	ns
Clock duty cycle		47.5	52.5	%
Input DAT (referenced to CLK)				
Input set-up time	tISUddr	0.4		ns
Input hold time	tIHddr	0.4		ns

After(ver.1.0)

[Table 15] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
8 GB	175	18
16 GB	220	40
32 GB	250	50
64 GB		

* Test / Estimation Condition : Bus width x8, 200MHz DDR, 512KB data transfer, w/o file system overhead

[Table 20] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value			
					8GB	16GB	32GB	64GB
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00			
Supported modes	SUPPORTED_MODES	1	R	[493]	0x01			
FFU features	FFU_FEATURES	1	R	[492]	0x00			
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00			
FFU Argument	FFU_ARG	4	R	[490:487]	0x00			
Number of received sectors	NUMBER_OF_RECEIVED_SECTORS	4	R	[305:302]	0x00			
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0x00			
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x01			
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x01			
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01			
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x00			
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x08	0x10	0x20	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01			
Device version	DEVICE_VERSION	2	R	[263:262]	0x00			
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	FW Patch Ver.			
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00			
Product state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x00			
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x07			
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00			
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00			
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00			
FFU status	FFU_STATUS	1	R	[26]	0x00			
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]				
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	0x00			
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x00			
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x09			
Reserved[1]		16	-	[15:0]				

7.3.1 HS400 Device Input Timing

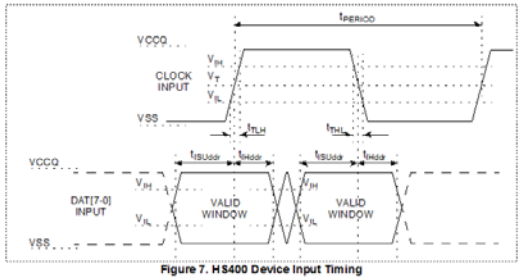

Figure 7. HS400 Device Input Timing

NOTE:
1) t_{ISU} and t_{IH} are measured at V_{IL} (max.) and V_{IH}(min).
2) V_{IH} denotes V_{IH}(min.) and V_{IL} denotes V_{IL} (max.)

[Table 22] HS400 Device input timing

Parameter	Symbol	Min	Max.	Unit
Input CLK				
Cycle time data transfer mode	t_{PERIOD}	5	-	ns
Clock rising / falling time	t_{TLH}, t_{THL}	-	0.1 t_{PERIOD} (=0.5)	ns
Clock duty cycle		46	54	%
Input DAT (referenced to CLK)				
Input set-up time	tISUddr	0.4		ns
Input hold time	tIHddr	0.4		ns

NOTE :
1) It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

7.3.2 HS400 Device Output Timing

RCLK is used to read data (data read and CRC status response read) in HS400 mode. The device output value of RCLK is "High-Z" when the device is not in outputting data(data read, CRC status response). RCLK is toggled only during data read period.

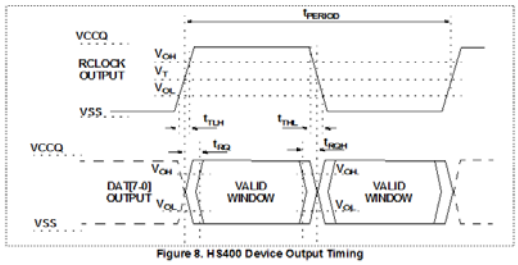

Figure 8. HS400 Device Output Timing

NOTE:
V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

[Table 23] HS400 Device Output timing

Parameter	Symbol	Min	Max.	Unit
	Output RCLK			
Cycle time data transfer mode	t_{PERIOD}	5	-	ns
Clock rising/falling time	t_{TLH}, t_{THL}	-	0.16*t_{PERIOD}	ns
Clock duty cycle		45	55	%
	Output DAT (referenced to RCLK)			
Output hold skew	tIRQ		0.4	ns
Output hold time	tIRQH		0.4	ns

[Table 27] Active Power Consumption during operation

Density	NAND Type	CTRL	NAND	Unit
8 GB	64Gb MLC x 1	150	80	mA
16 GB	64Gb MLC x 2		130	
32 GB	64 Gb MLC x4		230	
64 GB	64Gb MLC x 8		430	

* Power Measurement conditions: Bus configuration =x8 @200MHz DDR
* The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

8.5 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST} the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the e·MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 31] Bus Signal Line Load

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{BGA}			12	pF	
Maximum signal line inductance				16	nH	f_{pp} <= 52 MHz

[Table 32] Capacitance and Resistance for HS400 mode

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	CL			14	pF	Single Device
Single Device capacitance	C_{BGA}	4		6	pF	
Pull-down resistance for RCLK	R_{RCLK}	10		100	KOhm	

7.3.2 HS400 Device Output Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode. The device output value of Data Strobe is "High-Z" when the device is not in outputting data(data read, CRC status response). Data Strobe is toggled only during data read period.

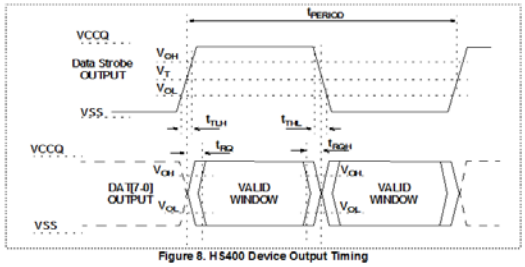

Figure 8. HS400 Device Output Timing

NOTE:
V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

[Table 23] HS400 Device Output timing

Parameter	Symbol	Min	Max.	Unit
	Output Data Strobe			
Cycle time data transfer mode	t_{PERIOD}	5	-	ns
Clock rising/falling time	t_{TLH}, t_{THL}	-	0.16 t_{PERIOD} (=0.8)	ns
Clock duty cycle		42	58	%
	Output DAT (referenced to Data Strobe)			
Output hold skew	tRQ		0.4	ns
Output hold time	tRQH		0.4	ns

NOTE :
1) It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

[Table 27] Active Power Consumption during operation

Density	NAND Type	CTRL	NAND	Unit
8 GB	64Gb MLC x 1	150	80	mA
16 GB	64Gb MLC x 2		130	
32 GB	64 Gb MLC x4		230	
64 GB	64Gb MLC x 8			

* Power Measurement conditions: Bus configuration =x8 @200MHz DDR
* The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

8.5 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST} the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the e·MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 31] Bus Signal Line Load

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Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			12	pF	
Maximum signal line inductance				16	nH	f_{pp} <= 52 MHz

[Table 32] Capacitance and Resistance for HS400 mode

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	CL			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	

Table Of Contents

INTRODUCTION

SAMSUNG e·MMC is an embedded MMC solution designed in a BGA package form. e·MMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.0 which is a industry standard.

e·MMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG e•MMC supports 200MHz DDR – up to 400MBps with bus widths of 8 bit in order to improve sequential bandwidth, especially sequential read performance.

There are several advantages of using e·MMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash management software or FTL(Flash Transition Layer) of e·MMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

1.0 PRODUCT LIST

[Table 1] Product List

Capacities	e·MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
8 GB	KLM8G1GEAC-B031	64Gb x 1	91.0%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA
16 GB	KLMAG2GEAC-B031	64Gb x 2				
32 GB	KLMBG4GEAC-B031	64Gb x 4				
64 GB	KLMCG8GEAC-B031	64Gb x 8			11.5mm x 13mm x 1.2mm	

2.0 KEY FEATURES

• embedded MultiMediaCard Ver. 5.0 compatible. Detail description is referenced by JEDEC Standard

• SAMSUNG e·MMC supports features of eMMC4.5 which are defined in JEDEC Standard

- Supported Features : Packed command, Cache, Discard, Sanitize, Power Off Notification, Data Tag, Partition types, Context ID, Real Time Clock, Dynamic Device Capacity, HS200

- Non-supported Features : Large Sector Size (4KB)

• Additional features of eMMC5.0 : HS400 mode (200MHz DDR - up to 400Mbps), Field Firmware Update, Device Health Report, Sleep Notification, Secure Removal Type

• Full backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-e·MMC systems)

• Data bus width : 1bit (Default), 4bit and 8bit

• MMC I/F Clock Frequency : 0 ~ 200MHz
MMC I/F Boot Frequency : 0 ~ 52MHz

• Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)

• Power : Interface power → VDD(VCCQ) (1.70V ~ 1.95V or 2.7V ~ 3.6V) , Memory power → VDDF(VCC) (2.7V ~ 3.6V)

3.0 PACKAGE CONFIGURATIONS

3.1 153 Ball Pin Configuration

[Table 2] 153 Ball Information

Pin NO	Name
A3	DAT0
A4	DAT1
A5	DAT2
B2	DAT3
B3	DAT4
B4	DAT5
B5	DAT6
B6	DAT7
K5	RSTN
C6	VDD
M4	VDD
N4	VDD
P3	VDD
P5	VDD
E6	VDDF
F5	VDDF
J10	VDDF
K9	VDDF
C2	VDDI
M5	CMD
H5	Data Strobe
M6	CLK
J5	VSS
A6	VSS
C4	VSS
E7	VSS
G5	VSS
H10	VSS
K8	VSS
N2	VSS
N5	VSS
P4	VSS
P6	VSS

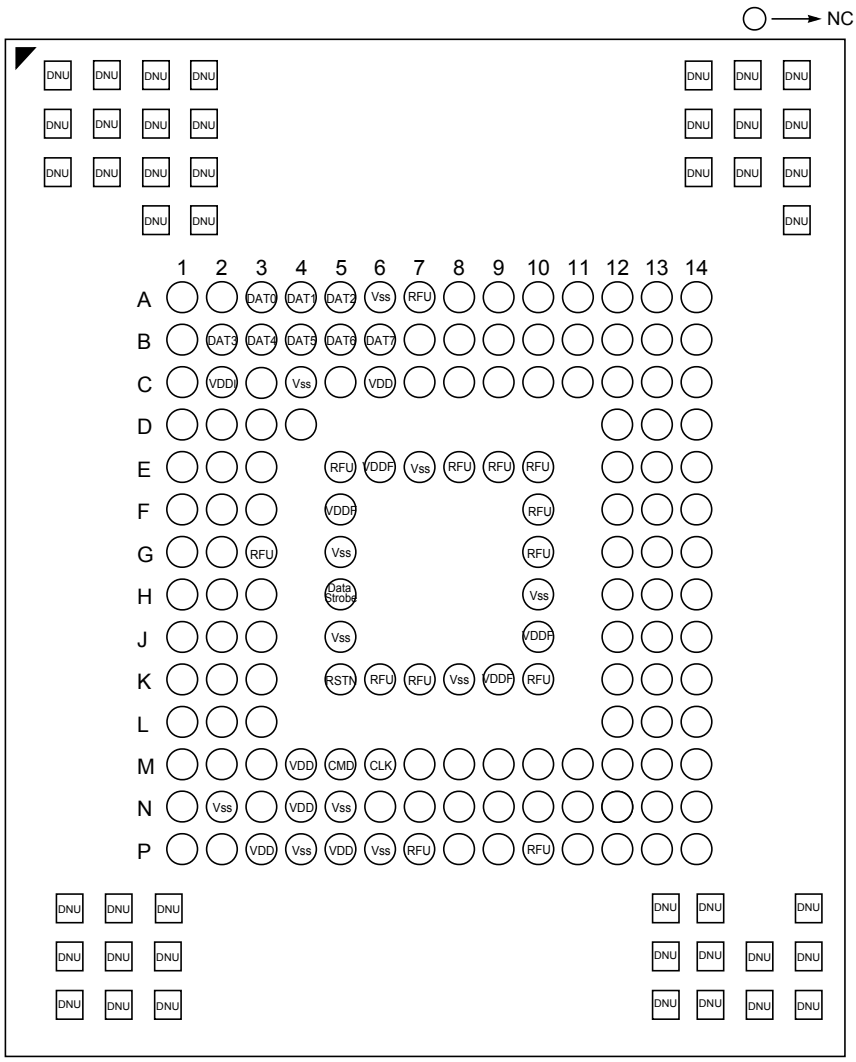


Figure 1. 153-FBGA

- CLK : Clock input
- Data Strobe : Newly assigned pin for HS400 mode. Data Strobe is generated from e.MMC to host.
  In HS400 mode, read data and CRC response are synchronized with Data Strobe.
- CMD : A bidirectional signal used for device initialization and command transfers.
  Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
- DAT0-7 : Bidirectional data channels. It operates in push-pull mode.
- RST_n : H/W reset signal pin
- VDDF(VCC) : Supply voltage for flash memory
- VDD(VCCQ) : Supply voltage for memory controller
- VDDi : Internal power node to stabilize regulator output to controller core logics
- VSS : Ground connections

3.1.1 11.5mm x 13mm x 1.0mm Package Dimension

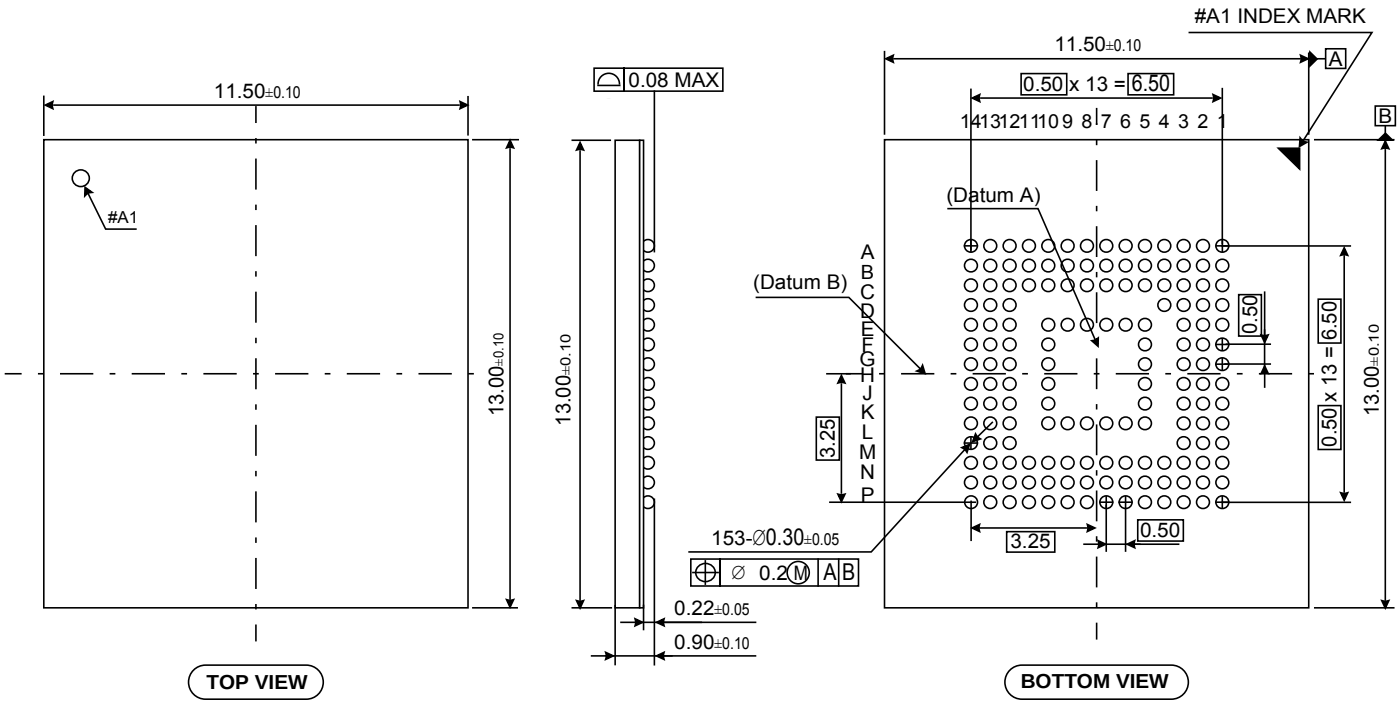


Figure 2. 11.5mm x 13mm x 1.0mm Package Dimension

3.1.2 11.5mm x 13mm x 1.2mm Package Dimension

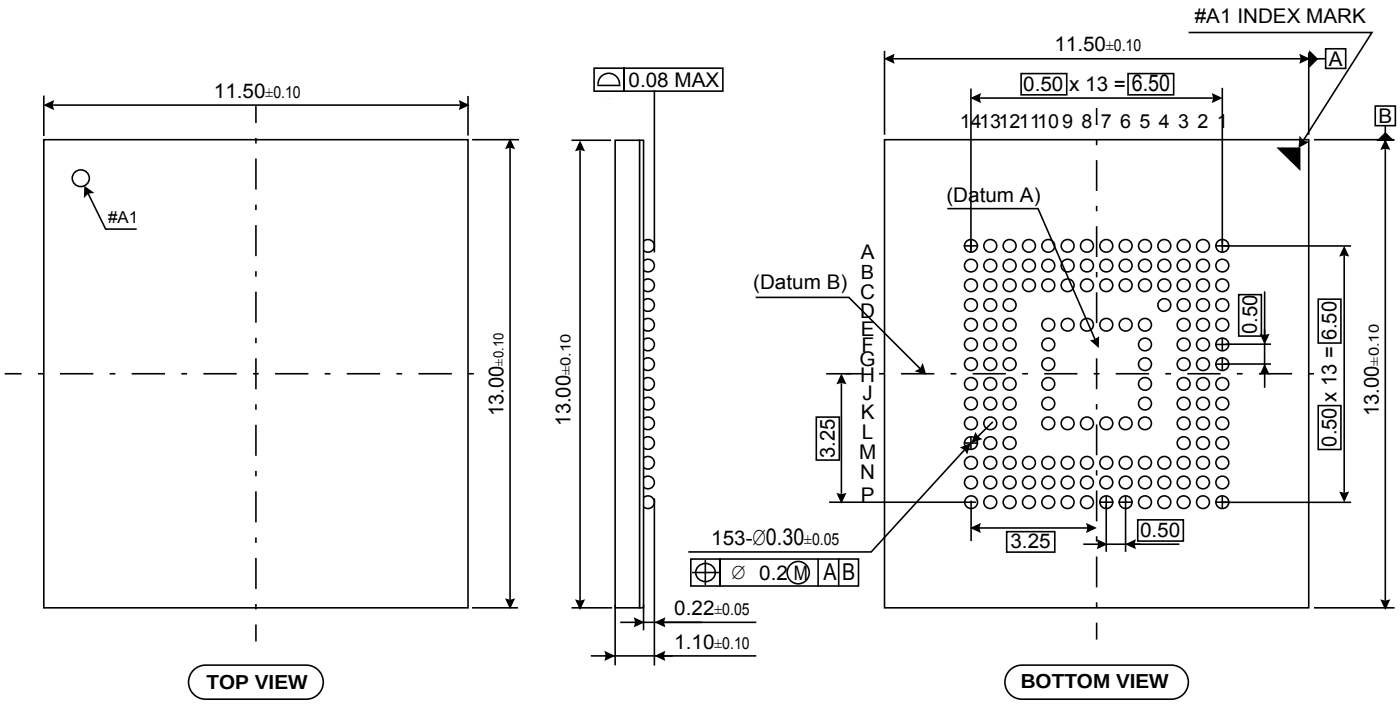


Figure 3. 11.5mm x 13mm x 1.0mm Package Dimension

3.2 Product Architecture

- e·MMC consists of NAND Flash and Controller. V_{DD} (V_{CCQ}) is for Controller power and V_{DDF} (V_{CC})is for flash power

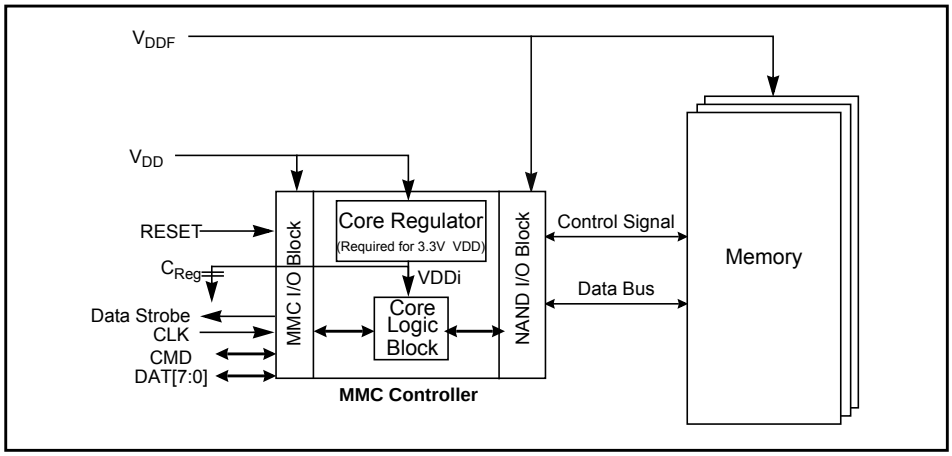


Figure 4. e·MMC Block Diagram

4.0 e.MMC 5.0 feature

4.1 HS400 mode

e.MMC5.0 product supports high speed DDR interface timing mode up to 400MB/s at 200MHz with 1.8V I/O supply.

HS400 mode supports the following features :
- DDR Data sampling method
- CLK frequency up to 200MHz DDR – up to 400Mbps
- Only 8-bits bus width available
- Signaling levels of 1.8V
- Six selectable Drive Strength (refer to the table below)

[Table 3] I/O driver strength types

Driver Type	HS200 & HS400 Support	Nominal Impedance	Approximated driving capability compared to Type-0	Remark
0	Default	50Ω	x1	Default Driver Type. Supports up to 200MHz operation.
1	Optional	33Ω	x1.5	Supports up to 200MHz Operation.
2	Optional	66Ω	x0.75	The weakest driver that supports up to 200MHz operation.
3	Optional	100Ω	x0.5	For low noise and low EMI systems. Maximal operating frequency is decided by Host design.
4	Optional	40Ω	x1.2	Supports up to 200MHz DDR operation

NOTE:
1) Support of Driver Type-0 is default for HS200 & HS400 Device, while supporting Driver types 1~4 are optional for HS200 & HS400 Device.
2) It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

[Table 4] Device type values (EXT_CSD register : DEVICE_TYPE [196])

Bit	Device Type	Supportability
7	HS400 Dual Data Rate e•MMC @ 200 MHz - 1.2V I/O	Not support
6	HS400 Dual Data Rate e•MMC @ 200 MHz - 1.8V I/O	Support
5	HS200 Single Data Rate *e*•MMC @ 200 MHz - 1.2V I/O	Not support
4	HS200 Single Data Rate *e*•MMC @ 200 MHz - 1.8V I/O	Support
3	High-Speed Dual Data Rate *e*•MMC @ 52MHz - 1.2V I/O	Not support
2	High-Speed Dual Data Rate *e*•MMC @ 52MHz - 1.8V or 3V I/O	Support
1	High-Speed *e*•MMC @ 52MHz - at rated device voltage(s)	Support
0	High-Speed *e*•MMC @ 26MHz - at rated device voltage(s)	Support

NOTE:
1) It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

[Table 5] Extended CSD revisions (EXT_CSD register : EXT_CSD_REV [192])

Value	Timing Interface	EXT_CSD Register Value
255-8	Reserved	-
7	Revision 1.7 (for MMC V5.0)	0x07[1)]
6	Revision 1.6 (for MMC V4.5, V4.51)	-
5	Revision 1.5 (for MMC V4.41)	-
4	Revision 1.4 (Obsolete)	-
3	Revision 1.3 (for MMC V4.3)	-
2	Revision 1.2 (for MMC V4.2)	-
1	Revision 1.1 (for MMC V4.1)	-
0	Revision 1.0 (for MMC V4.0)	-

NOTE:
1) Current eMMC standard defined by JEDEC supports up to 0x06 for EXT_CSD_REV value, 0x07 is additionally assigned to support e.MMC5.0 product. It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

[Table 6] High speed timing values (EXT_CSD register : HS_TIMING [185])

Value	Timing Interface	Supportability
0x0	Selecting backwards compatibility interface timing	Support
0x1	High Speed	Support
0x2	HS200	Support
0x3	HS400	Support

NOTE:

1) It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

5.0 Technical Notes

5.1 S/W Agorithm

5.1.1 Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

5.1.1.1 Boot Area Partition and RPMB Area Partition

Boot Partition size & RPMB Partition Size are set by the following command sequence :

[Table 7] Setting sequence of Boot Area Partition size and RPMB Area Partition size

Function	Command	Description
Partition Size Change Mode	CMD62(0xEFAC62EC)	Enter the Partition Size Change Mode
Partition Size Set Mode	CMD62(0x00CBAEA7)	Partition Size setting mode
Set Boot Partition Size	CMD62(BOOT_SIZE_MULT)	Boot Partition Size value
Set RPMB Partition Size	CMD62(RPMB_SIZE_MULT)	RPMB Partition Size value F/W Re-Partition is executed in this step.
Power Cycle		

Boot partition size is calculated as (128KB * BOOT_SIZE_MULT)
The size of Boot Area Partition 1 and 2 can not be set independently. It is set as same value.

RPMB partition size is calculated as (128KB * RPMB_SIZE_MULT).
In RPMB partition, CMD 0, 6, 8, 12, 13, 15, 18, 23, 25 are admitted.

Access Size of RPMB partition is defined as the below:

[Table 8] REL_WR_SEC_C value for write operation on RPMB partition

REL_WR_SEC_C	Description
REL_WR_SEC_C = 1	Access sizes 256B and 512B supported to RPMB partition
REL_WR_SEC_C > 1	Access sizes up to REL_WR_SEC_C * 512B supported to RPMB partition with 256B granularity

Any undefined set of parameters or sequence of commands results in failure access.

If the failure is in data programming case, the data is not programmed. And if the failure occurs in data read case, the read data is ‘0x00’.

5.1.1.2 Enhanced Partition (Area)

SAMSUNG e·MMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies double size of original set up size. (ex> if master set 1MB for enhanced mode, total 2MB user data area is needed to generate 1MB enhanced area)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes)

5.1.2 Boot operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

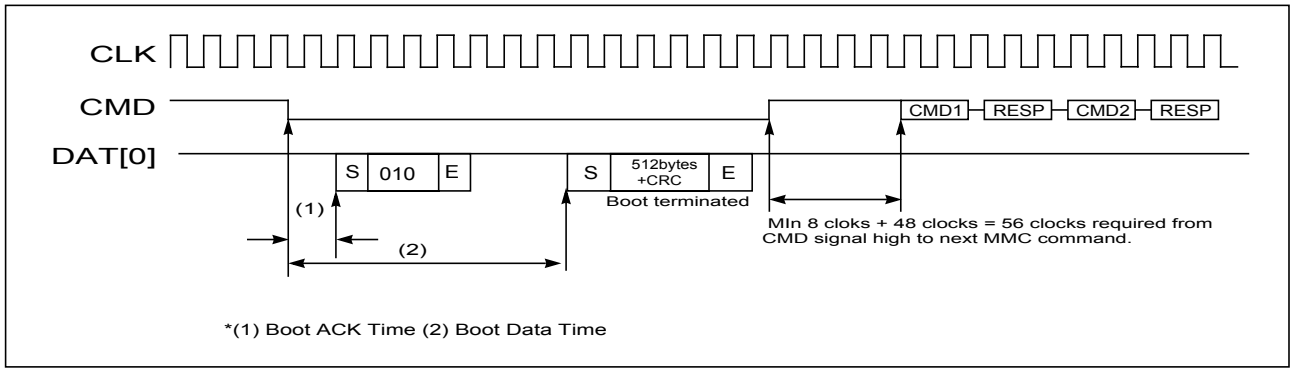


Figure 5. embedded MultiMediaCard state diagram (boot mode)

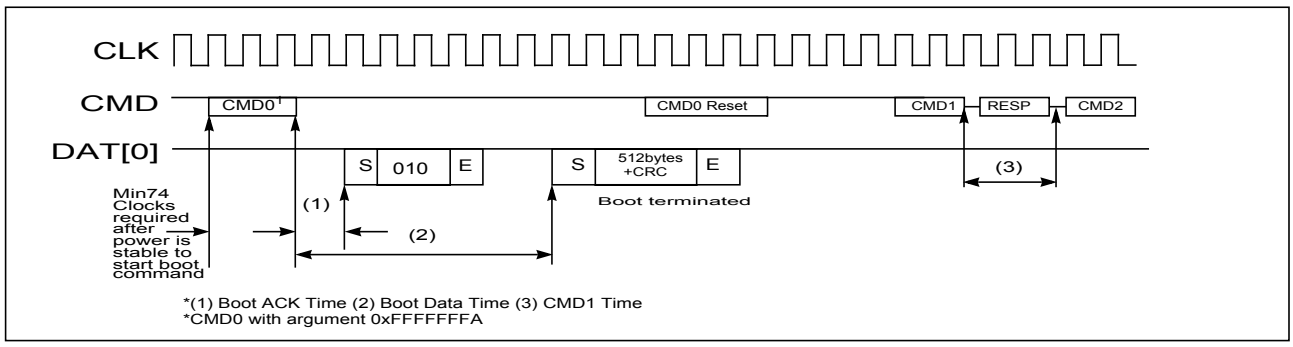


Figure 6. embedded MultiMediaCard state diagram (alternative boot mode)

[Table 9] Boot ack, boot data and initialization Time

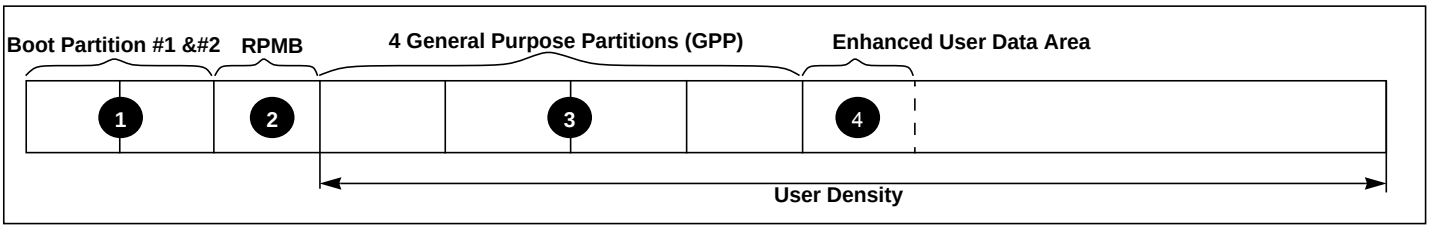
Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 100 ms
(3) Initialization Time[1)]	< 3 secs

NOTE:

1) This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 6.4 Extended CSD Register.
Normal initialization time (without partition setting) is completed within 1sec

5.1.3 User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 64MB in MLC.
This results in decreasing of user density



[Table 10] Capacity according to partition

Capacities	Value	Boot partition 1	Boot partition 2	RPMB
8GB	Default.	4,096KB	4,096KB	512KB
	Max.	4,096KB	4,096KB	4,096KB
16GB,32GB,64GB	Default.	4,096KB	4,096KB	4,096KB
	Max.	4,096KB	4,096KB	4,096KB

[Table 11] Maximum Enhanced Partition Size

Device	Max. Enhanced Partition Size
8 GB	3,909,091,328 Bytes
16 GB	7,809,794,048 Bytes
32 GB	15,627,976,704 Bytes
64 GB	31,264,342,016 Bytes

[Table 12] User Density Size

Device	User Density Size
8 GB	7,818,182,656 Bytes
16 GB	15,634,268,160 Bytes
32 GB	31,268,536,320 Bytes
64 GB	62,537,072,640 Bytes

5.1.4 Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.

At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion

[Table 13] Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

[Table 14] Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	OFF
GotoSleep Time	< 1ms	< 1ms

5.1.5 Performance

[Table 15] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
8 GB	175	18
16 GB	220	40
32 GB	250	50
64 GB		

* Test / Estimation Condition : Bus width x8, 200MHz DDR, 512KB data transfer, w/o file system overhead

6.0 REGISTER VALUE

6.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the e·MMC. In addition, this register includes a status information bit. This status bit is set if the e·MMC power up procedure has been finished. The OCR register shall be implemented by all e·MMCs.

[Table 16] OCR Register

OCR bit	VDD voltage window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) -[2GB] 10b (sector mode) -[*Higher than 2GB only]
[31]	e·MMC power up status bit (busy)[1]	

NOTE :
1) This bit is set to LOW if the e·MMC has not finished the power up routine
2) The voltage for internal flash memory(VDDF) should be 2.7-3.6v regardless of OCR Register value.

6.2 CID Register

[Table 17] CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	___[1]
Product name	PNM	48	[103:56]	See Product name table
Product revision	PRV	8	[55:48]	___[2]
Product serial number	PSN	32	[47:16]	___[3]
Manufacturing date	MDT	8	[15:8]	___[4]
CRC7 checksum	CRC	7	[7:1]	___[5]
not used, always '1'	-	1	[0:0]	---

NOTE :
1),4),5) description are same as e.MMC JEDEC standard
2) PRV is composed of the revision count of controller and the revision count of F/W patch
3) A 32 bits unsigned binary integer. (Random Number)

6.2.1 Product name table (In CID Register)

[Table 18] Product name table

Part Number	Density	Product Name in CID Register (PNM)
KLM8G1GEAC-B031	8 GB	0 x 4D3847314743
KLMAG2GEAC-B031	16 GB	0 x 4D4147324743
KLMBG4GEAC-B031	32 GB	0 x 4D4247344743
KLMCG8GEAC-B031	64 GB	0 x 4D4347384743

6.3 CSD Register

The Card-Specific Data register provides information on how to access the e·MMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:
R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 19] CSD Register

Name	Field	Width	Cell Type	CSD-slice	CSD Value			
					8GB	16GB	32GB	64GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03			
System specification version	SPEC_VERS	4	R	[125:122]	0x04			
Reserved	-	2	R	[121:120]	-			
Data read access-time 1	TAAC	8	R	[119:112]	0x27			
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01			
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32			
Device command classes	CCC	12	R	[95:84]	0xF5			
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09			
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00			
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00			
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00			
DSR implemented	DSR_IMP	1	R	[76:76]	0x00			
Reserved	-	2	R	[75:74]	-			
Device size	C_SIZE	12	R	[73:62]	0xFFF			
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x06			
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x06			
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x06			
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x06			
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07			
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F			
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F			
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F			
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01			
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00			
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x03			
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09			
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00			
Reserved	-	4	R	[20:17]	-			
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00			
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00			
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01			
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00			
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00			
File format	FILE_FORMAT	2	R/W	[11:10]	0x00			
ECC code	ECC	2	R/W/E	[9:8]	0x00			
CRC	CRC	7	R/W/E	[7:1]	-			
Not used, always'1'	-	1	—	[0:0]	-			

6.4 Extended CSD Register

The Extended CSD register defines the e·MMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the e·MMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e·MMC is working in. These modes can be changed by the host by means of the SWITCH command.
R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable

[Table 20] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value			
					8GB	16GB	32GB	64GB
Properties Segment								
Reserved[1]		6	-	[511:506]	-			
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00			
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01			
HPI features	HPI_FEATURES	1	R	[503]	0x01			
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01			
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F			
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F			
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x01			
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x04			
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x00			
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05			
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07			
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03			
Supported modes	SUPPORTED_MODES	1	R	[493]	0x01			
FFU features	FFU_FEATURES	1	R	[492]	0x00			
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00			
FFU Argument	FFU_ARG	4	R	[490:487]	0x00			
Reserved[1]		181	-	[486:306]	-			
Number of received sectors	NUMBER_OF_RECEIVED_SECTORS	4	R	[305:302]	0x00			
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0x00			
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x01			
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x01			
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01			
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x00			
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x08	0x10	0x20	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01			
Device version	DEVICE_VERSION	2	R	[263:262]	0x00			
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	FW Patch Ver.			
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00			
Cache size	CACHE_SIZE	4	R	[252:249]	0x00010000			
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A			

Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C			
Background operations status	BKOPS_STATUS	1	R	[246]	0x00			
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00			
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E			
Reserved[1]		1	-	[240]	-			
Power class for 52MHz, DDR at Vcc = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00			
Power class for 52MHz, DDR at Vcc = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00			
Power class for 200MHz at Vccq = 1.95V, Vcc = 3.6V	PWR_CL_200_195	1	R	[237]	0x00			
Power class for 200MHz, at Vccq = 1.3V, Vcc = 3.6V	PWR_CL_200_130	1	R	[236]	0x00			
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00			
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00			
Reserved[1]		1	-	[233]	-			
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02			
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55			
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B			
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11			
Boot information	BOOT_INFO	1	R	[228]	0x07			
Reserved[1]		1	-	[227]	-			
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20			
Access size	ACC_SIZE	1	R	[225]	0x07			
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01			
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x01			
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01			
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10			
Sleep current (VCC)	S_C_VCC	1	R	[220]	0x07			
Sleep current (VCCQ)	S_C_VCCQ	1	R	[219]	0x07			
Product state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x00			
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11			
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x07			
Sector Count	SEC_COUNT	4	R	[215:212]	0xE90000	0x1D1F000	0x3A3E000	0x747C000
Reserved[1]		1	-	[211]	-			
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00			
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00			
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00			
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00			
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00			
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00			
Reserved[1]		1	-	[204]	-			

Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x00
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x05
I/O Driver Strength CSD structure version	DRIVER_STRENGTH	1	R	[197]	0x1F
Device type	DEVICE_TYPE	1	R	[196]	0x57
Reserved[1]		1	-	[195]	-
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved[1]		1	-	[193]	-
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x07
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved[1]		1	-	[190]	-
Command set revision	CMD_SET_REV	1	R	[189]	0x00
Reserved[1]		1	-	[188]	-
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved[1]		1	-	[186]	-
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Reserved[1]		1	-	[184]	-
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved[1]		1	-	[182]	-
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved[1]		1	-	[180]	-
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00
Reserved[1]		1	-	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00
Reserved[1]		1	-	[172]	-
User area write protection register	USER_WP	1	R/W, R/W/C_P &R/W/E_P	[171]	0x00
Reserved[1]		1	-	[170]	-
FW configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x04 | 0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x04
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00

HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00			
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x07			
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x1D2	0x3A3	0x747	0xE8F
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00			
Partitioning Setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0x00			
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00			
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00			
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00			
Reserved[1]		1	-	[135]	-			
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00			
Production state awareness	PRODUCTION_STATE_ AWARENESS	1	R/W/E	[133]	0x00			
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00			
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00			
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x01			
Reserved[1]		64	-	[129:66]	-			
Optimized Features	OPTIMIZED_FEATURES	2	R	[65:64]	0x0F			
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00			
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00			
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00			
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00			
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00			
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x00			
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00			
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00			
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00			
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00			
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00			
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00			
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00			
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00			
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00			
Reserved[1]		1	-	[31]	-			
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00			
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00			
Reserved[1]		2	-	[28:27]	-			
FFU status	FFU_STATUS	1	R	[26]	0x00			
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00			
Max pre loading data size	MAX_PRE_LOADING_DATA_ SIZE	4	R	[21:18]	0x00			
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x00			
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x09			
Reserved[1]		16	-	[15:0]	-			

NOTE : 1) Reserved bits should read as “0.”

7.0 AC PARAMETER

7.1 Timing Parameter

[Table 21] Timing Parameter

Timing Paramter		Max. Value	Unit
Initialization Time (tINIT)	Normal 1)	1	s
	After partition setting 2)	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		20	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout		600	ms
Partition Switching Timeout (after Init)		1	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms

NOTE:
1) Normal Initialization Time without partition setting
2) Initialization Time after partition setting, refer to INI_TIMEOUT_AP in 6.4 EXT_CSD register
3) Be advised Timeout Values specified in Table above are for testing purposes under Samsung test pattern only and actual timeout situations may vary
4) EXCEPTION_EVENT may occur and the actual timeout values may vary due to user environment

7.2 Previous Bus Timing Parameters for DDR52 and HS200 mode are defined by JEDEC standard

7.3 Bus Timing Specification in HS400 mode

7.3.1 HS400 Device Input Timing

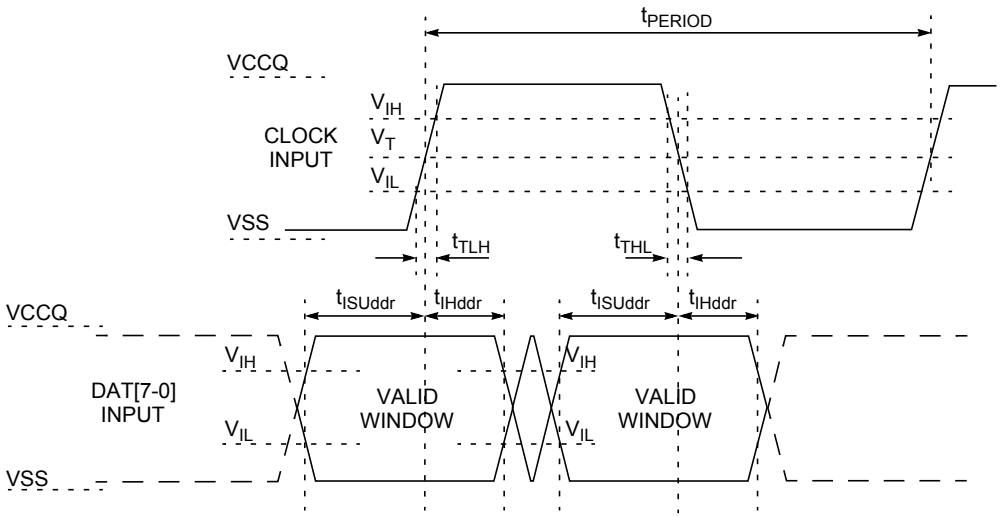


Figure 7. HS400 Device Input Timing

NOTE:
1) t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min).
2) V_{IH} denotes V_{IH}(min.) and V_{IL} denotes V_{IL}(max.)

[Table 22] HS400 Device input timing

Parameter	Symbol	Min	Max.	Unit
Input CLK				
Cycle time data transfer mode	t_{PERIOD}	5	-	ns
Clock rising / falling time	t_{TLH}, t_{THL}	-	0.1·t_{PERIOD} (=0.5)	ns
Clock duty cycle		46	54	%
Input DAT (referenced to CLK)				
Input set-up time	tISUddr	0.4		ns
Input hold time	tIHddr	0.4		ns

NOTE :
1) It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

7.3.2 HS400 Device Output Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode. The device output value of Data Strobe is “High-Z” when the device is not in outputting data(data read, CRC status response). Data Strobe is toggled only during data read period.

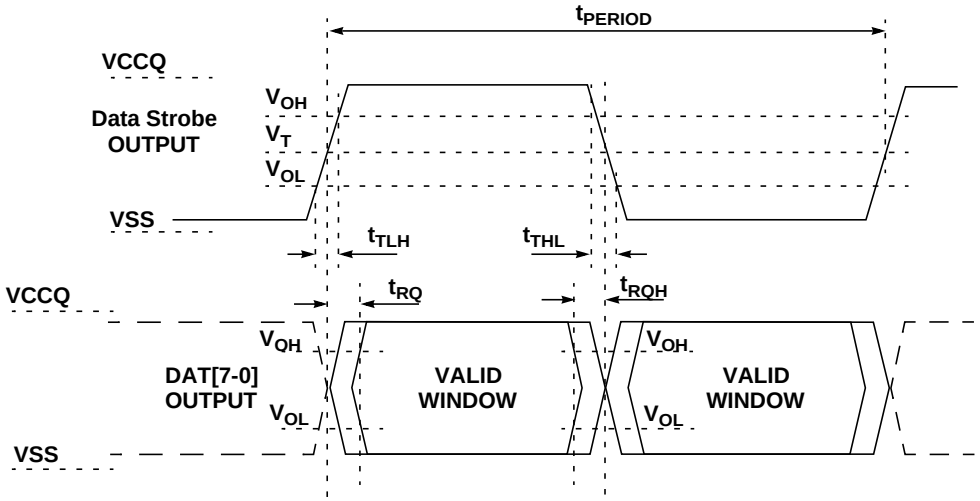


Figure 8. HS400 Device Output Timing

NOTE:
V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

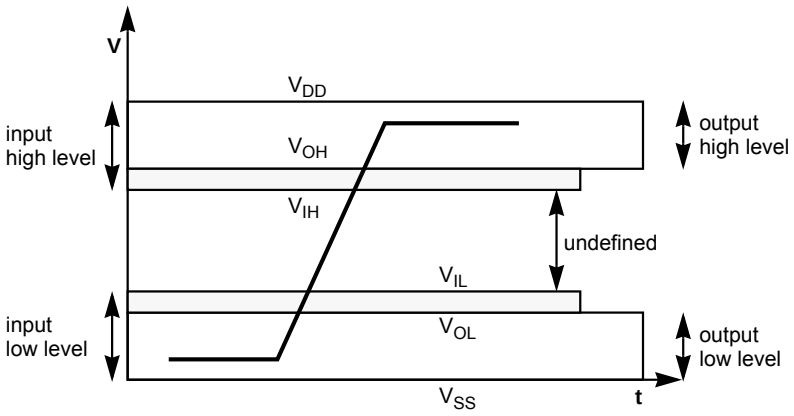
[Table 23] HS400 Device Output timing

Parameter	Symbol	Min	Max.	Unit
Output Data Strobe				
Cycle time data transfer mode	t_{PERIOD}	5	-	ns
Clock rising/falling time	t_{TLH}, t_{THL}	-	0.16·t_{PERIOD} (=0.8)	ns
Clock duty cycle		42	58	%
Output DAT (referenced to Data Strobe)				
Output hold skew	tRQ		0.4	ns
Output hold time	tRQH		0.4	ns

NOTE :
1) It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

7.4 Bus signal levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



7.4.1 Open-drain mode bus signal level

[Table 24] Open-drain bus signal level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.2	-	V	1)
Output LOW voltage	V_{OL}	-	0.3	V	I_{OL} = 2 mA

NOTE:
1) Because Voh depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min value.

7.4.2 Push-pull mode bus signal level eMMC

The device input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range

[Table 25] Push-pull signal level—high-voltage eMMC

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75*V_{CCQ}	-	V	I_{OH} = -100 uA@V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125*V_{CCQ}	V	I_{OL} = 100 uA@V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625*V_{CCQ}	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25*V_{CCQ}	V	-

[Table 26] Push-pull signal level—1.70 - 1.95 V_{CCQ} voltage Range

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45V	-	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	-	0.45V	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65*V_{CCQ} 1)	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{CCQ} 2)	V	-

NOTE:
1) 0.7*V_{CCQ} for MMC4.3 and older revisions.
2) 0.3*V_{CCQ} for MMC4.3 and older revisions.

8.0 DC PARAMETER

8.1 Active Power Consumption during operation

[Table 27] Active Power Consumption during operation

Density	NAND Type	CTRL	NAND	Unit
8 GB	64Gb MLC x 1	150	80	mA
16 GB	64Gb MLC x 2		130	
32 GB	64 Gb MLC x4		230	
64 GB	64Gb MLC x 8			

* Power Measurement conditions: Bus configuration =x8 @200MHz DDR
* The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

8.2 Standby Power Consumption in auto power saving mode and standby state.

[Table 28] Standby Power Consumption in auto power saving mode and standby state

Density	NAND Type	CTRL		NAND		Unit
		25°C(Typ)	85°C	25°C(Typ)	85°C	
8 GB	64Gb MLC x 1	120	400	40	85	uA
16 GB	64Gb MLC x 2			50	135	
32 GB	64 Gb MLC x4			70	235	
64 GB	64Gb MLC x 8			130	435	

NOTE:
Power Measurement conditions: Bus configuration =x8, No CLK
*Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.

8.3 Sleep Power Consumption in Sleep State

[Table 29] Sleep Power Consumption in Sleep State

Density	NAND Type	CTRL		NAND	Unit
		25°C(Typ)	85°C		
8 GB	64Gb MLC x 1	120	400	0[1)]	uA
16 GB	64Gb MLC x 2				
32 GB	64 Gb MLC x4				
64 GB	64Gb MLC x 8				

NOTE:
Power Measurement conditions: Bus configuration =x8, No CLK
1) In auto power saving mode , NAND power can not be turned off .However in sleep mode NAND power can be turned off. If NAND power is alive , NAND power is same with that of the Standby state.

8.4 Supply Voltage

[Table 30] Supply voltage

Item	Min	Max	Unit
V_{DD} (V_{CCQ})	1.70 (2.7)	1.95 (3.6)	V
V_{DDF} (V_{CC})	2.7	3.6	V
V_{SS}	-0.5	0.5	V

8.5 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the e·MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 31] Bus SIgnal Line Load

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			12	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

[Table 32] Capacitance and Resistance for HS400 mode

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	CL			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	