| REFERENCE SPECIFICATIONS | |
|---|---|
| **Product Name** | **8.9"WQXGA** |

**Approval Signature**

Accepted by: _____

Date: _____

Proposed by: _____

Japan Display Inc.

# RECORD OF REVISIONS

| Date | Sheet No. | Summary |
|---|---|---|
| | | Initial release (Ver01) |
| | | |

## 3. GENERAL DATA

3.1 LCM

| | | |
|---|---|---|
| (1) | Part Name | 8.9"WQXGA |
| (2) | Module Dimensions | 200.9 (H) mm × 132.1 (V) mm × 1.82 (t) mm<br>(Excluding I/F-FPC and electronic components) |
| (3) | Active Area Dimensions | 192.0 (H) mm × 120.0 (V) mm |
| (4) | Pixel Pitch | 0.075 (H) mm × 0.075 (V) mm |
| (5) | Resolution | 2560 × 3 (R,G,B) (H) × 1600 (V) dots |
| (6) | Color Pixel Arrangement | RGB Vertical Stripe |
| (7) | Display Mode | Transmissive Type, Normally Black Mode, In-Plane Switching Mode |
| (8) | Number of Colors | 16,777,216 Colors |
| (9) | Viewing Direction | - |
| (10) | Backlight | Light Emitting Diode (LED), 36 LEDs in linear connection<br>Backlight current : 20mA / LED (typ) |
| (11) | Weight | 78g (typ) |
| (12) | Power Supply Voltage | VBAT = 3.3V |
| (13) | Interface I/O power supply | VDDIO = 1.8V<br>The same voltage as "H" level of a customer's interface signal must be supplied to VDDIO. |
| (14) | LCD Driver IC | R69429 x2pcs (Renesas SP drivers Inc.) |
| (15) | Interface | MIPI-DSI Command/Video mode (4Lane x 2Port) |
| (16) | Method of Inversion | Column Inversion |
| (17) | Surface Treatment | Hard coat |

## 4. ABSOLUTE MAXIMUM RATINGS

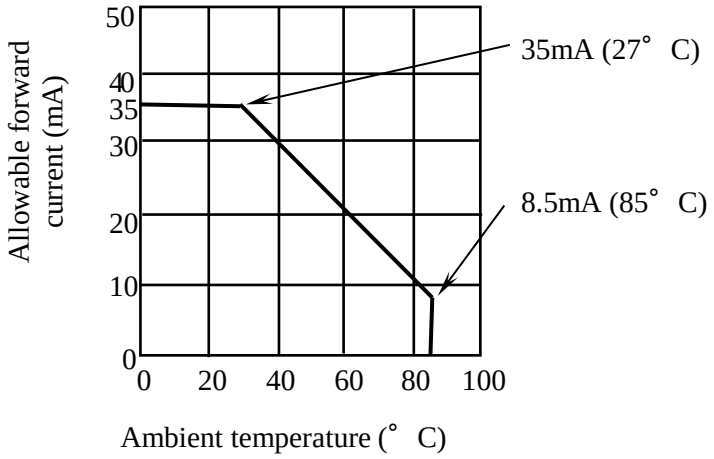
4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD GND=0 V, Ta=25°C

| Item | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Power Supply for Interface | VDDIO | −0.3 | 4.6 | V | (1) |
| Power Supply for DC/DC converter | VBAT | −0.3 | | V | (1) |
| Input Voltage | Vi | −0.3 | VDDIO+0.3 | V | (2) |
| LED Reverse Voltage | $V_R$ | - | 5 | V | |
| LED Forward Current | $I_{LED}$ | - | Note (3) | mA | per LED |
| Static Electricity | - | - | ±2 | kV | (4) |

Notes (1) Keep all Voltages no lower than GND.

(2) Applies to the RESET pin.

(3) Ambient Temperatures vs. Allow able Forward Current.



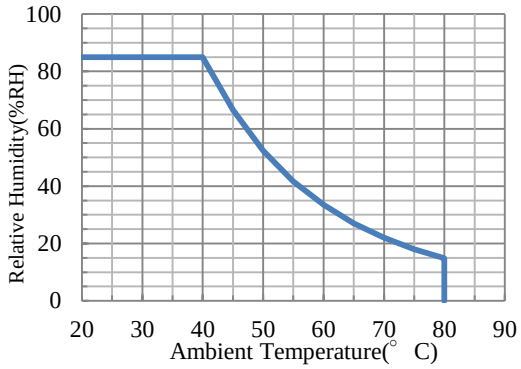

(4) 100 pF - 1.5 kohm, 25°C-70%RH

Static electricity discharge is to be aimed at the center of the active area.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

| Item | Operating | | Non-Operating Note(3) | | Remarks |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Ambient Temperature | -20°C | 60°C | -20°C | 65°C | Note (2) |
| Humidity | Note (1) | | Note (1) | | No condensation |
| Corrosive Gas | Not Acceptable | | Not Acceptable | | |

Notes (1) Ta ≤ 40°C 85%RH max.
Ta > 40°C Absolute humidity must be lower than the humidity of 85%RH at 40°C.
No dew condensation is allowed.




(2) Background color slightly changes depending on ambient temperature and viewing angle.
The temperature for operating in the table above apply to operation only.
Visual qualities, such as contrast ratio and response time, to be evaluated at Ta = 25°C Operating.

(3) This is not for storing condition. When storing LCM for long term, please follow the condition mentioned in "11.5 STORAGE".

## 5. ELECTRICAL CHARACTERISTICS

LCD Module GND=0V, Ta=25°C

| Item | Symbol | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Power Supply Voltage for Logic and Analog | VBAT | -<br>- | 3.0 | 3.3 | 4.5 | V | - |
| Power Supply Voltage for I/O Interface | VDDI | - | 1.7 | 1.8 | 1.9 | V | - |
| Input Voltage for Logic Circuits | Vi | "H" level | 0.70×VDDIO | - | VDDIO | V | (1),(2) |
| | | "L" level | 0 | - | 0.30×VDDIO | | |
| Input Voltage for EN | Vi | "H" level | 0.90×VDDIO | - | VDDIO | V | (1) |
| | | "L" level | 0 | - | 0.10×VDDIO | | |
| Output Voltage for Logic Circuits | Vo | "H" level | 0.80×VDDIO | - | - | V | (1),(2) |
| | | "L" level | - | - | 0.20×VDDIO | | |
| Power Consumption | POWER | All White | - | (230) | | mW | (3),(4) |

Notes (1) VDDIO = 1.7V to 1.9V
(2) Input : RESET, DBIST
Output : PWM, TE
(3) VDDIO=1.7V～1.9V, VBAT=3V～4.5V, Column inversion mode.
Display image : ALL White
(4) Operation Mode : MIPI-DSI Command mode, LCM Display frame rate = 60.37～66.72fps
MIPI-DSI Data and Clock lane = LP11

## 6. OPTICAL CHARACTERISTICS

LCD (BACKLIGHT ON)

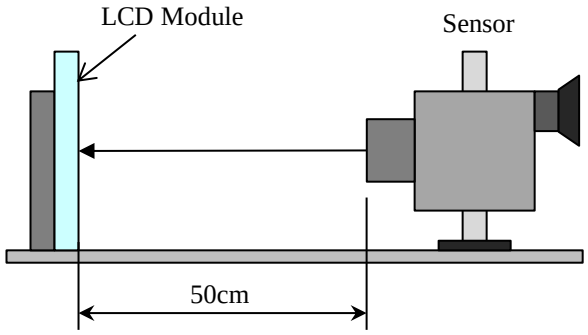
| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Brightness | B | φ=0°, θ=0° | | (500) | - | $cd/m^2$ | (1),(2) |
| Contrast Ratio | CR | φ=0°, θ=0° | | (1200) | - | - | (3) |

Measurement Conditions

Measurement environment : Dark room
Ambient temperature : Ta=25°C
Sequence : Refer to Item 8.5.2
Power supply voltage : VDDIO=1.8V, VBAT=3.3V
Backlight current : $I_{LED}$=20mA

Notes (1) Definition of Brightness "B"

(2) Display image for measurement : All White

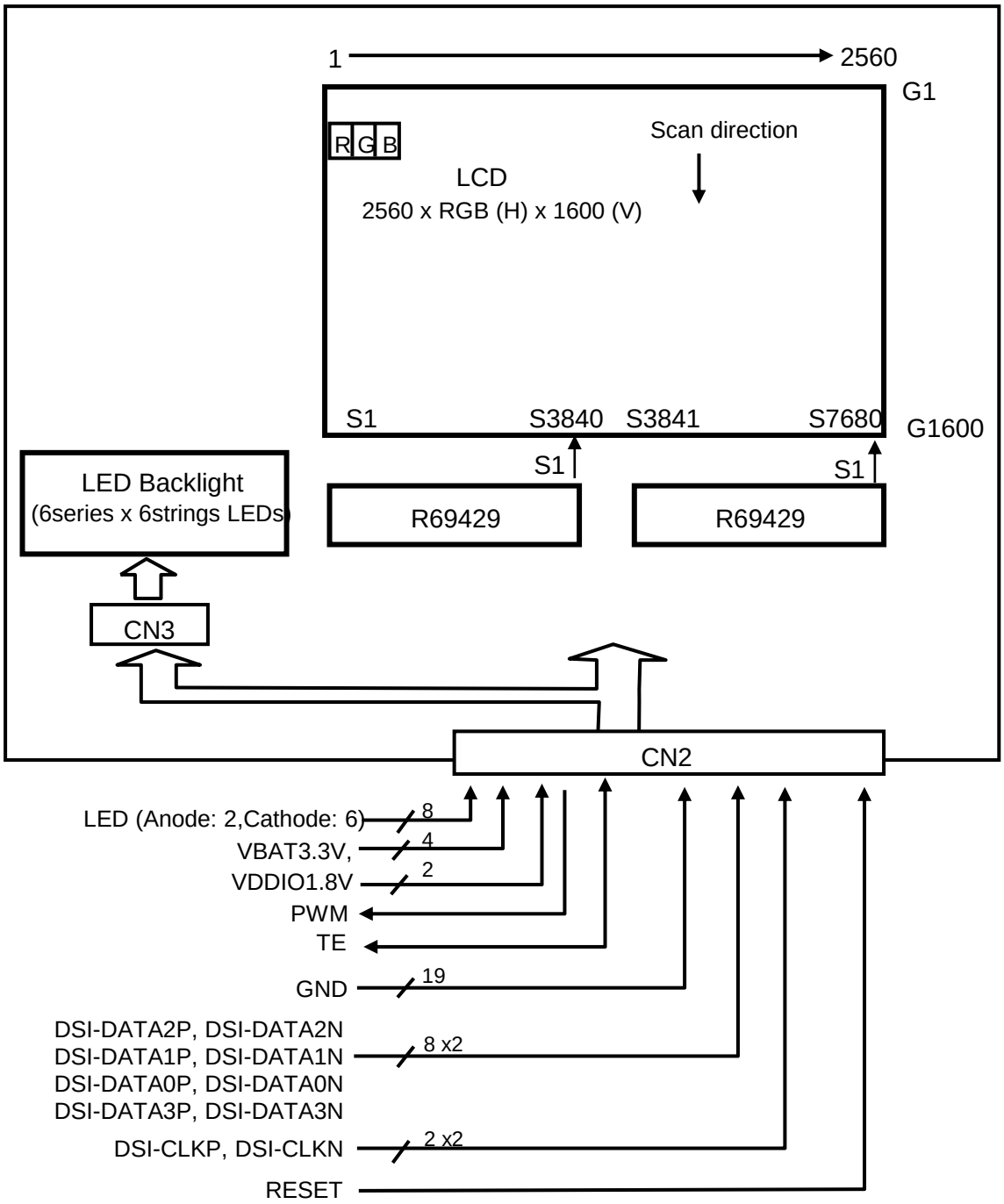


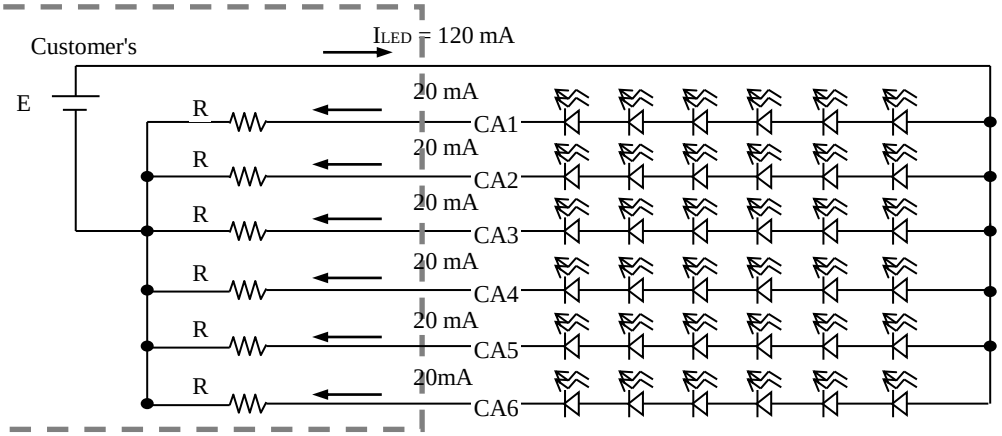

Sensor : KONICA MINOLTA CS-1000 or equivalent
Measurement point: Center of LCD's active area

(3) Definition of Contrast "CR"

$$CR = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

## 7. BLOCK DIAGRAM




| | | | | | | |
|---|---|---|---|---|---|---|
| Japan Display Inc. | | | Sh. No. | | Page | 7-1/1 |

## 8. INTERFACE

### 8.1 INTERNAL PIN CONNECTION

| Pin No. | Signal | I/O | Function | Driver's Signal name |
|---|---|---|---|---|
| 1 | GND | - | GND | - |
| 2 | GND | - | GND | - |
| 3 | GND | - | GND | - |
| 4 | V_LED_C6 | - | GND for LED | - |
| 5 | V_LED_C5 | - | GND for LED | - |
| 6 | V_LED_C4 | - | GND for LED | - |
| 7 | V_LED_C3 | - | GND for LED | - |
| 8 | V_LED_C2 | - | GND for LED | - |
| 9 | V_LED_C1 | - | GND for LED | - |
| 10 | V_LED_A | - | Power Supply for LED | - |
| 11 | V_LED_A | - | Power Supply for LED | - |
| 12 | N.C | - | Non connect | - |
| 13 | GND | - | GND | - |
| 14 | PWM | O | Control Signal for LED Brightness | LEDPWM |
| 15 | TE | O | Tearing Effect Output | TE |
| 16 | GND | - | GND | - |
| 17 | DSI_R-DATA-2P | I | Positive MIPI Data2 Input | DATA2P |
| 18 | DSI_R-DATA-2N | I | Negative MIPI Data2 Input | DATA2N |
| 19 | GND | - | GND | - |
| 20 | DSI_R-DATA-1P | I | Positive MIPI Data1 Input | DATA1P |
| 21 | DSI_R-DATA-1N | I | Negative MIPI Data1 Input | DATA1N |
| 22 | GND | - | GND | - |
| 23 | DSI-CLKP | I | Positive MIPI Clock Input | CLKP |
| 24 | DSI-CLKN | I | Negative MIPI Clock Input | CLKN |
| 25 | GND | - | GND | - |
| 26 | DSI_R-DATA-0P | I/O | Positive MIPI Data0 Input/Output | DATA0P |
| 27 | DSI_R-DATA-0N | I/O | Negative MIPI Data0 Input/Output | DATA0N |
| 28 | GND | - | GND | - |
| 29 | DSI_R-DATA-3P | I | Positive MIPI Data3 Input | DATA3P |
| 30 | DSI_R-DATA-3N | I | Negative MIPI Data3 Input | DATA3N |
| 31 | GND | - | GND | - |
| 32 | EN | I | Enable Pin to Operate DC/DC converter | - |

Continue to next page

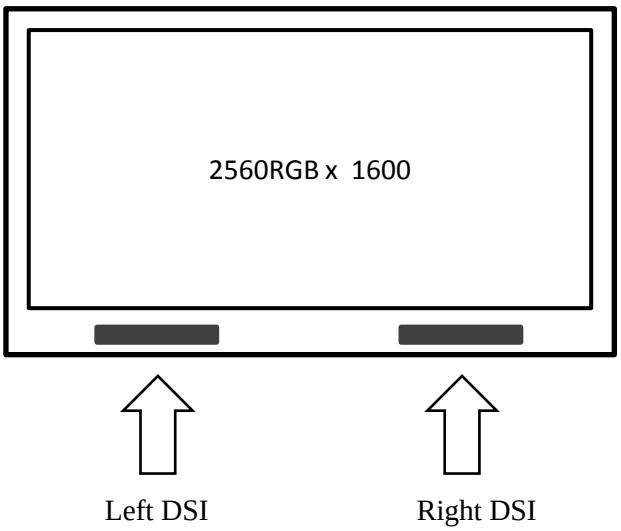
| Pin No. | Signal | I/O | Function | Driver's Signal name |
|---|---|---|---|---|
| 33 | N.C | - | Non connect | - |
| 34 | VBAT | - | Power Supply for DC/DC converter | - |
| 35 | VBAT | - | Power Supply for DC/DC converter | - |
| 36 | VBAT | - | Power Supply for DC/DC converter | - |
| 37 | VBAT | - | Power Supply for DC/DC converter | - |
| 38 | N.C | - | Non connect | - |
| 39 | VDDIO | - | Power Supply for I/O Interface and logic | - |
| 40 | VDDIO | - | Power Supply for I/O Interface and logic | - |
| 41 | GND | - | GND | - |
| 42 | DBIST(GND) | I | GND (Enable pin to Generate Self Reflesh Imag | DBIST |
| 43 | TE_S | O | Non connect (Test pin for LCD Module supplier) | - |
| 44 | GND | - | GND | - |
| 45 | RESET | I | Reset Signal | RESX |
| 46 | GND | - | GND | - |
| 47 | DSI_L-DATA-2P | I | Positive MIPI Data2 Input | DATA2P |
| 48 | DSI_L-DATA-2N | I | Negative MIPI Data2 Input | DATA2N |
| 49 | GND | - | GND | - |
| 50 | DSI_L-DATA-1P | I | Positive MIPI Data1 Input | DATA1P |
| 51 | DSI_L-DATA-1N | I | Negative MIPI Data1 Input | DATA1N |
| 52 | GND | - | GND | - |
| 53 | DSI-CLKP | I | Positive MIPI Clock Input | CLKP |
| 54 | DSI-CLKN | I | Negative MIPI Clock Input | CLKN |
| 55 | GND | - | GND | - |
| 56 | DSI_L-DATA-0P | I/O | Positive MIPI Data0 Input/Output | DATA0P |
| 57 | DSI_L-DATA-0N | I/O | Negative MIPI Data0 Input/Output | DATA0N |
| 58 | GND | - | GND | - |
| 59 | DSI_L-DATA-3P | I | Positive MIPI Data3 Input | DATA3P |
| 60 | DSI_L-DATA-3N | I | Negative MIPI Data3 Input | DATA3N |
| 61 | GND | - | GND | - |

LCM Connector :FH36W-61S-0.3SHW(50)(Header) (HIROSE)

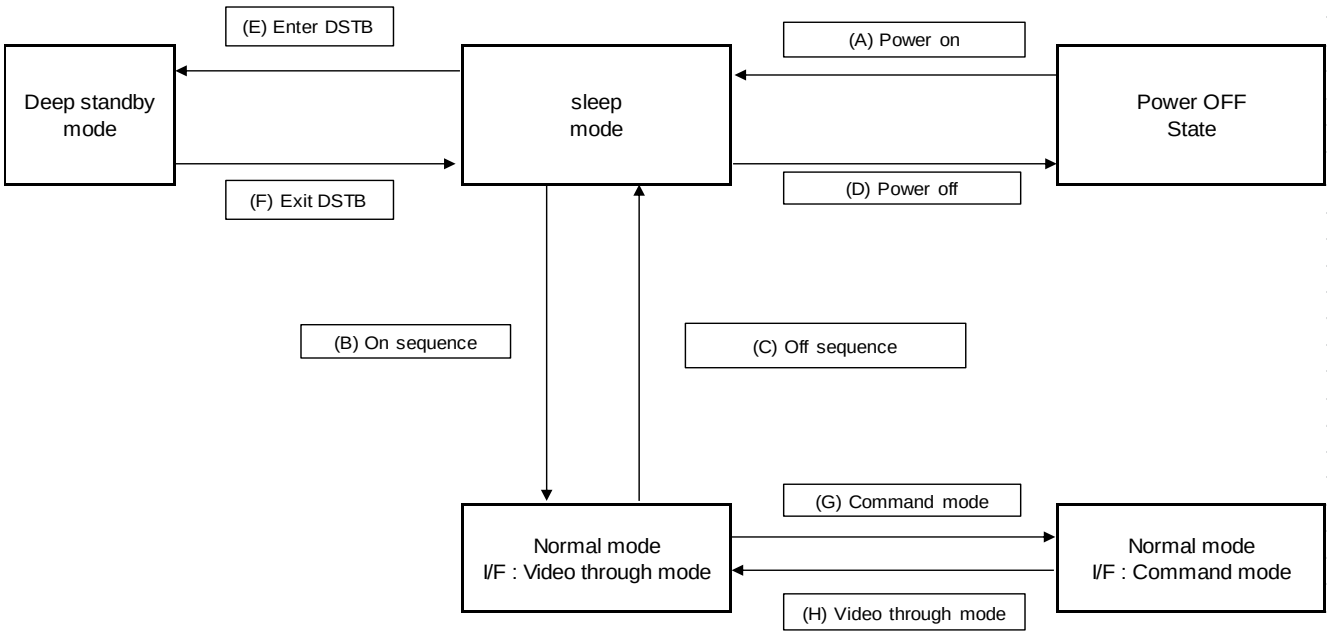
8.2 LCM Control sequence

8.2.1 LCM Circuit configuration

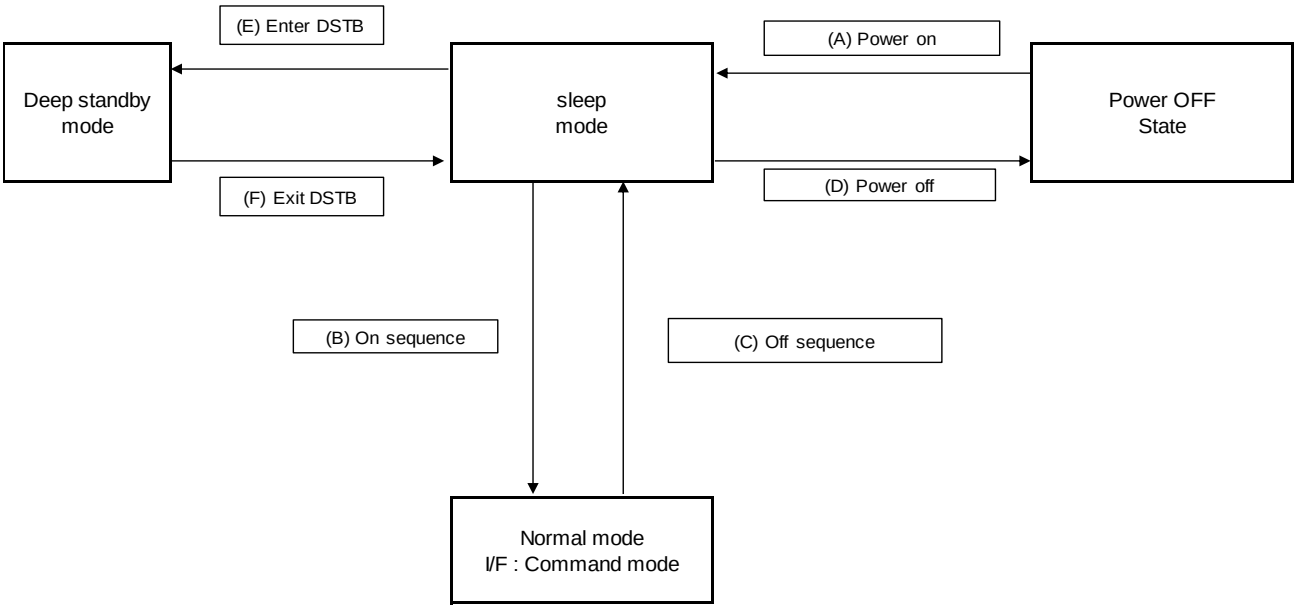
H:2560RGB x V:1600
R69429, 2Chip
w/RAM
Mipi-DSI 4lane x 2port
Power Supply : VDDIO=1.8v(typ), VBAT=3.3v(typ)
(The DCDC on flex generates R69429's VSP/VSN from VBAT.)




8.2.2 Video through mode and Command mode Status flow



8.2.3 Command mode Status flow



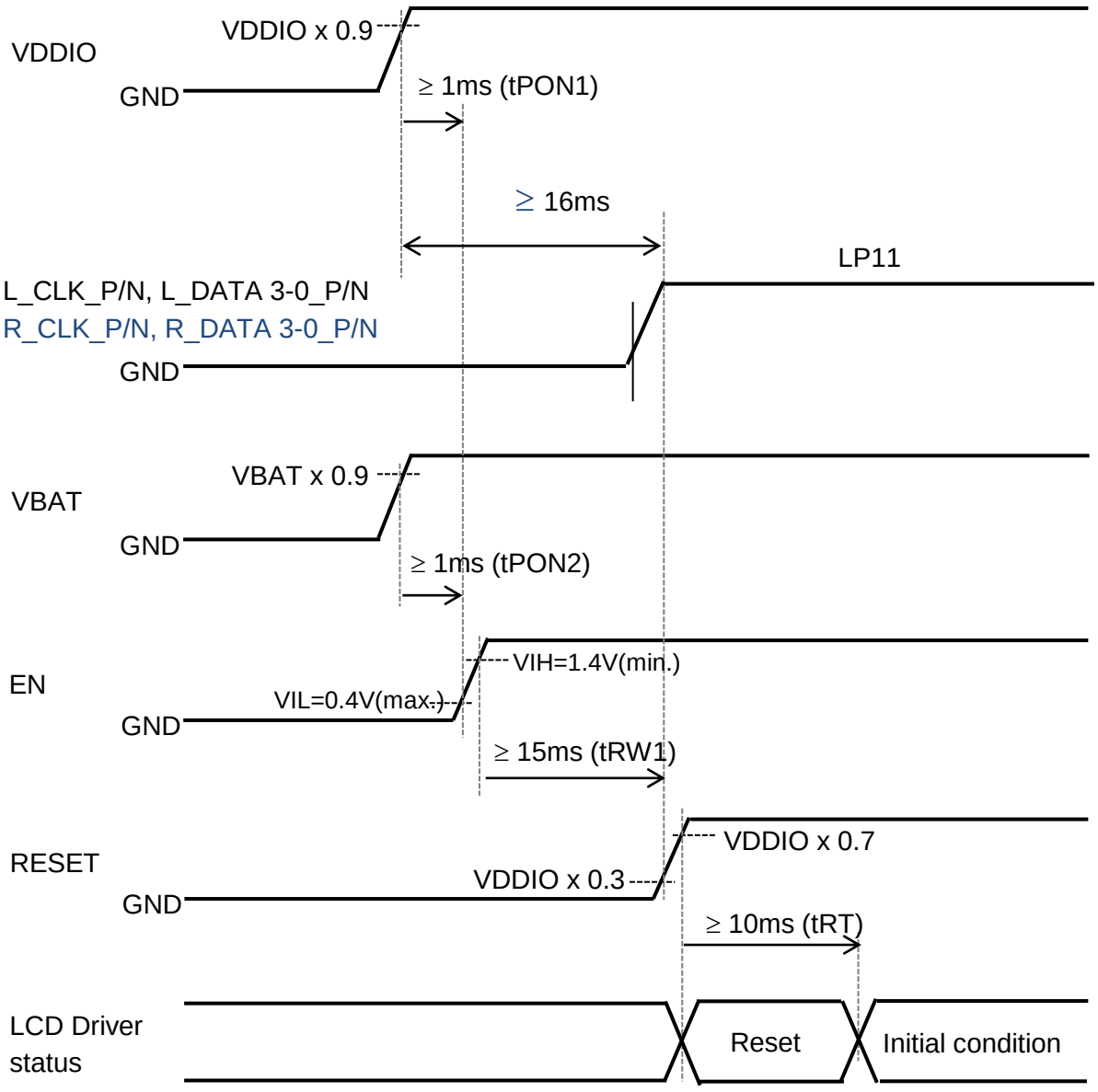
### 8.2.4 Power Supply Sequence

Note1) Make sure that the following relationship are satisfied : VDDIO ≥ RESET,
VDDIO ≥ MIPI-DSI signals.

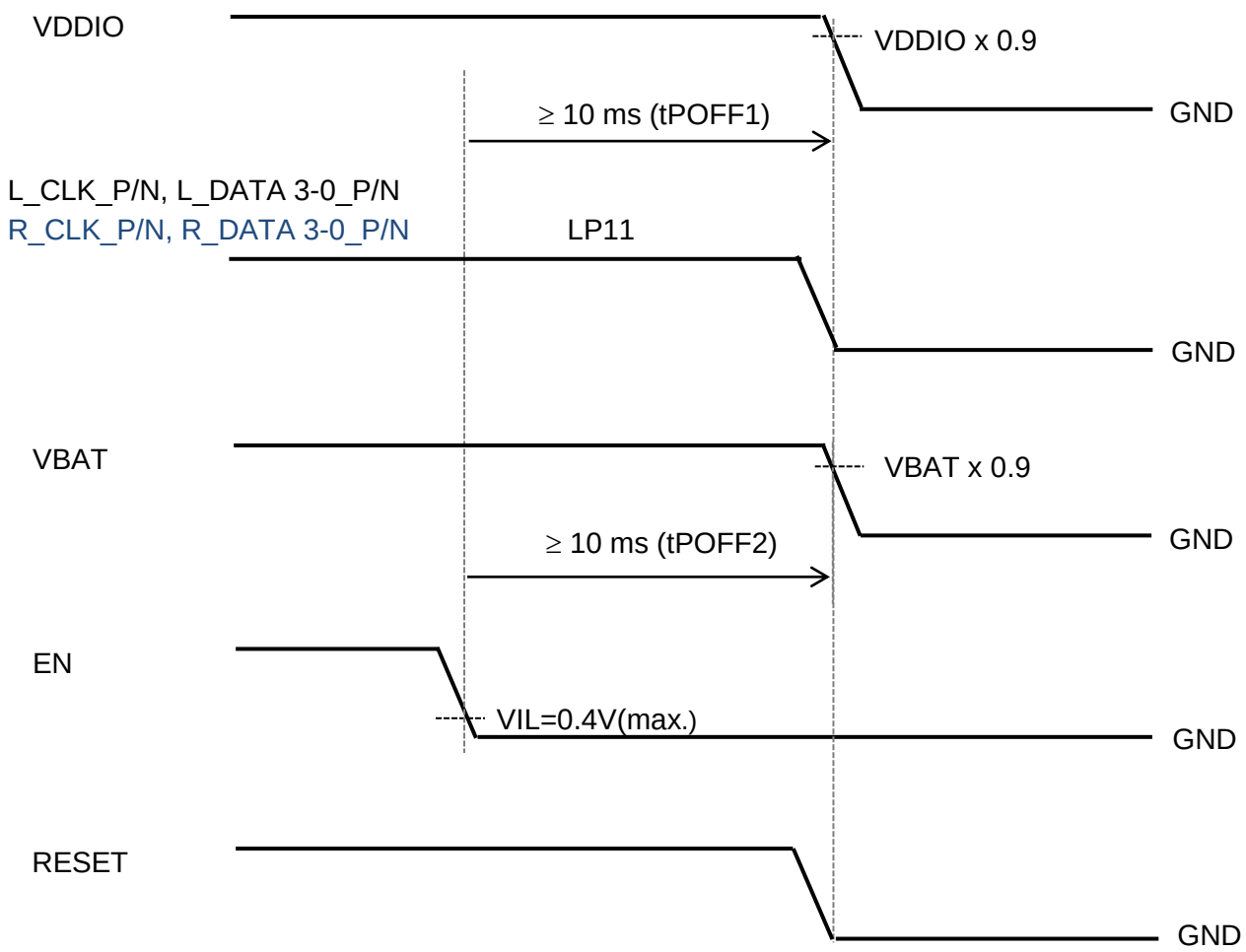
Note 2) Reset Timing Characteristics
(Power supply voltage and temperature range are ruled by the LCM delivery

| Item | Symbol | Unit | Test condition | Min. | Max. |
|---|---|---|---|---|---|
| VDDIO-EN delay time | tPON1 | ms | Power On | 1 | - |
| 3.3V-EN delay time | tPON2 | ms | Power On | 1 | - |
| Reset low-level width | tRW1 | ms | Power On | 15 | - |
| Reset time | tRT | ms | Power On | 10 | - |
| EN-VDDIO delay time | tPOFF1 | ms | Power Off | 10 | - |
| EN-3.3V delay time | tPOFF2 | ms | Power Off | 10 | - |

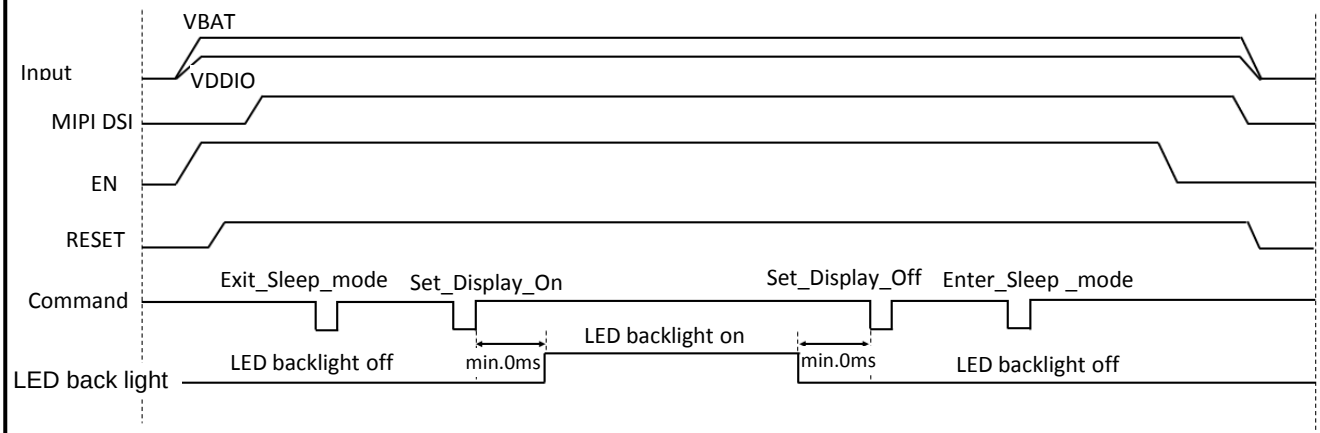
### 8.2.5 Power On sequence



8.2.6 Power Off sequence




. LED Power On/Off sequence



## 8.2.7 Video through mode and Command mode Sequence

**(A) Power on**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| POWER OFF STATE | | | | | | | |
| ↓ | | | | | | | |
| PWR supply on | | | | | | VDDIO, VBAT on | |
| wait 1ms | | | | | | | |
| EN L -> H | | | | | | VSP,VSN on | |
| wait 15ms | | | | | | | |
| RESET L->H | | | | | | RESET L->H | |
| wait 10ms | | | | | | | |
| (EN H -> L) | | | | | | VSP,VSN off | (*1)Can skip "VSP/VSN off" in case of going to normal mode without staying sleep status. |
| (wait 10ms) | | | | | | | |
| ↓ | | | | | | | |
| SLEEP MODE | | | | | | | |

**(B) On sequence**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| SLEEP MODE | | | | | | | |
| ↓ | | | | | | | |
| EN L -> H | | | | | | VSP,VSN on | (*1) |
| wait 20ms | | | | | | | (*1) |
| | | | | | | | |
| command | 05 | 01 | - | - | L/R | soft reset | |
| wait 5ms | | | | | | | |
| | | | | | | | |
| command | 15 | 3A | 1 | 77 | L/R | set pixel format | |
| command | 39 | 2A | 1 | 00 | L/R | set column address | |
| | | | 2 | 00 | | | |
| | | | 3 | 04 | | | |
| | | | 4 | FF | | | |
| command | 39 | 2B | 1 | 00 | L/R | set page address | |
| | | | 2 | 00 | | | |
| | | | 3 | 06 | | | |
| | | | 4 | 3F | | | |
| | | | | | | | |
| command | 15 | 35 | 1 | 00 | R | set tear on | Recommend monitering TE timing due to the restriction in 2chip system, for details, refer "Restriction on command timing" |
| command | 39 | 44 | 1 | 00 | R | set tear scanline | |
| | | | 2 | 00 | | | |
| command | 15 | 51 | 1 | FF | L/R | write_display_brightness | |
| command | 15 | 53 | 1 | 24 | L/R | write_control_display | |
| command | 15 | 55 | 1 | 00 | L/R | write_adaptive_brightness_control<br>C[1:0] = 0x00 : ACO・CABC Off | Please use Auto Contrast Optimization ( ACO ) function and<br>Content Adaptive Brightness Control ( CABC ) function<br>by C[1:0] register, changing. |
| | | | 1 | 01 | L/R | write_adaptive_brightness_control<br>C[1:0] = 0x01 : ACO On | |
| | | | 1 | 02 | L/R | write_adaptive_brightness_control<br>C[1:0] = 0x02 : CABC On Max. Backlight reduction ratio : -33% setting | |
| | | | 1 | 03 | L/R | write_adaptive_brightness_control<br>C[1:0] = 0x03 : CABC On Max. Backlight reduction ratio : -54% setting | |
| command | 05 | 11 | - | - | L/R | exit sleep mode | |
| wait 120ms | | | | | | | |
| command | 23 | B0 | 1 | 00 | L/R | MCAP | This command is inputted for change of LEDPWM clock frequency.<br>When using [ C[1:0] = 0x00 : ACO・CABC Off ] and<br>[ C[1:0] = 0x01 : ACO On ] , it is not necessary to input this command. |
| command | 29 | CE | 1 | 7D | L/R | Back Light Control 4 | (1)This command is inputted for change of LEDPWM clock frequency.<br>When using [ C[1:0] = 0x00 : ACO・CABC Off ] and<br>[ C[1:0] = 0x01 : ACO On ] , it is not necessary to input this command.<br><br>(2)Please optimize a LEDPWM clock frequency by PWMDIV [7:0]<br>and PWM_CYCLE[7:0]<br>according to the characteristic of the LED driver used in your company. |
| | | | 2 | 40 | | | |
| | | | 3 | 48 | | | |
| | | | 4 | 56 | | | |
| | | | 5 | 67 | | | |
| | | | 6 | 78 | | | |
| | | | 7 | 88 | | | |
| | | | 8 | 98 | | | |
| | | | 9 | A7 | | | |
| | | | 10 | B5 | | | |
| | | | 11 | C3 | | | |
| | | | 12 | D1 | | | |
| | | | 13 | DE | | | |
| | | | 14 | E9 | | | |
| | | | 15 | F2 | | | |
| | | | 16 | FA | | | |
| | | | 17 | FF | | | |
| | | | 18 | 04 | | PWM_DIV[7:0] | |
| | | | 19 | 00 | | PWM_CYCLE[7:0] | |
| Transferring video mode packets (> 1 frame)<br>Note ) it is necessary to input DSICLK / VSYNC packet / HSYNC packet, before setting B3h register. | | | | | | | |
| command | 23 | B0 | 1 | 00 | L/R | MCAP | |
| command | 29 | B3 | 1 | 14 | L/R | Interface setting | Video through mode setting |
| command | 23 | B0 | 1 | 03 | L/R | MCAP | |
| command | 05 | 29 | - | - | L/R | set display on | |
| ↓ | | | | | | | |
| NORMAL MODE, I/F : Video through mode | | | | | | | |

# LCM Control Sequence (Continued)

(1)These CABC setting values are our proposal values.
It optimizes based on the evaluation result of your company.

CABC On -33% : Max. Backlight power reduction rate -33% setting
CABC On -54% : Max. Backlight power reduction rate -54% setting

(2)LEDPWM frequency calculation formula
LEDPWM frequency = fOSC2 / ( PWMDIV + 1 ) / ( PWM_CYCLE + 255 )
fOSC2 spec. = 26.6MHz(min.) - 28MHz(typ.) - 29.4MHz(max.)

(3)LEDPWM frequency default setting :
Command 0xCE, PWMDIV[7:0]=0x04, PWM_CYCLE[7:0]=0x00
LEDPWM frequency = 28MHz (typ.) / (4+1) / (0+255) = 21.961kHz(typ.)

**(c) Off sequence**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| NORMAL MODE, I/F : Video through mode | | | | | | | |
| ⇩ | | | | | | | |
| command | 05 | 28 | - | - | L/R | set display off | |
| wait 20ms | | | | | | | |
| command | 05 | 10 | - | - | L/R | enter sleep mode | |
| wait 80ms | | | | | | | |
| EN H -> L | | | | | | VSP,VSN off | |
| wait 10ms | | | | | | | |
| ⇩ | | | | | | | |
| SLEEP MODE | | | | | | | |

**(D) Power off**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| SLEEP MODE | | | | | | | |
| ⇩ | | | | | | | |
| RESET H->L | | | | | | | |
| PWR supply off | | | | | | VDDIO, VBAT off | |
| ⇩ | | | | | | | |
| POWER OFF STATE | | | | | | | |

**(E) Enter DSTB**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| SLEEP MODE | | | | | | | |
| ⇩ | | | | | | | |
| command | 23 | B0 | 1 | 00 | L/R | MCAP | |
| command | 23 | B1 | 1 | 01 | L/R | DSTB=1 | |
| ⇩ | | | | | | | |
| DSTB MODE | | | | | | | |

**(F) Exit DSTB**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| DSTB MODE | | | | | | | |
| ⇩ | | | | | | | |
| RESET H -> L | | | | | | | |
| wait 10ms | | | | | | | |
| EN L -> H | | | | | | VSP,VSN on | |
| wait 20ms | | | | | | | |
| RESET L->H | | | | | | RESET L->H | |
| wait 10ms | | | | | | | |
| (EN H -> L) | | | | | | VSP,VSN off | (*1)Can skip "VSP/VSN off" in case of going to normal mode without staying sleep status. |
| (wait 10ms) | | | | | | | |
| ⇩ | | | | | | | |
| SLEEP MODE | | | | | | | |

# LCM Control sequence (Continued)

**(G) Command mode**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| NORMAL MODE, I/F : Video through mode | | | | | | | |
| ⇩ | | | | | | | |
| Triggered by detecting TE="High" Note ) Command input in blank period | | | | | | | |
| command | 23 | B0 | 1 | 00 | L/R | MCAP | |
| command | 29 | B3 | 1 | 0C | L/R | Interface setting | Video capture mode setting |
| command | 23 | B0 | 1 | 03 | L/R | MCAP | |
| Transferring video mode packets (> 1 frame) Note ) it is necessary to input DSICLK / VSYNC packet / HSYNC packet, until 1frame period after setting B3h regisiter. | | | | | | | |
| ⇩ | | | | | | | |
| NORMAL MODE, I/F : Command mode | | | | | | | |
| Transferring command mode packets | | | | | | | |
| send image | 39 | 2C/3C | | | L/R | write memory / write memory continue | |

**(H) Video through mode**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| NORMAL MODE, I/F : Command mode | | | | | | | |
| ⇩ | | | | | | | |
| Transferring video mode packets Note ) it is necessary to input DSICLK / VSYNC packet / HSYNC packet, before setting B3h register. | | | | | | | |
| Triggered by detecting TE="High" Note ) Command input in blank period | | | | | | | |
| command | 23 | B0 | 1 | 00 | L/R | MCAP | |
| command | 29 | B3 | 1 | 1C | L/R | Interface setting | Video through mode setting |
| command | 23 | B0 | 1 | 03 | L/R | MCAP | |
| Transferring video mode packets (> 1 frame) | | | | | | | |
| ⇩ | | | | | | | |
| NORMAL MODE, I/F : Video through mode | | | | | | | |

**MP (J1) ID Code**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| command | 06 | A1 | 1 | 28 | Right | read_DDB_start | |
| | | | 2 | 0A | | | |
| | | | 3 | MP Production year and week code | | | |

**MP (D1) ID Code**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| command | 06 | A1 | 1 | 29 | Right | read_DDB_start | |
| | | | 2 | 0A | | | |
| | | | 3 | MP Production year and week code | | | |

## 8.2.8 Command mode Sequence

**(A) Power on**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| POWER OFF STATE | | | | | | | |
| ↓ | | | | | | | |
| PWR supply on | | | | | | VDDIO, VBAT on | |
| wait 1ms | | | | | | | |
| EN L -> H | | | | | | VSP,VSN on | |
| wait 15ms | | | | | | | |
| RESET L->H | | | | | | RESET L->H | |
| wait 10ms | | | | | | | |
| (EN H -> L) | | | | | | VSP,VSN off | (*1)Can skip "VSP/VSN off" in case of going to normal mode without staying sleep status. |
| (wait 10ms) | | | | | | | |
| ↓ | | | | | | | |
| SLEEP MODE | | | | | | | |

**(B) On sequence**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| SLEEP MODE | | | | | | | |
| ↓ | | | | | | | |
| EN L -> H | | | | | | VSP,VSN on | (*1) |
| wait 20ms | | | | | | | (*1) |
| | | | | | | | |
| command | 05 | 01 | - | - | L/R | soft reset | |
| wait 5ms | | | | | | | |
| | | | | | | | |
| command | 15 | 3A | 1 | 77 | L/R | set pixel format | |
| command | 39 | 2A | 1 | 00 | L/R | set column address | |
| | | | 2 | 00 | | | |
| | | | 3 | 04 | | | |
| | | | 4 | FF | | | |
| command | 39 | 2B | 1 | 00 | L/R | set page address | |
| | | | 2 | 00 | | | |
| | | | 3 | 06 | | | |
| | | | 4 | 3F | | | |
| send image | 39 | 2C/3C | | | L/R | write memory / write memory continue | |
| | | | | | | | |
| command | 15 | 35 | 1 | 00 | R | set tear on | Recommend monitering TE timing due to the restriction in 2chip system, for details, refer "Restriction on command timing" |
| command | 39 | 44 | 1 | 00 | R | set tear scanline | |
| | | | 2 | 00 | | | |
| command | 15 | 51 | 1 | FF | L/R | write_display_brightness | |
| command | 15 | 53 | 1 | 24 | L/R | write_control_display | |
| command | 15 | 55 | 1 | 00 | L/R | write_adaptive_brightness_control C[1:0] = 0x00 : ACO・CABC Off | Please use Auto Contrast Optimization ( ACO ) function and Content Adaptive Brightness Control ( CABC ) function by C[1:0] register, changing. |
| | | | 1 | 01 | L/R | write_adaptive_brightness_control C[1:0] = 0x01 : ACO On | |
| | | | 1 | 02 | L/R | write_adaptive_brightness_control C[1:0] = 0x02 : CABC On Max. Backlight reduction ratio : -33% setting | |
| | | | 1 | 03 | L/R | write_adaptive_brightness_control C[1:0] = 0x03 : CABC On Max. Backlight reduction ratio : -54% setting | |
| command | 05 | 11 | - | - | L/R | exit sleep mode | |
| wait 120ms | | | | | | | |
| command | 23 | B0 | 1 | 00 | L/R | MCAP Off | This command is inputted for change of LEDPWM clock frequency. When using [ C[1:0] = 0x00 : ACO・CABC Off ] and [ C[1:0] = 0x01 : ACO On ] , it is not necessary to input this command. |
| command | 29 | CE | 1 | 7D | L/R | Back Light Control 4 | (1)This command is inputted for change of LEDPWM clock frequency. When using [ C[1:0] = 0x00 : ACO・CABC Off ] and [ C[1:0] = 0x01 : ACO On ] , it is not necessary to input this command.<br><br>(2)Please optimize a LEDPWM clock frequency by PWMDIV [7:0] and PWM_CYCLE[7:0] according to the characteristic of the LED driver used in your company. |
| | | | 2 | 40 | | | |
| | | | 3 | 48 | | | |
| | | | 4 | 56 | | | |
| | | | 5 | 67 | | | |
| | | | 6 | 78 | | | |
| | | | 7 | 88 | | | |
| | | | 8 | 98 | | | |
| | | | 9 | A7 | | | |
| | | | 10 | B5 | | | |
| | | | 11 | C3 | | | |
| | | | 12 | D1 | | | |
| | | | 13 | DE | | | |
| | | | 14 | E9 | | | |
| | | | 15 | F2 | | | |
| | | | 16 | FA | | | |
| | | | 17 | FF | | | |
| | | | 18 | 04 | | PWM_DIV[7:0] | |
| | | | 19 | 00 | | PWM_CYCLE[7:0] | |
| Deleted from Video through mode sequence | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| command | 23 | B0 | 1 | 03 | L/R | MCAP On | |
| Deleted from Video through mode sequence | | | | | | | |
| command | 05 | 29 | - | - | L/R | set display on | |
| wait 0ms min. | | | | | | | |
| LED backlight on | | | | | | | |
| ↓ | | | | | | | |
| NORMAL MODE, I/F : Command mode | | | | | | | |

# LCM Control Sequence (Continued)

(1)These CABC setting values are our proposal values.
It optimizes based on the evaluation result of your company.

CABC On -33% : Max. Backlight power reduction rate -33% setting
CABC On -54% : Max. Backlight power reduction rate -54% setting

(2)LEDPWM frequency calculation formula
LEDPWM frequency = fOSC2 / ( PWMDIV + 1 ) / ( PWM_CYCLE + 255 )
fOSC2 spec. = 26.6MHz(min.) - 28MHz(typ.) - 29.4MHz(max.)

(3)LEDPWM frequency default setting :
Command 0xCE, PWMDIV[7:0]=0x04, PWM_CYCLE[7:0]=0x00
LEDPWM frequency = 28MHz (typ.) / (4+1) / (0+255) = 21.961kHz(typ.)

**(c) Off sequence**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| NORMAL MODE | | | | | | | |
| ↓ | | | | | | | |
| LED backlight off | | | | | | | |
| wait 0ms min. | | | | | | | |
| command | 05 | 28 | - | - | L/R | set display off | |
| wait 20ms | | | | | | | |
| command | 05 | 10 | - | - | L/R | enter sleep mode | |
| wait 80ms | | | | | | | In Video mode, please continue the input of Vsync packet, Hsync packet, and DSICLK until Off sequence is completed. |
| EN H -> L | | | | | | VSP,VSN off | |
| wait 10ms | | | | | | | |
| ↓ | | | | | | | |
| SLEEP MODE | | | | | | | |

**(D) Power off**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| SLEEP MODE | | | | | | | |
| ↓ | | | | | | | |
| RESET H->L | | | | | | | |
| PWR supply off | | | | | | VDDIO, VBAT off | |
| ↓ | | | | | | | |
| POWER OFF STATE | | | | | | | |

**(E) Enter DSTB**

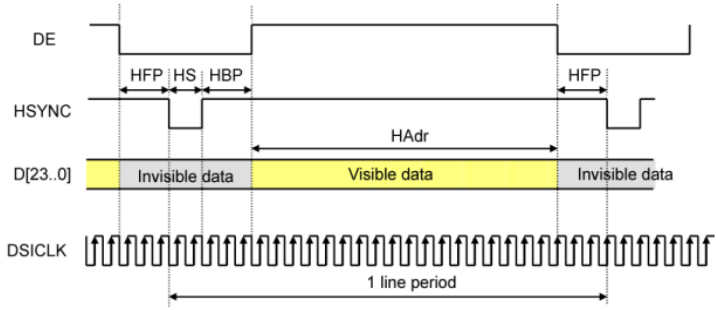
| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| SLEEP MODE | | | | | | | |
| ↓ | | | | | | | |
| command | 23 | B0 | 1 | 00 | L/R | MCAP | |
| command | 23 | B1 | 1 | 01 | L/R | DSTB=1 | |
| ↓ | | | | | | | |
| DSTB MODE | | | | | | | |

**(F) Exit DSTB**

| sequence | DataType (hex) | index (hex) | parameters # | parameters (hex) | L/R | description | comment |
|---|---|---|---|---|---|---|---|
| DSTB MODE | | | | | | | |
| ↓ | | | | | | | |
| RESET H -> L | | | | | | | |
| wait 10ms | | | | | | | |
| EN L -> H | | | | | | VSP,VSN on | |
| wait 20ms | | | | | | | |
| RESET L->H | | | | | | RESET L->H | |
| wait 10ms | | | | | | | |
| (EN H -> L) | | | | | | VSP,VSN off | (*1)Can skip "VSP/VSN off" in case of going to normal mode without staying sleep status. |
| (wait 10ms) | | | | | | | |
| ↓ | | | | | | | |
| SLEEP MODE | | | | | | | |

## 8.2.9 Timing restrictions in Video mode

The blanking period is specified for the pixel data transfer to the two chips in Video Mode.
Set 45 ByteClock or less in the time that the pixel data transfer to the salve chip precedes and is behind the pixel data transfer to the master chip.



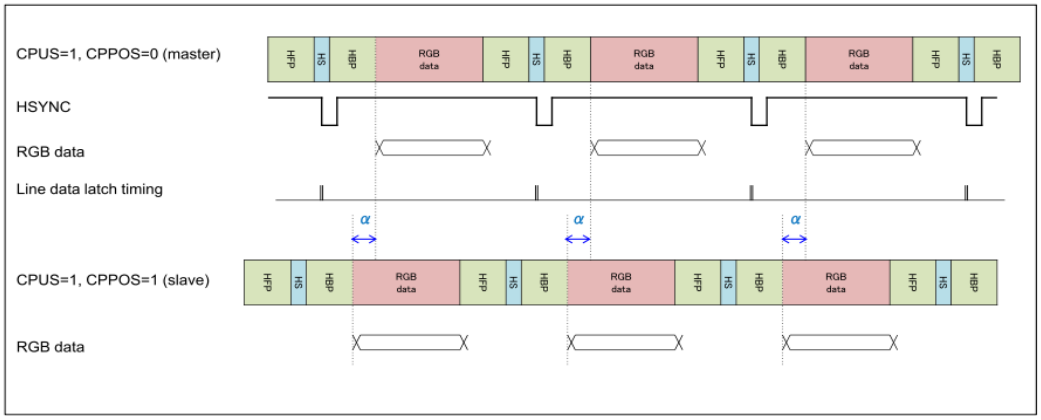

| Item | Symbol | Condition | Unit | Min. |
|---|---|---|---|---|
| Horizontal front porch | HFP | | ByteClock | 4lanes:100+β |
| Horizontal data start point | - | HS+HBP | ByteClock | 45+α |

αβ ≤ 45 ByteClock

α: Time the pixel data is transferred to the slave chip (CPUS=1, CPPOS=1) precedes time the pixel data is transferred to the master chip (CPUS=1, CPPOS=0)
β: Time the pixel data is transferred to the slave chip (CPUS=1, CPPOS=1) is behind time the pixel data is transferred to the master chip (CPUS=1, CPPOS=0)
1 ByteClock = 4 DSI Clock, 1ByteClock=4/3PixelClock (4 lanes)

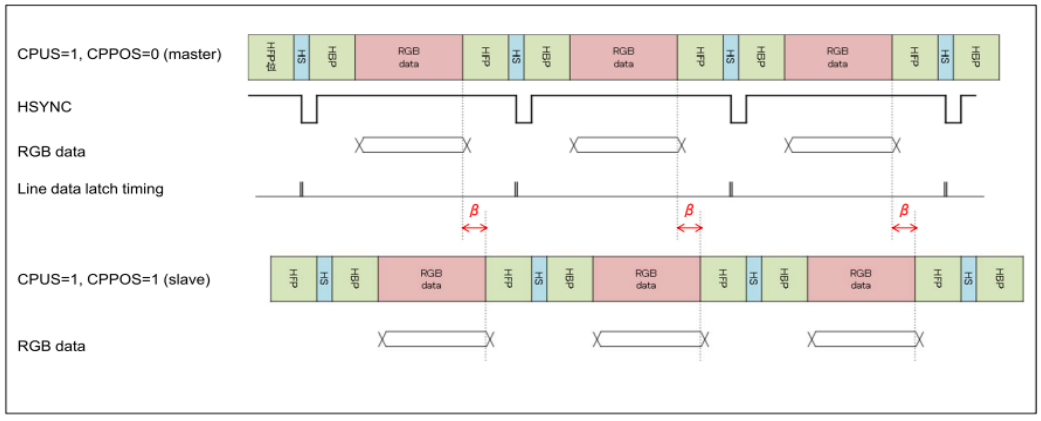
### 1) Video Access (Pixel Data Transfer to Slave Chip Precedes Pixel Data Transfer To Master Chip)

Add the precursor time α to the HS+HBP (horizontal data start point) setting.




### 2) Video Access (Pixel Data Transfer to Slave Chip is behind Pixel Data Transfer to Master Chip)

Add the delay time β to the HFP (Horizontal front porch) setting.

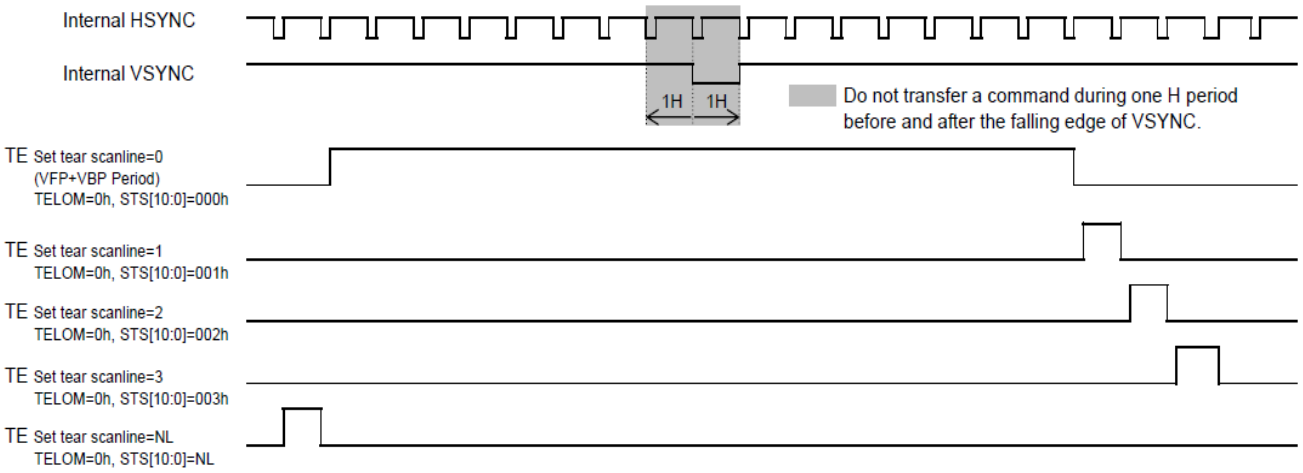


8.2.10 Restriction on command timing (in case of command access)

## Timing Restrictions on the transfer command of Two-Chip Structure

When two chips are used (for point-to-point system), the execution of a command in a first chip may be one frame period behind that of a command in a second chip according to the timing that the host transfer a command. Therefore, the transfer command has the following timing restrictions.

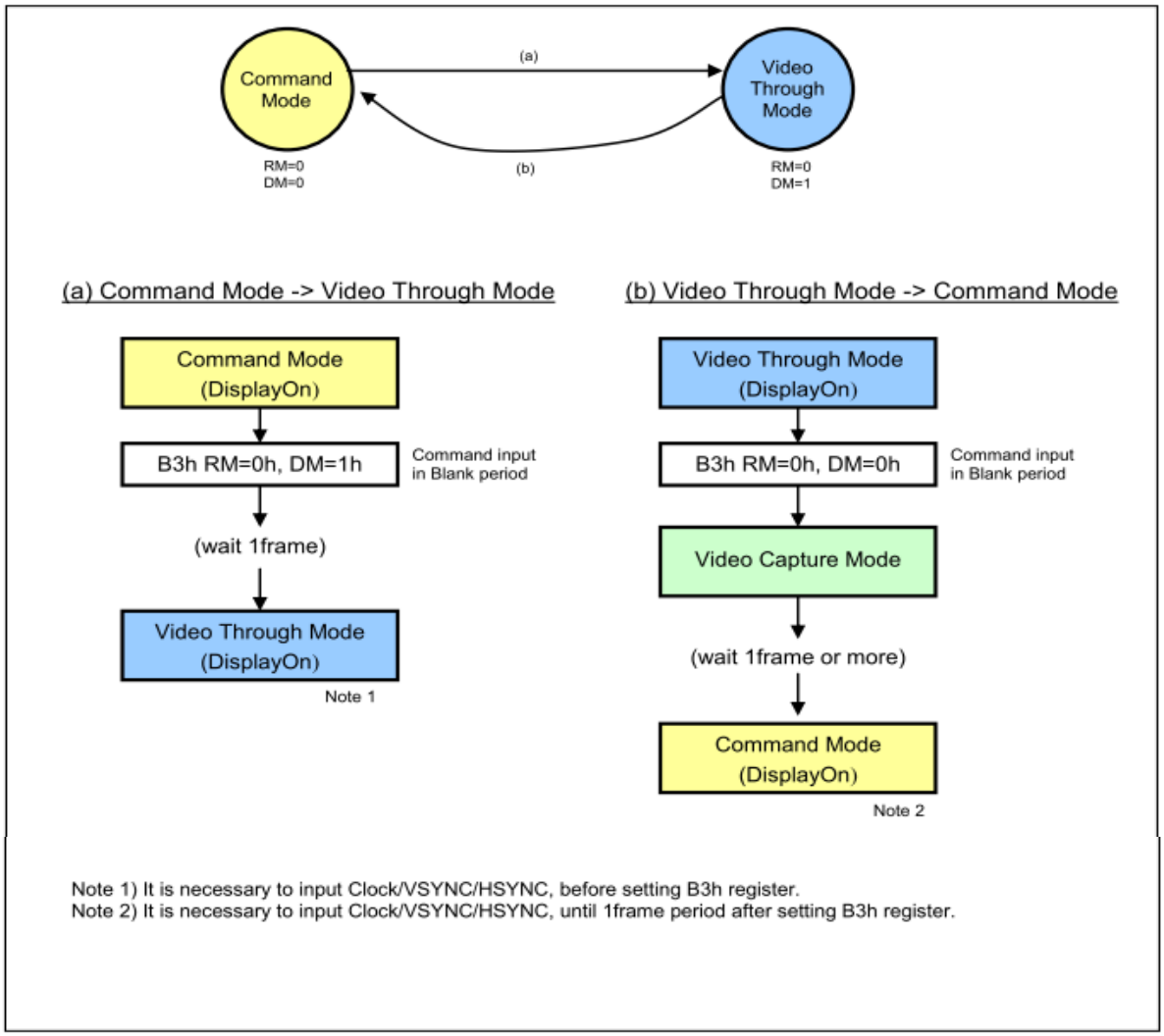
2. Command Access



8.2.11 Display mode change in SleepOUT (Display on)

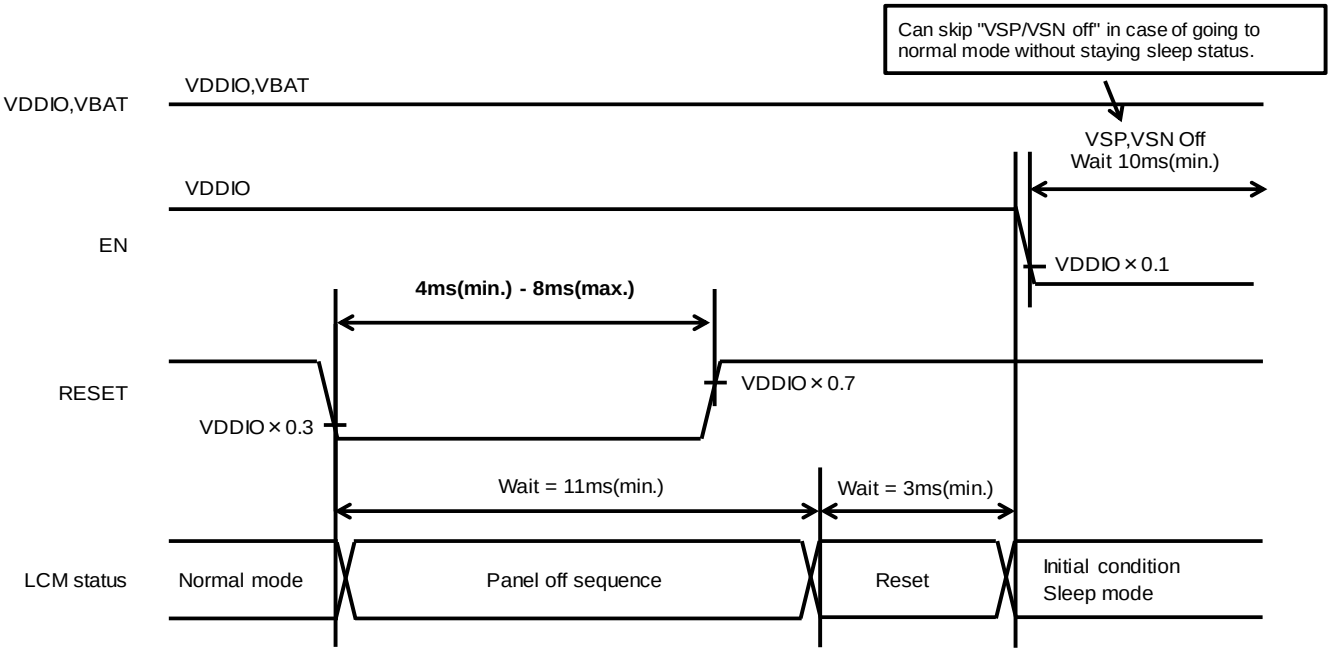
**(2) Display mode change in SleepOut (Display On)**

Command Mode and Video Through Mode can be changed while on DisplayOn state via Video Capture Mode. (Case B3h V2CRM bit = 1)




Note 1) It is necessary to input Clock/VSYNC/HSYNC, before setting B3h register.
Note 2) It is necessary to input Clock/VSYNC/HSYNC, until 1frame period after setting B3h register.

8.2.12 Reset timing spec. during display



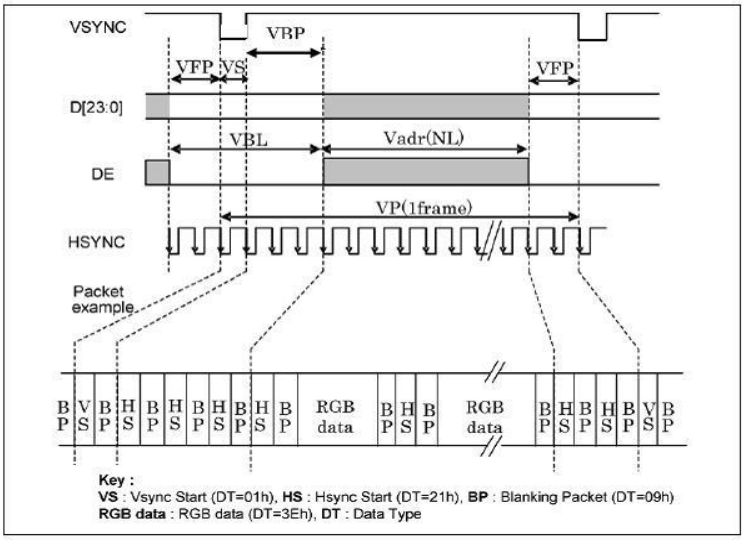
8.2.13 Interface setting

MIPI-DSI Video mode timing chart

| | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| # of lane | - | 4 | - | lane |
| HS+HBP | 45 | *(69)* | - | ByteClock |
| Hadr | - | 960 | - | ByteClock |
| | - | 1280 | - | pixel |
| HFP | 100 | *(123)* | - | ByteClock |
| Hp | - | *(1152)* | - | ByteClock |
| | - | 10.29 | - | us |
| VS | - | 4 | - | Line |
| VBP | - | 4 | - | Line |
| Vadr | - | 1600 | - | Line |
| VFP | - | 12 | - | Line |
| Vp | - | 1620 | - | Line |

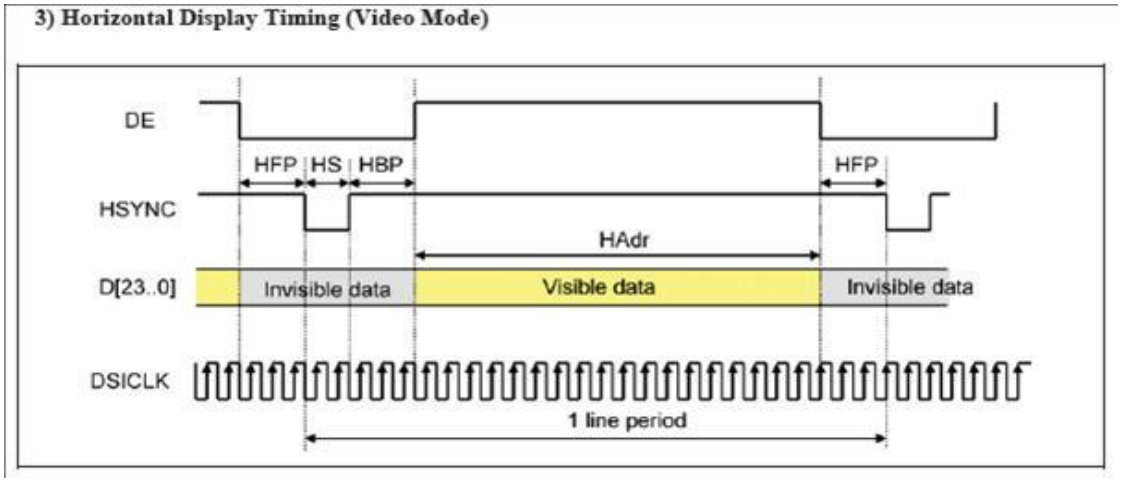
| | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Vsync | - | 60.0 | - | Hz |
| Hsync | - | 97.2 | - | kHz |
| DSI Bit rate | - | 896 | 1000 | Mbps/lane |
| fDSICLK | - | 448 | - | MHz |
| fByteClock | - | 112 | - | MHz |

**2) Vertical Display Timing (Video Mode)**




Note: Case of 24bpp(DT=3Eh) 18bpp(DT=2Eh)
Same timing for each DSI port

**3) Horizontal Display Timing (Video Mode)**



8.3 MIPI-DSI Characteristics

8.3.1 DC Characteristics

| Item | | Symbol | Unit | Test condition | Min. | Typ. | Max. | Note |
|---|---|---|---|---|---|---|---|---|
| HS-RX | Differential input high threshold | VIDTH | mV | | - | - | 70 | 3 |
| | Differential input low threshold | VIDTL | mV | | -70 | - | - | 3 |
| | Single-ended input low voltage | VILHS | mV | | -40 | - | - | |
| | Single-ended input high voltage | VIHHS | mV | | - | - | 460 | |
| | Common-mode voltage HS receive mode | VCMRX(DC) | mV | | 70 | - | 330 | 1 |
| | Differential input impedance | ZID | Ω | | - | 100 | - | 2 |
| LP-RX | Logic 0 input voltage not in ULP State | VIL | mV | | -50 | - | 550 | |
| | Logic 1 input voltage | VIH | mV | | 880 | - | 1350 | |
| | I/O leakage current | ILEAK | μA | Vin= -50mV - 1350mV | -10 | - | 10 | |
| LP-TX | Thevenin output low level | VOL | mV | | -50 | - | 50 | |
| | Thevenin output high level | VOH | V | | 1.1 | 1.2 | 1.3 | |
| | Output impedance of LP Transmitter | ZOLP | Ω | | 110 | - | - | 2 |
| CD-RX | Logic 0 contention threshold | VILCD | mV | | - | - | 200 | |
| | Logic 1 contention threshold | VIHCD | mV | | 450 | - | - | |

Note: 1. VCMRX(DC)=(VDP+VDN)/2

2. Excluding COG resistance (contact resistance and ITO wiring resistance).

3. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

8.3.2 MIPI DSI HS-RX Clock and Data-Clock Specifications

| Item | Symbol | Unit | Min. | Typ. | Max. | Note |
|---|---|---|---|---|---|---|
| DSICLK Frequency | fDSICLK | MHz | 100 | - | 500 | 4 |
| DSICLK Cycle time | tCLKP | ns | 1 | - | 10 | |
| DSI Data Transfer Rate | tDSIR | Mbps | 200 | - | 1000 | 4 |
| Data to Clock Setup Time | tSETUP | UI | 0.15 | - | - | 6 |
| | | ns | 0.15 | - | - | 5,6 |
| Clock to Data Hold Time | tHOLD | UI | 0.15 | - | - | 6 |
| | | ns | 0.15 | - | - | 5,6 |

Note: 4. When fDSICLK < 125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.

5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.

6. tSETUP/tHOLD Time are measured without HS-TX Jitter.

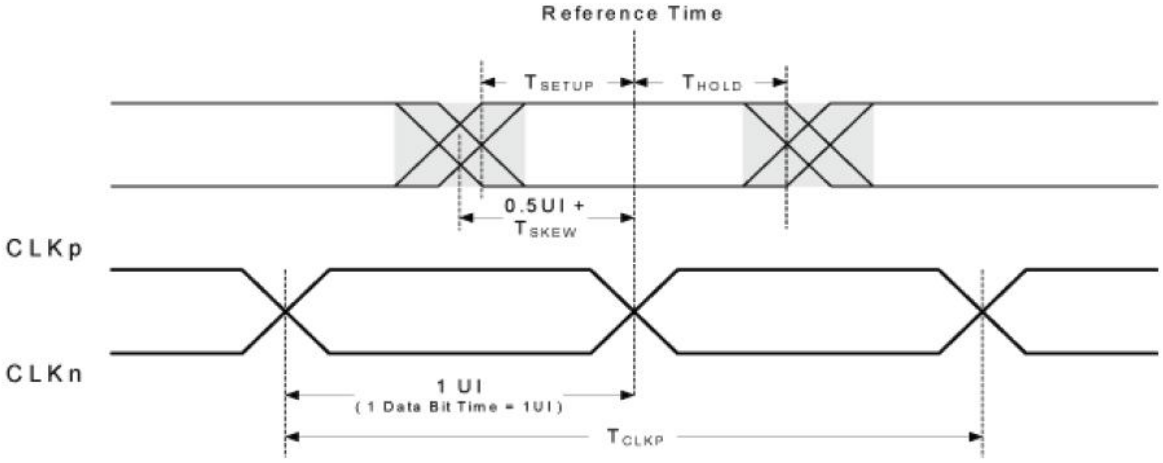



Figure. Data to Clock Timing Definitions

8.3.3 MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

| Parameter | Description | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| $T_{HS-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 40 ns+4*UI | - | 85 ns+6*UI | ns | |
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence | 145 ns+10*UI | - | - | ns | |
| $T_{HS-TRAIL}$ | Time to drive flipped differential state after last payload data bit of a HS transmission burst | max (n*8*UI, 60 ns+n*4*UI) | - | - | ns | 1,2 |
| $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | - | ns | |
| $T_{TA-GO}$ | Time to drive LP-00 after Turnaround Request | $4*T_{LPTX}$ | | | | |
| $T_{TA-SURE}$ | Time-out before new TX side starts driving | $1*T_{LPTX}$ | - | $2*T_{LPTX}$ | | |
| $T_{TA-GET}$ | Time to drive LP-00 by new TX | $5*T_{LPTX}$ | | | | |
| $T_{LPX}$ | Length of any Low-Power state period | 50 | - | - | ns | |
| Ratio $T_{LPX}$ | Ratio of $T_{LPX(MASTER)}$ / $T_{LPX(SLAVE)}$ between Master and Slave side | 2/3 | - | 3/2 | | |
| $T_{CLK-POST}$ | Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode | 60 ns+52UI | - | - | ns | 3 |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock | 300 | - | - | ns | |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode | 8 | - | - | UI | |
| $T_{CLK-PREPARE}$ | Time to drive LP-00 to prepare for HS clock transmission | 38 | - | 95 | ns | |
| $T_{CLK-TRAIL}$ | Time to drive HS differential state after last payload clock bit of an HS transmission burst | 60 | - | - | ns | |
| $T_{EOT}$ | Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state | - | - | 105 ns+n*12*UI | | 2 |
| $T_{LPTX1}$ | Length of Low-Power TX period in case of using DSI clock | - | 48 | - | UI | 4 |
| $T_{LPTX2}$ | Length of Low-Power TX period in case of using internal OSC clock | - | 1/fosc1 | - | ns | |

Note: 1. If a>b then max(a,b)=a, otherwise max(a,b)=b

2. Where n=1 for Forward-direction HS mode

3. The R69429 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R69429 can work without the remained process if tCLK-POST is more than 256 UI.

4. The R69429 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disable. Here,"fosc1" is the frequency of oscillator clock, typical 28MHz.

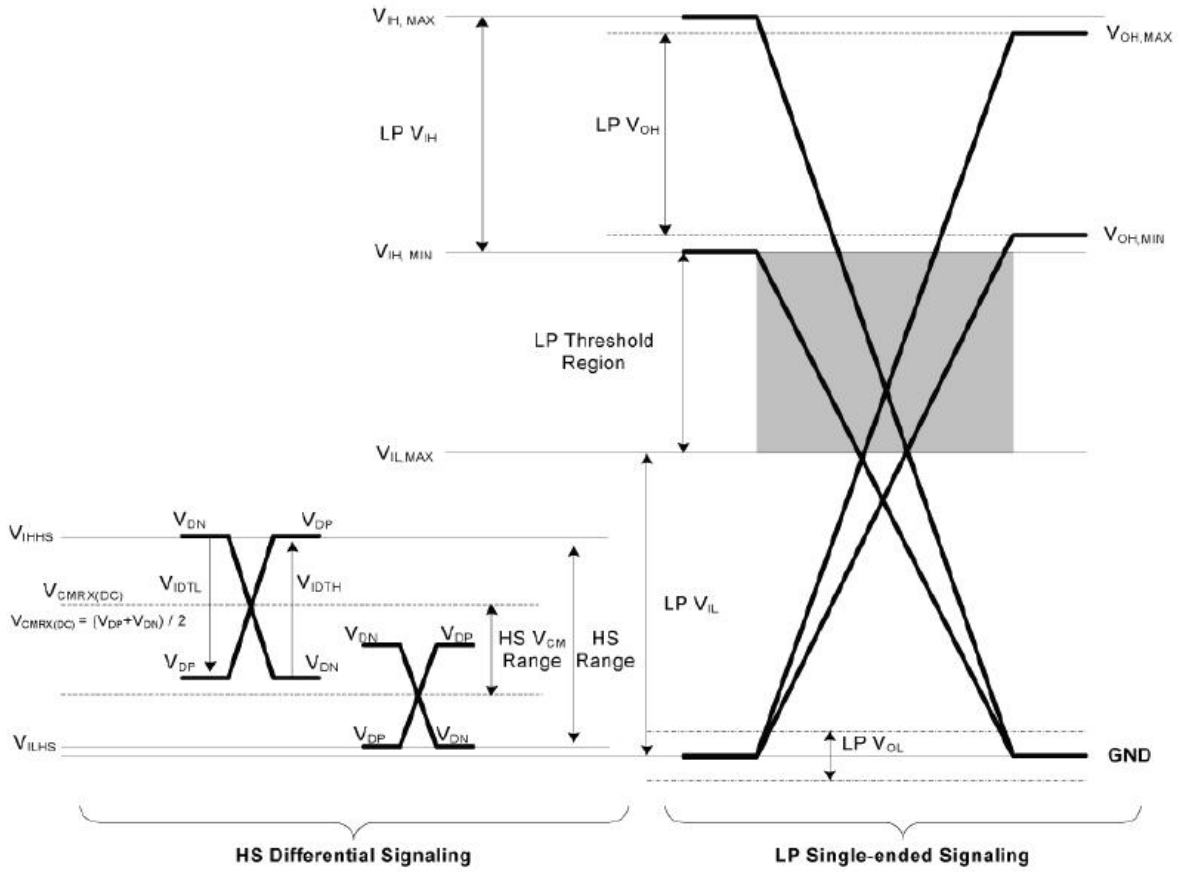
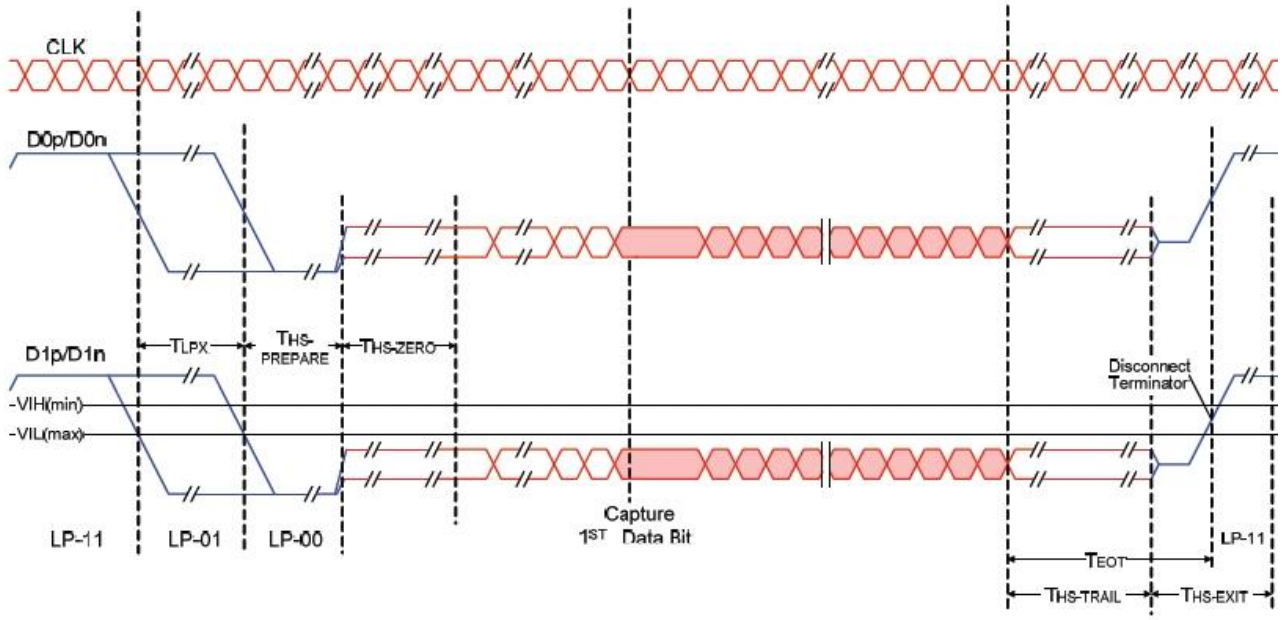



Figure. DSI LP Mode




Note: THS-SYNC: Proper match found for Sync sequence in HS stream,the following bits are payload data.

Figure. HS Data Transmission in Bursts

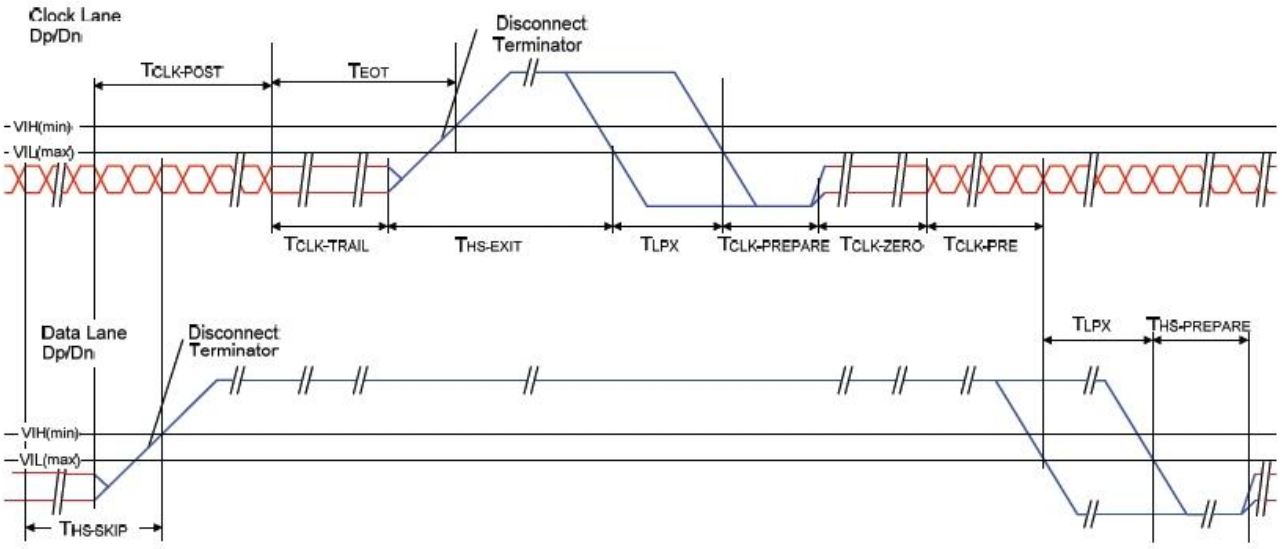



Figure. Switching the Clock Lane between Clock Transmission and LP Mode

8.3.4 ID Code

1. ID Bit Programming

| | | | | |
|---|---|---|---|---|
| **MP (J1)** | ID1 ( ID1[15:8] ) | Vendor Code | 001 | JDI |
| | | Build | 01 | MP |
| | | | 000 | J1 |
| | ID2 ( ID1[7:0] ) | Reserved | 00 | - |
| | | Register setting revision | 01010 | Rev.1.0 |
| | ID3 ( ID2[15:8] ) | Year | - | - |
| | | Week code | - | - |
| **MP (D1)** | ID1 ( ID1[15:8] ) | Vendor Code | 001 | JDI |
| | | Build | 01 | MP |
| | | | 001 | D1 |
| | ID2 ( ID1[7:0] ) | Reserved | 00 | - |
| | | Register setting revision | 01010 | Rev.1.0 |
| | ID3 ( ID2[15:8] ) | Year | - | - |
| | | Week code | - | - |

2. Driver IC ID Bit Programming

| Command | A1h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1st Parameter | ID1[15:8] | Vendor Code | | | Reserved | | Build | | |
| 2nd Parameter | ID1[7:0] | - | Reserved | | Register setting revision | | | | |
| 3rd Parameter | ID2[15:8] | Year | | Week code | | | | | |

**MP (J1)**

| Command | A1h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| 1st Parameter | ID1[15:8] | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 |
| 2nd Parameter | ID1[7:0] | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A |
| 3rd Parameter | ID2[15:8] | MP Production year and week code | | | | | | | | |

**MP (D1)**

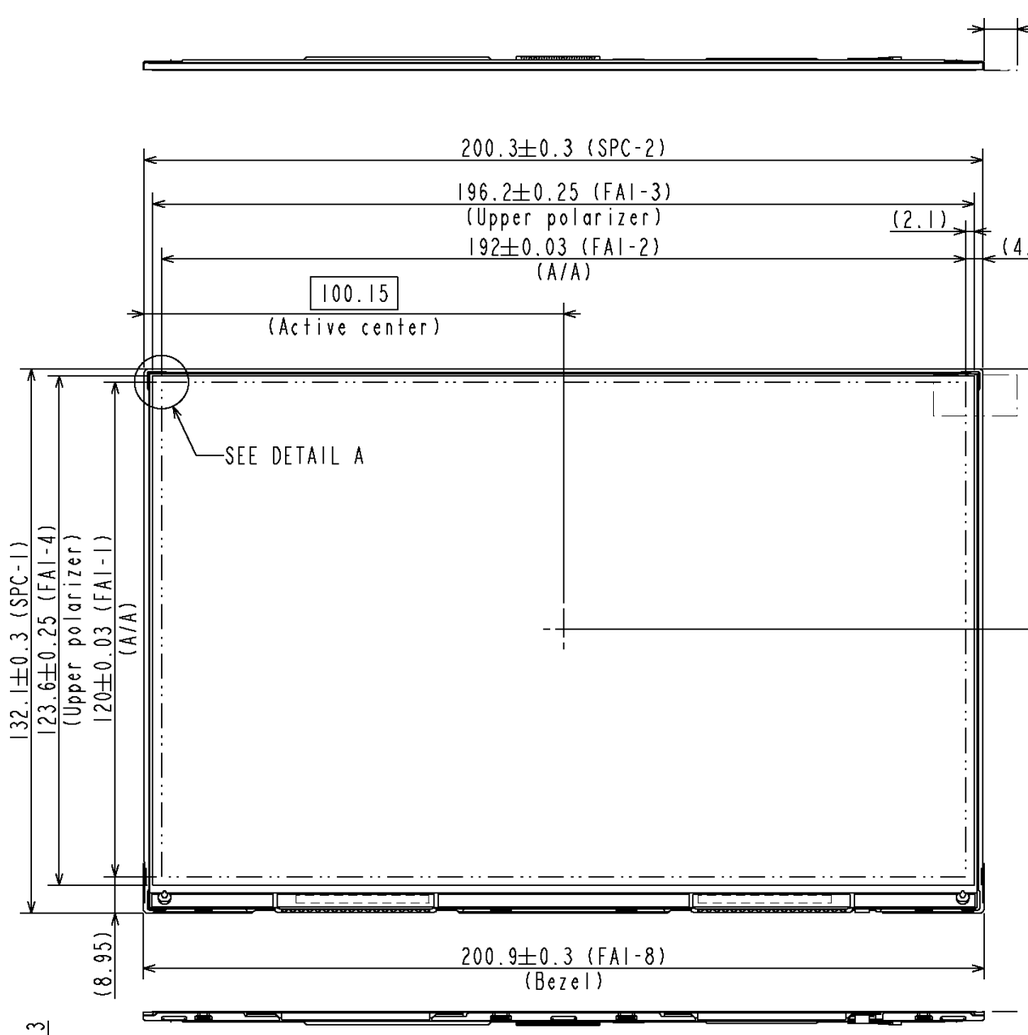
| Command | A1h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|
| 1st Parameter | ID1[15:8] | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 |
| 2nd Parameter | ID1[7:0] | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A |
| 3rd Parameter | ID2[15:8] | MP Production year and week code | | | | | | | | |

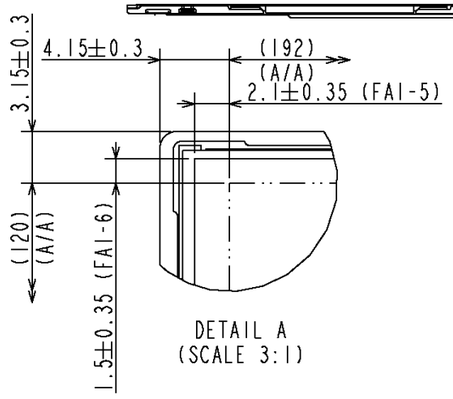
**MP Production year and week code**

| Production week | | Year code 01 :2013 10 : 2014 | Week code | ID 3rd Parameter (HEX) |
|---|---|---|---|---|
| 9/9 - 9/15 | Week37 | 01 | 100101 | 65 |
| 9/16 - 9/22 | Week38 | 01 | 100110 | 66 |
| 9/23 - 9/29 | Week39 | 01 | 100111 | 67 |
| 9/30 - 10/6 | Week40 | 01 | 101000 | 68 |
| 10/7 - 10/13 | Week41 | 01 | 101001 | 69 |
| 10/14 - 10/20 | Week42 | 01 | 101010 | 6A |
| 10/21 - 10/27 | Week43 | 01 | 101011 | 6B |
| 10/28 - 11/3 | Week44 | 01 | 101100 | 6C |
| 11/4 - 11/10 | Week45 | 01 | 101101 | 6D |
| 11/11 - 11/17 | Week46 | 01 | 101110 | 6E |
| 11/18 - 11/24 | Week47 | 01 | 101111 | 6F |
| 11/25 - 12/1 | Week48 | 01 | 110000 | 70 |
| 12/2 - 12/8 | Week49 | 01 | 110001 | 71 |
| 12/9 - 12/15 | Week50 | 01 | 110010 | 72 |
| 12/16 - 12/22 | Week51 | 01 | 110011 | 73 |
| 12/23 - 12/29 | Week52 | 01 | 110100 | 74 |
| 12/30 - 1/5 | Week1 | 10 | 000001 | 81 |
| 1/6 - 1/12 | Week2 | 10 | 000010 | 82 |

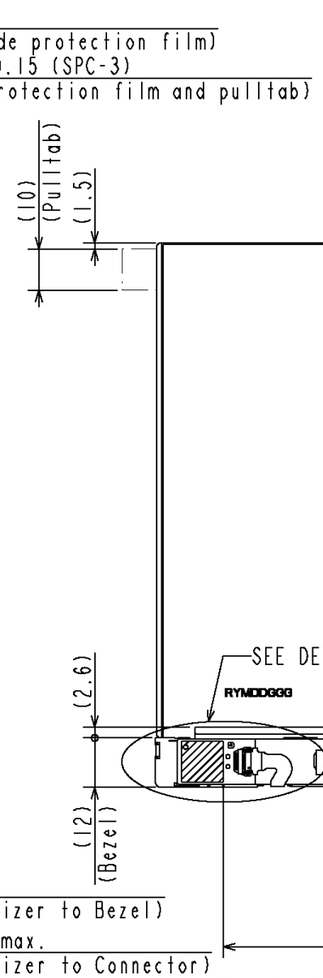
# 10. DIMENSIONAL OUTLINE

**ONLY REFERENCE PURPOSE (No Guarantee)**



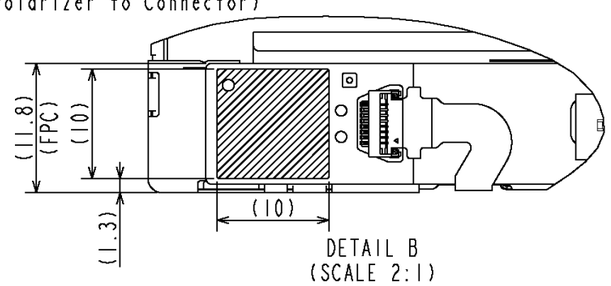




DETAIL A
(SCALE 3:1)










DETAIL B
(SCALE 2:1)

·INTERNAL PIN CONNECTION

| No. | Signal | No. | Signal | No. | Signal | No. | Signal |
|---|---|---|---|---|---|---|---|
| 1 | GND | 17 | DSI_R-DATA-2P | 33 | N.C | 49 | GND |
| 2 | GND | 18 | DSI_R-DATA-2N | 34 | VBAT | 50 | DSI_L-DATA-1P |
| 3 | GND | 19 | GND | 35 | VBAT | 51 | DSI_L-DATA-1N |
| 4 | V_LED_C6 | 20 | DSI_R-DATA-1P | 36 | VBAT | 52 | GND |
| 5 | V_LED_C5 | 21 | DSI_R-DATA-1N | 37 | VBAT | 53 | DSI_CLKP |
| 6 | V_LED_C4 | 22 | GND | 38 | N.C | 54 | DSI_CLKN |
| 7 | V_LED_C3 | 23 | DSI_CLKP | 39 | VDDIO | 55 | GND |
| 8 | V_LED_C2 | 24 | DSI_CLKN | 40 | VDDIO | 56 | DSI_L-DATA-0P |
| 9 | V_LED_C1 | 25 | GND | 41 | GND | 57 | DSI_L-DATA-0N |
| 10 | V_LED_A | 26 | DSI_R-DATA-0P | 42 | DBIST(GND) | 58 | GND |
| 11 | V_LED_A | 27 | DSI_R-DATA-0N | 43 | TE_S | 59 | DSI_L-DATA-3P |
| 12 | N.C | 28 | GND | 44 | GND | 60 | DSI_L-DATA-3N |
| 13 | GND | 29 | DSI_R-DATA-3P | 45 | RESET | 61 | GND |
| 14 | PWM | 30 | DSI_R-DATA-3N | 46 | GND | - | - |
| 15 | TE | 31 | GND | 47 | DSI_L-DATA-2P | - | - |
| 16 | GND | 32 | EN | 48 | DSI_L-DATA-2N | - | - |

·Back side BL serial No.

| | |
|---|---|
| R | Rev (A : All sheet 6hunger) |
| Y | Year (2013 = 3) |
| MM | Month |
| DD | Day |
| GGG | S/N |