

MODEL NO.

CAMERA MODULE CM6128-B200SF-E

Version:1.1

Step 08, 2012

PRODUCT : CAMERA MODULE : CM6128-B200SF-E

SUPPLIER : TRULY OPTO-ELECTRONICS LTD.

DATE : Step 08, 2012



CERT. No. 946535 ISO9001 TL9000

SPECIFICATION

Revision: 1.1

CM6128-B200SF-E

If there is no special request from customer, TRULY OPTO-ELECTRONICS LTD. will not reserve the tooling of the product under the following conditions:

1. There is no response from customer in two years after TRULY OPTO-ELECTRONICS LTD. submit the samples;

2. There is no order in two years after the latest mass production.

And correlated data (include quality record) will be reserved one year more after tooling was discarded.

TRULY OPTO-ELECTRONICS LTD.: **CUSTOMER:**

| Quality Assurance Department:Approved by: | Approved by: |
|---|--------------|
| Technical Department: | |
| | |



REVISION RECORD

| REV NO. | REV DATE | CONTENTS | REMARKS |
|---------|------------|------------------------------|---------|
| 1.0 | 2011-03-11 | First release | |
| 1.1 | 2012-09-08 | Modified / Update some SPEC. | |
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| WRITTEN BY | CHECKED BY | APPROVED BY |
|-------------|--------------|-------------|
| WANG FU MIN | WEI YOU XING | LIU TIE NAN |

Key Information

| Module No. | | CM6128-B200SF-E | | |
|-----------------------|-----------------|---|--|--|
| Module Size | | 6.50mm × 6.50mm × 4.35mm | | |
| Sensor Type | | OV2659 | | |
| Array Size | UXGA | 1632 × 1212 | | |
| | Core | 1.5VDC +/-5% | | |
| Power Supply | Analog | 2.6~3.0V | | |
| | I/O | 1.7~3.0V(Typical 2.8V) | | |
| Lens | | 1/5 inch 3Plastic+ IR | | |
| Focus(F.NO) | | 2.8 | | |
| View Angle | | 62° | | |
| Object Distance | | 60cm-infinity | | |
| Image Area | | 2856μm × 2121μm | | |
| Sensitivity | | 960 mV/Lux-sec | | |
| Pixel Size | | 1.75μm × 1.75μm | | |
| IR Cutter | | 650nm | | |
| Tama anatawa Dan aa | Operating | -20°C to 70°C | | |
| Temperature Range | Stable Image | 0°C to 50°C | | |
| Output Formats(8-bit) | | YUV(422)/YCbCr422 GBR422 RGB565/555 8-/10-bit raw RGB data | | |
| | UXGA(1600×1200) | 15 fps | | |
| Maximum Image | SVGA (800×600) | 30 fps | | |
| Transfer Rate | 720P(1280×720) | 30 fps | | |
| | 1366x768 | 24 fps | | |
| Max S/N Ratio | | 36 dB | | |
| Dynamic Range | | 66 dB @ 8×gain | | |
| IC Package | | 47-pin CSP3 | | |
| Sensor Power | Active | 142mW (using 1.8V DOVDD) | | |
| Requirements | Standby | 30μΑ | | |
| Shutter | | rolling shutter | | |
| Scan Mode | | Progressive | | |
| Maximum Exposure In | nterval | $1228 \times t_{ROW}$ | | |
| Gamma Correction | | Programmable | | |
| Dark Current | | 4 mV/s @ 60°C junction temperature | | |
| Package | | Antistatic Plastic | | |



Pin Assignment

| No. | Name | Pin type | Description |
|-----|-------|----------|---|
| 1 | D0 | I/O | DVP data output port 0 |
| 2 | AVDD | Power | Power for analog circuit/sensor array |
| 3 | D1 | I/O | DVP data output port 1 |
| 4 | AGND | Ground | Ground for analog circuit |
| 5 | D2 | I/O | DVP data output port 2 |
| 6 | DVDD | Power | Power for digital core |
| 7 | D3 | I/O | DVP data output port 3 |
| 8 | RESET | Input | Reset (active low with internal pull-up resistor) |
| 9 | D4 | I/O | DVP data output port 4 |
| 10 | DOVDD | Power | Power for I/O circuit |
| 11 | D5 | I/O | DVP data output port 5 |
| 12 | PWDN | Input | Power down (active high with internal pull-down resistor) |
| 13 | D6 | I/O | DVP data output port 6 |
| 14 | SIO_C | Input | SCCB input clock |
| 15 | D7 | I/O | DVP data output port 7 |
| 16 | SIO_D | I/O | SCCB data |
| 17 | D8 | I/O | DVP data output port 8 |
| 18 | DGND | Ground | Ground for digital circuit |
| 19 | D9 | I/O | DVP data output port 9 |
| 20 | VSYNC | I/O | DVP VSYNC output |
| 21 | DGND | Ground | Ground for digital circuit |
| 22 | HSYNC | I/O | DVP HREF output |
| 23 | MCLK | Input | System input clock |
| 24 | PCLK | I/O | DVP PCLK output |
| 25 | DGND | Ground | Ground for digital circuit |
| 26 | DGND | Ground | Ground for digital circuit |
| 27 | DGND | Ground | Ground for digital circuit |
| 28 | NC | | |
| 29 | DGND | Ground | Ground for digital circuit |
| 30 | NC | | |

Sensor Electrical Characteristics

1. Absolute Maximum Ratings

| parameter | | absolute maximum rating ^a |
|--|--------------------|--------------------------------------|
| | V_{DD-A} | 4.5V |
| supply voltage (with respect to ground) | V_{DD-D} | 3V |
| | $V_{DD\text{-}IO}$ | 4.5V |
| alastus statis disabaura (FCD) | human body model | 2000V |
| electro-static discharge (ESD) | machine model | 200V |
| all input/output voltages (with respect to ground) | | -0.3V to V _{DD-IO} + 1V |
| I/O current on any input or output pin | | ± 200 mA |
| peak solder temperature (10 second dwell time) | | 245°C |

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability

2. Functional temperature

| parameter | range |
|---|-------------------------------------|
| operating temperature ^a | -20°C to +70°C junction temperature |
| stable operating temperature ^b | 0°C to +50°C junction temperature |

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range b. image quality remains stable throughout this temperature range

3.DC Characteristics $(-20^{\circ}\text{C} < \text{TJ} < 70^{\circ}\text{C})$

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| symbol | parameter | min | typ | max | unit | |
|--------------------------------|--------------------------------------|-----------------|------------|-------|------|--|
| supply | | | | | | |
| V _{DD-A} | supply voltage (analog) | 2.6 | 2.8 | 3.0 | V | |
| V _{DD-D} ^a | supply voltage (digital core) | 1.425 | 1.5 | 1.575 | V | |
| $V_{\text{DD-IO}}$ | supply voltage (digital I/O) | 1.7 | 1.8 | 3.0 | V | |
| I _{DD-A} | active (operating) current | | 25 | 30 | mA | |
| I _{DD-IO} b | active (operating) current | | 40 | 50 | mA | |
| I _{DDS-SCCB} | standby current ^c | | 30 | 75 | μΑ | |
| I _{DDS-PWDN} | Standby Current | | 30 | 75 | μΑ | |
| digital inputs | (typical conditions: AVDD = 2.8V, DV | 'DD = 1.5V, DO\ | /DD = 1.8V |) | | |
| V _{IL} | input voltage LOW | | | 0.54 | V | |
| V_{IH} | input voltage HIGH | 1.26 | | | V | |
| C _{IN} | input capacitor | | | 10 | pF | |
| digital output | s (standard loading 25 pF) | | | | | |
| V _{OH} | output voltage HIGH | 1.62 | | | V | |
| V _{OL} | output voltage LOW | | | 0.18 | V | |
| serial interface inputs | | | | | | |
| V_{IL}^d | SIOC and SIOD | -0.5 | 0 | 0.54 | V | |
| V _{IH} ^c | SIOC and SIOD | 1.26 | 1.8 | 2.3 | V | |

a. using the internal regulator is strongly recommended for minimum power down currents

4. AC Characteristics ($T_A=25^{\circ}C$, $V_{DD-A}=2.8V$)

| symbol | parameter | min | typ | max | unit |
|-----------|--|-----|-----|------|------|
| ADC parar | neters | | | | |
| В | analog bandwidth | | 30 | | MHz |
| DLE | DC differential linearity error | | 0.5 | | LSB |
| ILE | DC integral linearity error | | 1 | | LSB |
| | settling time for hardware reset | | | <1 | ms |
| | settling time for software reset | | | <1 | ms |
| | settling time for resolution mode change | | | <1 | ms |
| | settling time for register setting | | | <300 | ms |

b. active current is based on sensor resolution at full size and full speed

c. standby current is based on room temperature

d. based on DOVDD = 1.8V.



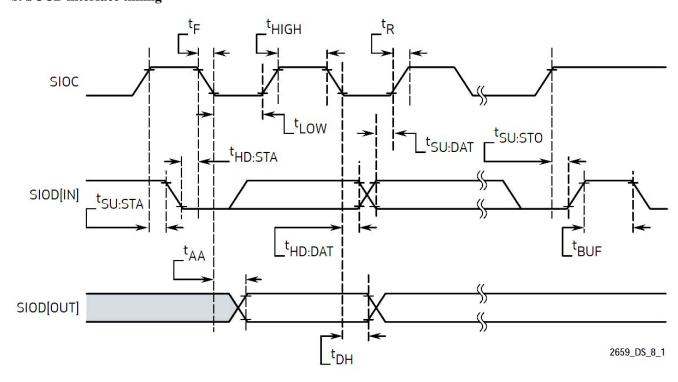
5. Timing Characteristics

a. Timing Characteristics

| symbol | parameter | min | typ | max | unit |
|---------------------------------|----------------------------|-----|-----|----------------------|------|
| oscillator and clock input | | | | | |
| fosc | frequency (XVCLK) | 6 | 24 | 27(54 ^a) | MHz |
| t _r , t _f | clock input rise/fall time | | | 5 (10 ^b) | ns |

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b. SCCB interface timing



a. If using the internal clock pre-scaler.

b. If using the internal PLL.

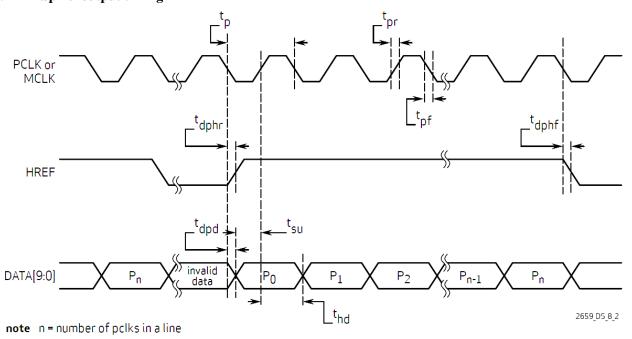


SCCB interface timing specifications^{ab}

| symbol | parameter | min | typ | max | unit |
|---------------------------------|--------------------------------|------|-----|-----|------|
| f _{SIOC} | clock frequency | ' | , | 400 | KHz |
| t _{LOW} | clock low period | 1.3 | | | μs |
| t _{HIGH} | clock high period | 0.6 | | | μs |
| t _{AA} | SIOC low to data out valid | 0.1 | | 0.9 | μs |
| t _{BUF} | bus free time before new start | 1.3 | | | μs |
| t _{HD:STA} | start condition hold time | 0.6 | | | μs |
| t _{SU:STA} | start condition setup time | 0.6 | | | μs |
| t _{HD:DAT} | data in hold time | 0 | | | μs |
| t _{SU:DAT} | data in setup time | 0.1 | | | μs |
| t _{su:sto} | stop condition setup time | 0.6 | | | μs |
| t _R , t _F | SCCB rise/fall times | | | 0.3 | μs |
| t _{DH} | data out hold time | 0.05 | | | μs |

a. SCCB timing is based on 400KHz mode

c. Line/pixel output timing



b. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%



pixel timing specifications^a

| symbol | parameter | min | typ | max | unit |
|-------------------|--|-----|-------|-----|------|
| t _p | PCLK period ^b | | 13.89 | | ns |
| t _{pr} | PCLK rising time ^b | | 1.33 | | ns |
| t _{pf} | PCLK falling time ^b | | 2.41 | | ns |
| t _{dphr} | PCLK negative edge to HREF rising edge | | 1 | | ns |
| t _{dphf} | PCLK negative edge to HREF negative edge | | 1 | | ns |
| t _{dpd} | PCLK negative edge to data output delay | 0 | | 4 | ns |
| t _{su} | data bus setup time | 5 | 7 | | ns |
| t _{hd} | data bus hold time | 5 | 7 | | ns |

a. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%

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6. Format and frame rate

| format | resolution | frame rate | scaling method | parallel port data rate (RAW/YUV) |
|----------|------------|------------|----------------|-----------------------------------|
| UXGA | 1600x1200 | 15 fps | full | 36/72 MHz |
| SVGA | 800x600 | 30 fps | down sampling | 24/48 MHz |
| VGA | 640x480 | 30 fps | scaling | 24/48 MHz |
| 400x300 | 400x300 | 30 fps | subsample | 18/36 MHz |
| 200x150 | 200x150 | 30 fps | subsample | 18/36 MHz |
| 720p | 1280x720 | 30 fps | cropping | 36/72 MHz |
| 1366x768 | 1366x768 | 24 fps | cropping | 36/72 MHz |

7. Power up sequence

Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the I2C during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred.

b. PCLK running at 72 MHz, CL = 10pF, and DOVDD = 2.8V



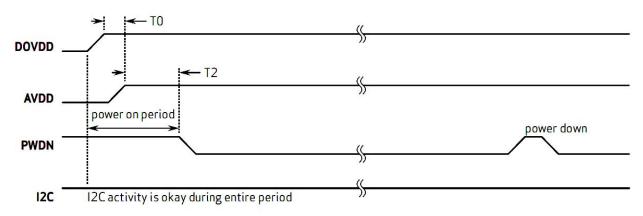
a. power up with internal DVDD and I2C access during power up period

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

- 1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
- 2. PWDN is active high with an asynchronized design (does not need clock)
- 3. PWDN must go high if I2C is accessed during the power up period
- 4. for PWDN to go low, power must first become stable (AVDD to PWDN $\geq 1 \text{ ms}$)
- 5. RESETB is active low with an asynchronized design
- 6. state of RESETB does not matter during power up period once DOVDD is up

power up timing with internal DVDD and I2C access during power up period

DOVDD first, then AVDD, and rising time is less than 5 ms



Note:

 $T0 \ge 0$ ms: delay from DOVDD stable to AVDD stable

 $T2 \ge 1$ ms: delay from AVDD stable to sensor power up stable

b. power up with internal DVDD and no I2C access during power up period

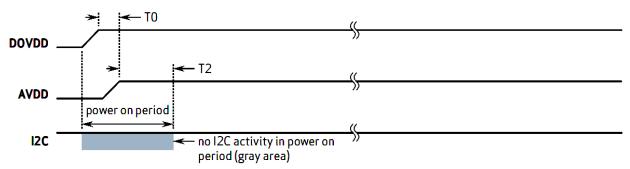
For powering up with the internal DVDD and no I2C access during the power ON period, the following conditions must

occur:

- 1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
- 2. PWDN is not required if there is no I2C access during the power up period
- 3. no I2C activity is allowed during the power up period
- 4. RESETB is active low with an asynchronized design
- 5. state of RESETB does not matter during power up period once DOVDD is up

power up timing with internal DVDD and no I2C access during power up period

DOVDD first, then AVDD, and rising time is less than 5 ms



Note:

 $T0 \ge 0$ ms: delay from DOVDD stable to AVDD stable

 $T2 \ge 1$ ms: delay from AVDD stable to sensor power up stable

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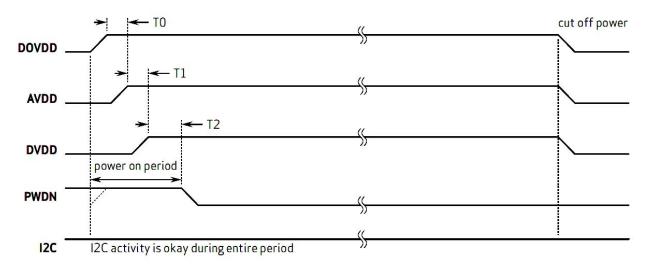
c. power up with external DVDD source and I2C access during power up period

For powering up with an external DVDD source and I2C access during the power ON period, the following conditions must occur:

- 1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
- 2. when AVDD and DVDD are turned ON, make sure AVDD becomes stable before DVDD becomes stable
- 3. PWDN is active high with an asynchronized design (does not need clock)
- 4. for PWDN to go low, power must first become stable (DVDD to PWDN ≥ 1 ms)
- 5. all powers are cut off when the camera is not in use (power down mode is not recommended
- 6. RESETB is active low with an asynchronized design
- 7. state of RESETB does not matter during power up period once DOVDD is up

power up timing with external DVDD source and I2C access during power up period

DOVDD first, then AVDD, followed by DVDD, and rising time is less than 5 ms



Note:

 $T0 \ge 0$ ms: delay from DOVDD stable to AVDD stable

 $T1 \ge 0$ ms: delay from AVDD stable to DVDD stable

 $T2 \ge 1$ ms: delay from DVDD stable to sensor power up stable



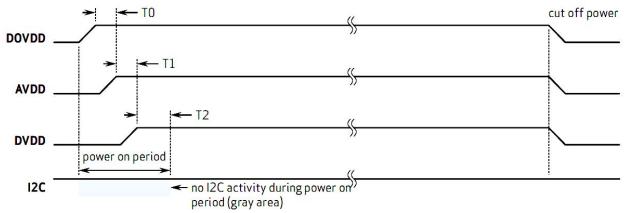
d. power up with external DVDD and no I2C access during power up period

For powering up with an external DVDD source and no I2C access during the power ON period, the following conditions must occur:

- 1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
- 2. when AVDD and DVDD are turned ON, make sure AVDD becomes stable before DVDD becomes stable
- 3. all powers are cut off when the camera is not in use (power down mode is not recommended
- 4. RESETB is active low with an asynchronized design
- 5. state of RESETB does not matter during power up period once DOVDD is up

power up timing with external DVDD source and I2C access during power up period

DOVDD first, then AVDD, followed by DVDD, and rising time is less than 5 ms



Note:

 $T0 \ge 0$ ms: delay from DOVDD stable to AVDD stable

 $T1 \ge 0$ ms: delay from AVDD stable to DVDD stable

 $T2 \ge 1$ ms: delay from DVDD stable to sensor power up stabl

8. hardware standby and software standby

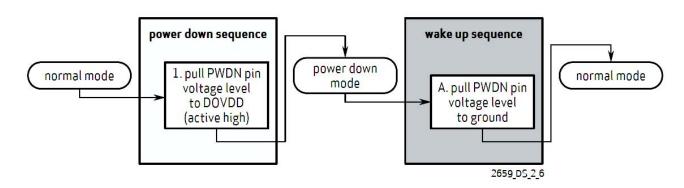
Two suspend modes are available for the OV2659:

- hardware standby
- software standby

a. hardware standby

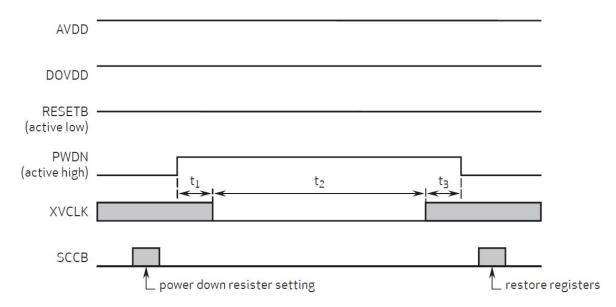
To initiate hardware standby mode, PWDN pin must be tied to high

power down/ wake up sequence





power down timing diagram



Note:

t1: XVCLK should keep more than 0.1ms after PWDN is pulled high

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- t2: power down period should last more than 1 VSYNC period
- t3: XVCLK should come more than 0.1ms before PWDN is pulled low

When this occurs, the OV2659 internal device clock is halted and all internal counters are reset and registers are maintained.

b. software standby control

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

software standby control

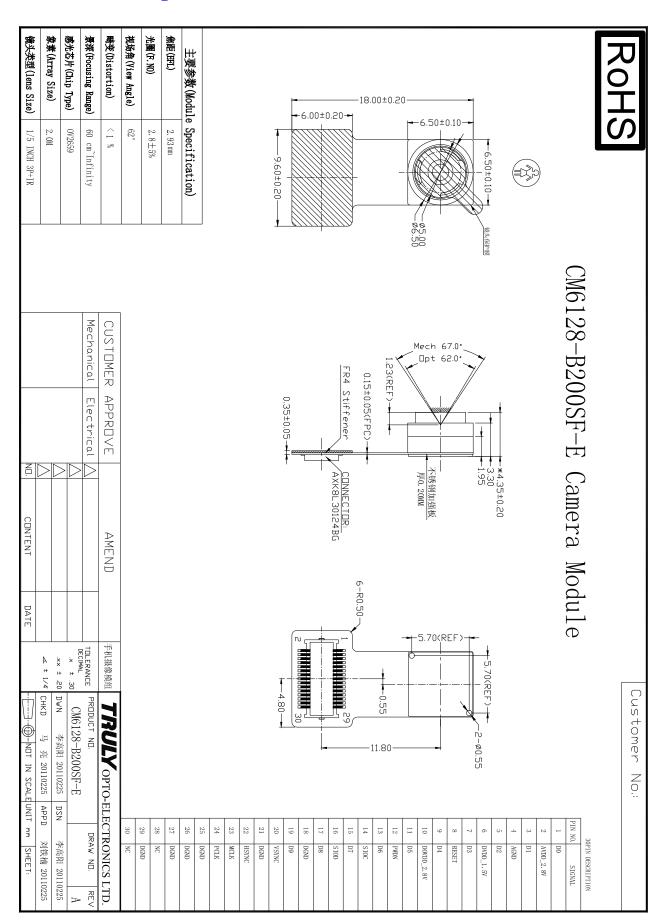
| addres | ss | register name | default value | R/W | descriptio | n |
|--------|----|------------------|------------------|-----|------------|---|
| 0x0100 | | SOFTWARE STANDBY | 0x00 | RW | Bit[0]: | Software standby 0: Software standby 1: Streaming |

Note:

For more information of sensor please refer to the OV2659 specification.

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Mechanical Drawing



Version:1.1

Appearance Specification

| NO. | Item | Standard | Importance Class |
|-----|------------------|--|---------------------|
| 1 | Top side of Lens | No obvious impurity and oil impurity on the front of lens within the half area; No feeling defect; Others are unlimited. | A |
| 2 | Screw glue | Normally screw glue shall be symmetrical distributed around lens circle side. Particular circs, glue distribution must not disturb customer's assembly operation. | A |
| 3 | Holder | No obvious impurity and distortion of outline. The width and length of defect is unlimited, the depth≤0.1mm and ≤1/4 of the thickness of Holder. | В |
| 4 | Sealed glue | Sealed glue distributing between holder and FPC must be symmetrical and smooth. Not allow glue leakage and asymmetric thickness. After holder assembly, the thickness distance between one side and its opposite side shall be less than 0.2mm. Excess glue over the holder shall not make the outside dimension be out of control. | A |
| 5 | FPC/PCB | Edge defect limitation: width \(\le 1/2H \) (H is minimum.), length \(\le 1 \) mm, defect numbers per edge \(\le 2 \) (No tearing gap inby edge for FPC); Edge outshoot limitation (width \(\le 0.3 \) mm, length \(\le 1 \) mm). No obvious impurity and crease on the surface. If there was shield film on the surface, the spot size of the film shall be less than 0.3 \(\text{mm} \times 1 \) mm and no line is exposed. If it was not be cleaned and did not influence the total thickness, it would be permitted. Label and mark shall be clear enough to be discerned. | A |
| 6 | Connector | No dust, fingerprint, and not allows to turning colors, distortion; Solder must be well; No open circuit or short circuit | A |
| 7 | Gold finger | No dust, fingerprint, and not allows to turning colors, burned, unsmoothed and peeled; No open circuit or short circuit; The defect width shall be smaller than 20% of gold finger's width. No copper/nickel exposed in defect. Numbers of defected pin shall be less than 3. The defect limitation:width <0.08 mm, length <5 mm. | A |



| 8 | Stiffener | Holder anchor pole length overtopping the steel plate shall be less than 0.2mm. No dust, rust and deep scratch on the steel surface without Double coated tapes. | В |
|----|---------------------|---|---|
| 9 | Double coated tapes | Adhered direction shall be right. Not allows to excess steel plate edge. No alveoli and stick. Not allows to peel glue and rip protective paper when tear the protective paper. | В |
| 10 | Protective film | No dust in the glue side. Not allows to float or drop. | В |

Remark:

- 1. The definition of the appearance importance class
 - A: The defect can be found in the finished product, or have obvious visual differences from good products, such as crack, defect and dust, or influence image quality, or are appointed by the customer. We will emphasize these items and check all products.
 - B: The defect can be found in the finished product and has visual difference from the good one, but will not affect customer's aesthetic judgement. Or the defect can not be found in the finished product and will not generate functional problem, but will slightly influence sequential manufacture process or condition. We will supervise these items in the manufacturing process and check products selectively.
 - C: Check method:distance 30cm, visual vertical or 45° reflection.

2. Sampling standard

Referenced standard: GB/T 2828.1-2003/ISO 2859-1:1999 and ANSI/ASQC.4-1993 II



Image Specification

| NO. | Item | Standard | Important Class |
|-----|----------------|---|--------------------|
| 1 | TV Line | Center≥700 0.7 viewing field ≥600 | A |
| 2 | Shading | The lighteness of 90% viewing area ≥ 40% of center lighteness(Lens correction Shading [Turn off]); The lighteness of 90% viewing area ≥ 60% of center lighteness(Lens correction Shading [Turn on]) | A |
| 3 | Blemish II I/4 | I area: Blemish number≤1 II area: Blemish number≤4 Blemish: particle size<0.6mm | В |
| 4 | Color | Color distortion ratio of center ± 15% | В |
| 5 | Gray Scale | Margin of two near scales' brightness≥6 | В |
| 6 | Distortion | <1% | В |

Step 08, 2012



Reliability Specification

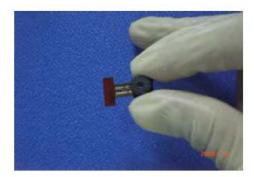
| No. | Test item | Test condition | Judgment | |
|-----|--|---|---|--|
| 1 | Temperature strike cycle [Power off] | Low temperature:-30°C±2°C for 30 min High temperature:+80°C±2°C for 30 min Cycle:10 times | | |
| 2 | High temperature and high humidity storage | Temperature:60°C Humidity:90%RH Time:96 hours | | |
| 3 | Low temperature operating | Temperature:-20°C±2°C Time:96 hours | | |
| 4 | High temperature operating | Temperature:70°C±2°C Time:96 hours | 1.Function: Resolution: difference<20% | |
| 5 | Low temperature storage | Temperature:-30°C±2°C Time:96 hours | after test Shading: | |
| 6 | High temperature storage | Temperature:80°C±2°C Time:96 hours | difference<20% after test | |
| 7 | ESD test [Power off] | C:150pF R:330Ω Voltage:±2KV Air discharge: Cycle:10 times | 2.Appearance: Do not exit NG after test | |
| 8 | Vibration Test [Packaged] | Frequency:10Hz~55Hz~10Hz Amplitude:1.5 mm Times: each X,Y,Z directions for 30mins | | |
| 9 | Dropping test [Packaged] | Product dropping from 150cm height to smooth marble Drop style:1 corner,3 arris,6 faces Test times:10 | | |



Precautions For Using CCM Modules

Handing Precautions

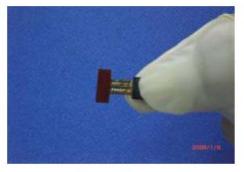
- —DO NOT try to open the unit enclosure as there is no user-serviceable component inside. To prevent damage to the camera module by electrostatic discharge, handling the camera module only after discharging all static electricity from yourself and ensuring a static-free environment for the camera module.
- —DO NOT touch the top surface of the lens.
- —DO NOT press down on the lens.
- —DO NOT try to focus the lens.
- —DO NOT put the camera module in a dusty environment.
- —To reduce the risk of electrical shock and damage to the camera module, turn off the power before connect and disconnect the camera module.
- —DO NOT drop the camera module more than 60 cm onto any hard surface.
- —DO NOT expose camera module to rain or moisture.
- —DO NOT expose camera module to direct sunlight.
- —DO NOT put camera in a high temperature environment.
- —DO NOT use liquid or aerosol cleaners to clean the lens.
- —DO NOT make any charges or modifications to camera module.
- —DO NOT subject camera module to strong electromagnetic field.
- —DO NOT subject the camera module to excessive vibration or shock.
- —DO NOT Impact or nip CCM module with speculate things
- —DO NOT alter, modify or change the shape of the tab on the metal frame.
- —DO NOT make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
- —DO NOT damage or modify the pattern writing on the printed circuit board.
- —Absolutely DO NOT modify the zebra rubber strip (conductive rubber) or heat seal connector
- Except for soldering the interface, DO NOT make any alterations or modifications with a soldering
- —DO NOT twist FPC of CCM.



Correct



Incorrect

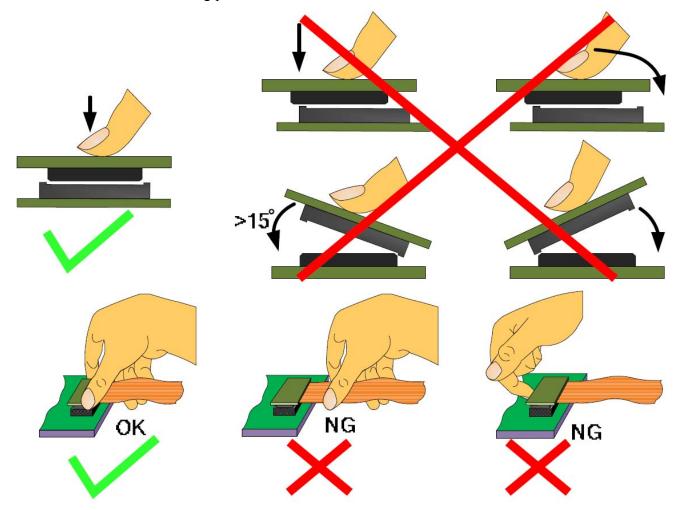


Incorrect

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Precaution for assemble the module with BTB connector:

Please note the position of the male and female connector position, don't assemble or assemble like the method which the following picture shows

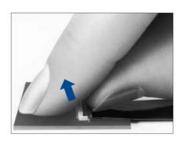


Precaution for assemble the module with ZIF connector:

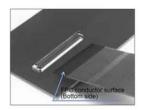
Operation **Precautions**

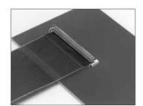
1. FPC/FFC Termination procedure. Connector installed on the board.

1) Lift up the actuator. Use thumb or index finger.

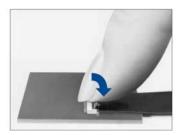


2) Assure that the FPC/FFC is fully inserted parallel to mounting surface, with the exposed conductive traces facing down.



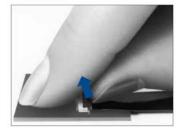


3) Rotate down the actuator until firmly closed. It is critical that the inserted FPC/FFC is not moved and remains fully inserted. Should the FPC/FFC be moved, open the actuator and repeat the process, starting with Step 1 above.



2. FPC/FFC Removal

- 1) Lift up the actuator.
- 2) Carefully remove the FPC/FFC.



1) Do not apply excessive force or use any type of tool to operate the actuator.





2) The connector will assure reliable performance when the actuator is open to 130° maximum. Do not exceed this angle, as this may cause permanent damage to the connector.



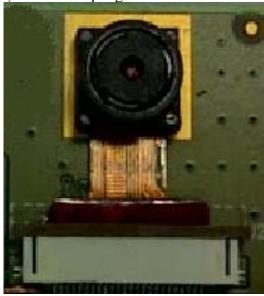
3) Application of excessive force to the inserted FPC/FFC may cause damage to connector and may affect the reliability of electrical connection. If specific application requires continuous or repeated pull or bend of the inserted FPC/FFC, assure that the forces are NOT transmitted directly to the connector.



Precaution for assembling the module to terminal unit

CAMERA MODULE

The temperature of running module is high base on the high-integrated sensor. In order to enhance the heat dissipation and reduce the noise infection from high temperature, TRULY recommend that the module's backside should be touched with rigid material directly, like as PCB or metal. If necessary, it's recommended the module backside is affixed with the materials which can transfer heat, like as electric-fabric, electric-adhesive, or electric-sponge.



Precaution for soldering the CCM:

| | Manual soldering | Machine drag soldering | Machine press soldering |
|-----------------|------------------------------|-----------------------------------|---|
| No ROHS product | 290°C ~350°C. Time: 3-5S. | 330°C ~350°C. Speed: 4-8 mm/s. | 300°C ~330°C. Time: 3-6S. Press: 0.8~1.2Mpa |
| ROHS product | 340°C ~370°C. Time: 3-5S. | 350°C ~370°C. Speed: 4-8 mm/s. | 330°C ~360°C. Time: 3-6S. Press: 0.8~1.2Mpa |

- (1) If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the lens surface with a cover during soldering to prevent any damage due to flux spatters.
- (2) The CCM module and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

Other precautions

For correct using please refer to the relative criterions of electronic products.

Limited Warranty

Unless agreed between TRULY and customer, TRULY will replace or repair any of its CCM modules which are found to be functionally defective when inspected in accordance with TRULY CCM acceptance standards for a period of one year from date of shipments. Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of TRULY limited to repair and/or replacement on the terms set forth above. TRULY will not be responsible for any subsequent or consequential events.

Return CCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

- -Holder is apart from module.
- -Holder or Connector is anamorphic.
- -Connector is turnup.
- -FPC is lacerated or disconnexion, and so on.

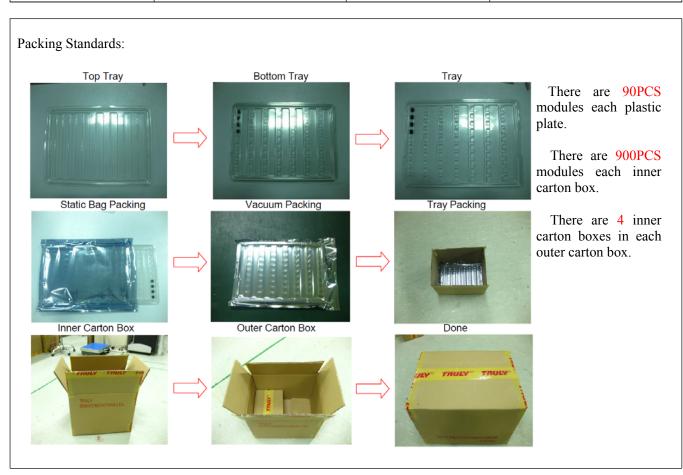
Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet, conductors and terminals.



Package Specification

Packaging Design One

| Product No. | CM6128-B200SF-E | Release date | | |
|---|---|------------------|---------|-----------|
| Product name | Compact Camera Module | Releaser | | |
| Supplier | TRULY OPTO-ELECTRONICS LTD. | Recycle | □YES | ■ NO |
| Quantity/ each box | 3600PCS | Material for box | ■ paper | ☐ plastic |
| Outer carton box size | 405mm*290mm*290mm | | | |
| Quantity / inner box * Quantity / outer box | 90PCS * 10 = 900PCS 900PCS * 4 = 3600PCS | Box type | ■new | □update |



Requirements of outer carton box:

1. Weight(Max): 0.75 Kg2. Height (Max): 0.29 M 3. Prohibition: Box made by log

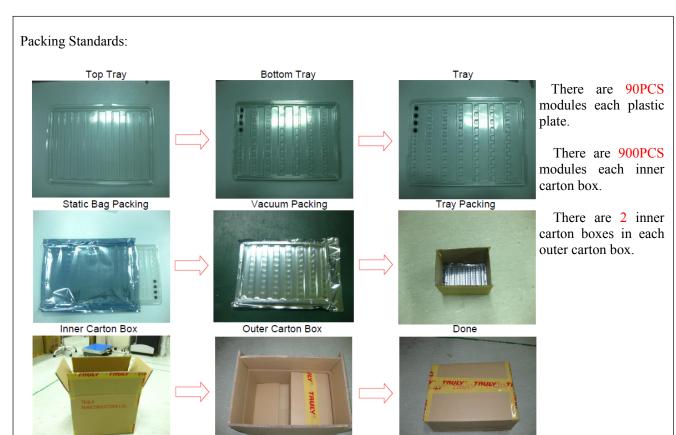
Material for Plastic tray

It is made of antistatic polystyrene which has no chemical pollution. Surface resistivity: 10⁶ ohm/sq



Packaging Design Two

| Product No. | CM6128-B200SF-E | Release date | | |
|---|---|------------------|---------|-----------|
| Product name | Compact Camera Module | Releaser | | |
| Supplier | TRULY OPTO-ELECTRONICS LTD. | Recycle | □YES | ■ NO |
| Quantity/ each box | 1800PCS | Material for box | ■ paper | ☐ plastic |
| Outer carton box size | 405 mm *290 mm *170 mm | | | |
| Quantity / inner box * Quantity / outer box | 90PCS * 10 = 900PCS 900PCS * 2 = 1800PCS | Box type | ■new | □update |



Requirements of outer carton box:

4. Weight(Max): 0.65 Kg 5. Height (Max): 0.17 M6. Prohibition: Box made by log

Material for Plastic tray

It is made of antistatic polystyrene which has no chemical pollution. Surface resistivity : $10^6 \, \text{ohm/sq}$

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Prior Consult Matter

- 1. ①For Truly standard products, we keep the right to change material, process for improving the product property without notice on our customer.
 - ②For OEM products, if any change needed which may affect the product property, we will consult with our customer in advance.
- 2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.

Factory Contact Information

FACTORY NAME: TRULY OPTO-ELECTRONICS LTD.

FACTORY ADDRESS: Truly Industrial Area, ShanWei City, GuangDong, China

FACTORY PHONE: 86-0660-3380061 FAX: 86-0660-3371772