Purpose: The mission of this lab is to investigate the use of multiple seven segments simultaneously. For this purpose, propose and implement a mini VHDL project that uses multiple seven segments. Implement modular design (no operations inside the top module, only connections). Run test bench for each individual module.

NOTES:

1. You must prepare and upload your preliminary report to Moodle before its deadline. Late submissions are not allowed. If you have not submitted your preliminary work on time, you are welcome to attend the lab but you will get zero from that lab.
2. You must show your lab results (Demo on BASYS 3, test bench simulation) to your assistant and get his/her approval in lab hours.
3. Before you leave the lab, you must upload the lab reports to Moodle. You are now allowed to write your reports after the lab. Late submissions are now allowed.
4. The photographs of VHDL codes will not accepted and you should include them to your lab reports by just copy-pasting.
5. You can write your lab report in Open Office/Microsoft Office. After the completing writing process, “Save the report in pdf format”, upload it to Moodle before leaving the laboratory. This report will also be used as a proof of your attendance. Your laboratory report is an individual effort and should be unique. Original work is required by all the students (NO PHOTOCOPIES, DUPLICATE PRINTOUTS OR CHEATING)

- **The Lab Preliminary Report** should contain the following (necessarily in this order):

- **Heading**

  The experiment number, lab title, your name, and date should be at the top right hand side of each page.

- **Abstract / Objective**

  The purpose of the abstract is to provide a brief overview of the report. In your own words, state the purpose of the laboratory exercise, the basic concepts covered, a very brief (two or three sentences) overview of the procedure followed.

- **Design Specification Plan**

  For a set of requirements, there are many ways to design a system that meets the requirement. The Design Specification Plan describes the methodology chosen and the reason for the selection (why).

- **Proposed Design Methodology**

  The experiment can be done from the information given in your report. Include the needed steps taken in the design of the circuit: Seven Segment Display, Logic Schematic Diagram, Truth Table, assumptions, definitions, Karnaugh Map(s), algebraic simplification steps, test plan etc…, if necessary. The proposed design procedure section should be a few paragraphs and no longer than one page.

- **VHDL Model and VHDL Test Bench**

  You should write VHDL code for your design and VHDL Test Bench code to test your implementation. While writing your codes, you should pay attention to the algorithm that you are using. The exact details of the VHDL language are not important at this stage of the preliminary work.

- **The Lab Report** should contain the following (necessarily in this order):

- **Heading**

  The experiment number, the lab title, date of the experiment, your section and your name should be at the top right hand side of each page.

- **The Design Methodology**

  The design methodology presents much of theory behind the lab exercise, which was confirmed with software simulation, hardware implementation, algebraic, etc. You should write how to design it. Please do not copy text from your "Proposed Design Methodology" part of your Preliminary Work. You must write the changes according to the "Proposed Design Methodology" which have mentioned to your Preliminary Work.

- **Results**

  In this section, you should clearly explain needed steps what to do in the lab and how to generate your circuit in XILINX to the BASYS 3 Board. The laboratory report is the record of all work pertaining to your experiment. The results section will have subsections if there is more than one result to present. You will include the results of your design procedure. The results section will typically attach your 7-Segment Display configuration, equations, circuit diagrams, RTL Schematic diagram, simulation commands, waveforms, etc., if necessary. Any of included figures must be labeled. All results must be explained and discussed.

- **Conclusion**

  In this section you should write about the concepts that you learned in the laboratory and how they relate to other aspects of the course or digital design in general. If you experienced problems or obtained data that was incorrect, here is where you might elaborate on the causes and ideas for solutions.

- **Appendices**

  Other materials that are referred in your report should be here. Typically you should attach your VHDL code, VHDL Test Bench code, Pin Assignment (.ucf file) here.