Lab 5 Preliminary Report

Labwork 5
ALU using VHDL
02.11.2018
Şevki Gavrem Kulkuloğlu
21601793 EE 102 -2

• Objective

- Our purpose in this experiment is to design an advanced arithmetic logic unit (ALU) which is going to be capable of some operations. In my design it is going to be capable of addition, subtraction, multiplication and taking the square of the bigger input. I will take inputs by switches and show all variables on the seven-segment display.

• Design Specification Plan

- I am going to design a system that takes 2 3-bit inputs and via using operation switches it is going to be able to operations between these 2 inputs which are addition, subtraction, multiplication and taking the square of the bigger input. It is going to be like a basic calculator with design a simplest way and also it is giving the opportunity to obtain octal result of operations of two binary numbers.

• Proposed Design Methodology

- In my design I am going to take two 3-bit binary inputs form 3 most significant switches and 3 right least significant switches. I will use 2 switches on the middle for changing the operations between addition, subtraction, multiplication and taking the square of the bigger input. There will be a reset switch located next to operation switches. I am going to display my inputs and output which is the result of the which operation used, as octal and inputs on the 2 most significant seven segment displays, and output on 2 least significant seven segment displays.

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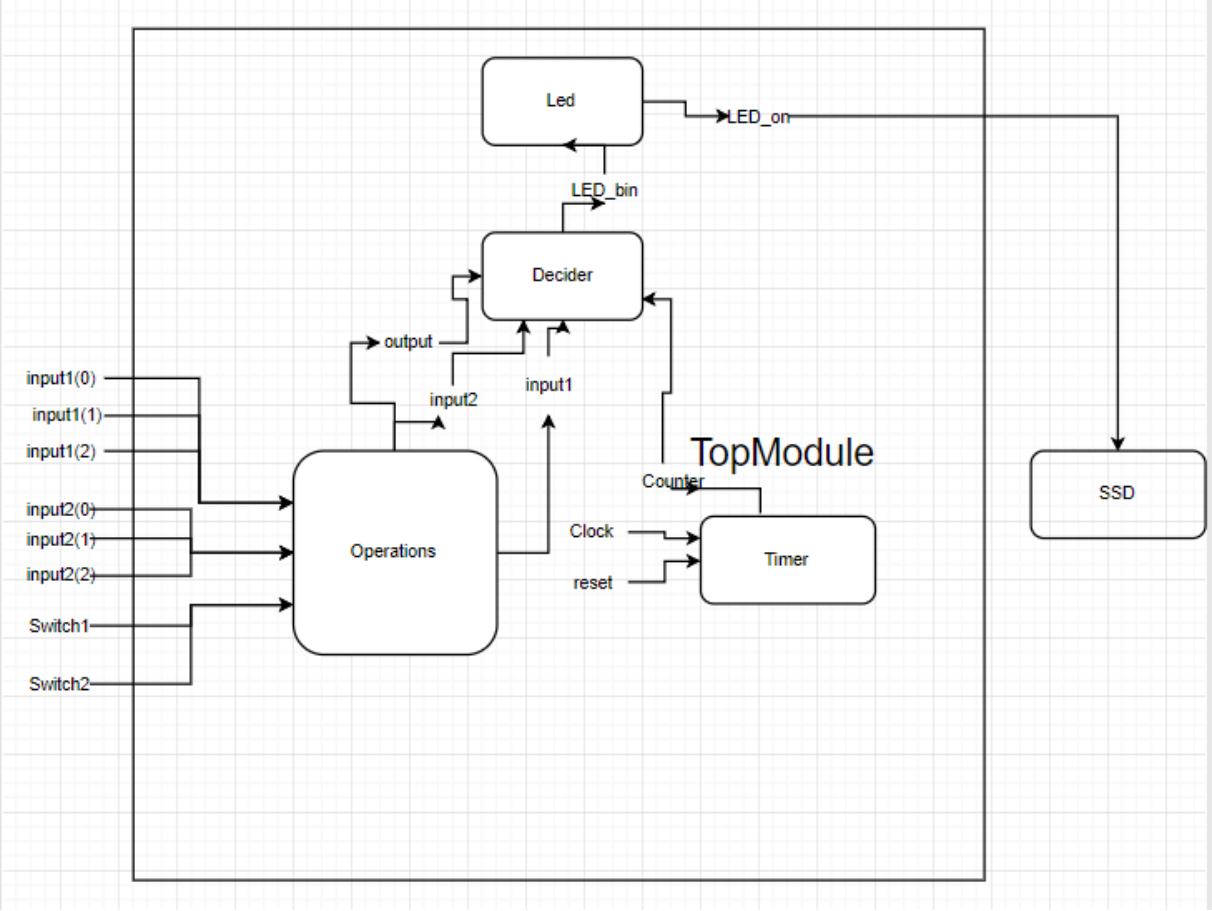

- VHDL Module

- I will have 4 sub module which are Operations, Timer, Decider and Led and a Top module in which these sub modules are going to be connected. In operations sub module I will take 8 inputs by 8 switches, first 3 switches will represent input1, last three switch will represent input2 and remaining 2 switches will be the operation changing switches. Input1, input2 and output (the result of the which operation used) will be the output of this sub module. In Timer sub module I will take 2 inputs clock and reset. Clock will be taken from basys3 and reset from a switch. Counter will be the output of this sub module. Outputs of the Timer and Operations which are counter, input1, input2 and output will be the input of decider sub module. The output of the decider module is Led_bin and it is input of Led sub module. Led_on is the output of the Led sub module and the output of the total design (TopModule).