Purpose:

In this experiment, you will design and implement an advanced arithmetic logic unit (ALU) and explain the circuit that you designed on RTL schematic on BASYS 3. Also, comment on your project design summary reports.

NOTES:

1. You must prepare and upload your preliminary work report to Moodle before its due date. *Late submissions are not allowed*. If you have not done your preliminary work on time, you are welcome to attend the lab but you will get zero from that lab.

2. You must show your lab results (Demo on BASYS 3, test bench simulation) to your assistant and get his/her approval in lab hours.

3. Before you leave the lab you must upload the Lab reports to Moodle. You are not allowed to write your reports after the lab. *Late submissions are not allowed*.

4. The photographs of VHDL codes will not accepted and you should include them to your lab reports by just copy pasting.

5. You can write your lab report in Open Office/Microsoft Office. After the completing writing process, **"Save the report in pdf format",** upload it to Moodle before leaving the laboratory. This report will be also used as a proof of your attendance. Your laboratory report is an individual effort and should be unique. Original work is required by all the students. (NO PHOTOCOPIES, DUPLICATE PRINTOUTS OR CHEATING).

- **The Lab Preliminary Report** should contain the following (necessarily in this order):

  - **Heading**

    The experiment number, the lab title, your name, and date should be at the top right hand side of each page.

  - **Abstract / Objective**

    The purpose of the abstract is to provide a brief overview of the report. In your own words, state the purpose of the laboratory exercise, the basic concepts covered, a very brief (two or three sentences) overview of the procedure followed.

  - **Design Specification Plan**

    For a set of requirements, there are many ways to design a system that meets the requirement. The Design Specification Plan describes the methodology chosen and the reason for the selection (why).

  - **Proposed Design Methodology**

    Design an arithmetic logic unit that is capable of computing function(s) you would like to have. You may take your inputs from switches on FPGA board or by some other ways you would like to. You may show your outputs on LED(s) or 7-segment display. Describe function(s) of your ALU. Show your block diagram of your design and corresponding top module and VHDL modules. Write your logic equations and draw your circuit diagram.

  - **VHDL Model**

    In this preliminary work, you do not have to write VHDL codes but explain VHDL module(s), how you will implement them and your inputs/outputs.

- **The Lab Report** should contain the following (necessarily in this order):

  - **Heading**

    The experiment number, the lab title, your name, and date should be at the top right hand side of each page.

  - **Design Methodology**

    The design methodology presents much of theory behind the lab exercise, which was confirmed with hardware implementation, algebraic, etc. You should write how to make design it, so you might re-state your function(s) of your ALU, logic equations, circuit diagram, VHDL block diagram etc. in preliminary work. Also, include final version of all VHDL module(s), top module and ucf/xdc file. Also, you must write the changes according to the "Proposed Design Methodology" compared to your preliminary work.

  - **Results**

    In this section, you should include your observvations. The laboratory report is the record of all work pertaining to your experiment. The results section will have subsections if there is more than one result to present. You will include the results of your design procedure. The results section will typically attach observations on LED(s)/7-segment display(s) on FPGA board, RTL schematics and project design summary report. Any of included figures must be labeled. All results must be explained and discussed.

  - **Discussion and Conclusion**

    You may compare your initial circuit diagram with RTL schematic and try to understand relation between VHDL code-RTL schematics. Make some comments about your observations about VHDL code-RTL schematics. Also, it is expected that you should make comments on project design summary report. You have to realize that FPGA board you have been using has some hardware implementation limits. In addition, you should write about the concepts that you learned in the laboratory and how they relate to other aspects of the course or digital design in general. If you experienced problems or obtained data that was incorrect, here is where you might elaborate on the causes and ideas for solutions.